Pixel Trigger

Pixel Processor
- BX Order and expand
- L1 Buffer
- Cluster find
- Translate row-col to X-Y
- Pattern match

Track Processor
- Connect segments by quadrant
- Diagnostic Buffer

Vertex Processor
- Project tracks to interaction region
- Calculate hit parameters

Trigger Events

L1 Hits to DA

Segments

Tracks
Current or Permanent:
- Implemented in FPGA.
- FO Links between detector area and trigger and DAQ upstairs.

Options that need more info:
- Hold raw data or translated data in L1 buffer.
- Simple or CENTER-OF-MASS cluster finder? Some analog or all digital data?
- Combine columns data into cluster processing?
- Need to simulate pattern-matching algorithms to select between BB33 and sweep.
- Where to split the hardware upstairs and downstairs?
- Define the dividing line between the pixel and trigger groups’ efforts.
Current or Permanent:
- Implemented in a floating point Digital Signal Processor.

Options that need more info:
- Microprocessor, DSP or neural net?
- Partition as quadrants or in Z?
- Cut segments first or after track finding?
- Remove quadrant segmentation at this step?
Current or Permanent:
- Implemented in a floating point Digital Signal Processor.

Options that need more info:
- Could this be done in the same fixed point DSP as the track processing?
- What information must the trigger output contain?
Current Efforts:

- Simulations of segment algorithms – Erik & Penny
- Data flow and queuing analysis - ESE
- Pixel processor subgroup - Gustavo
- DSP software investigation – Erik.
BB33 Algorithm
Station-5
Quad-1
Pixel
Processor

Station-6
Quad-1
Pixel
Processor

Station-7
Quad-1
Pixel
Processor

Pixels In

XY

XY

XY

Segments Out

Sweep Algorithm
Station-5/6 Quad-1
Station-6/7 Quad-1
Station-7/8 Quad-1

Pixels In

Y-Doublets + X Hits Out

Triplet Finder & X verifier
Triplet Finder & X verifier
Triplet Finder & X verifier

Segments Out

Combined Algorithm