Serial Input Register

Incoming bits are synchronized using a 16x clock. The SYNC counter is started at 9, on the rising edge of a start bit. Each time it passes through 0 (MID=1), a bit is sampled.

On the 37th bit, DAV is asserted. On the 38th bit, parity and framing are checked and START is cleared.

The SWAP control allows bits 16-31 to be swapped down to bits 0-15 for readout on a 16-bit bus.