October 15th tests
Worked with Denis CALVET and Emmanuelle PEREZ to exercise the ADF input channels.
Exercised the channels with different pulse amplitudes, results where consistent with what expected.

Prototype System
- Hardware
  a) Xilinx X2S150 FPGA Test Card (Digital)
  b) AD9765 Test Card (Digital to Analog Conversion)
  c) AD8138 Card (Amplification/Filtering)
  d) Custom power supply card
  e) Requires an external dual power supply (±7 Volt min)
- Software
  a) Interface with the outside world over RS232 serial ports.
  b) Provided GUI requires a personal computer with windows OS and MS Excel.

TWG Documentation:
http://www-ese.fnal.gov/D0Cal_TWG/
Xilinx X2S150 FPGA Test Card

HP 16500 Logic Analyzer Test Pods

Control

1024 x 12bit Memory

1024 x 12bit Memory

Voltage Regulator +5V

Voltage Regulator +3V (Digital)

Voltage Regulator +5V (Analog)

Voltage Regulator -5V (Analog)

Voltage Regulator +5V (Analog)

Voltage Regulator +5V

AD9765 Test Card

AD8138 Test Cards

Voltage Regulator +5V

Voltage Regulator -5V

AD8138 Amplifier/Filter

AD8138 Amplifier/Filter

JTAG

RS232

PC Windows OS

Dual Power Supply +7 Volt -7 Volt

Output Connector

10-bit counter

10-bit counter

X2S150 FPGA

HP 16500 Logic Analyzer Test Pods

EEprom

40MHz OSC

Voltage Regulator +5V

Voltage Regulator -5V

X2S150 FPGA Test Card

Voltage Regulation Custom Card