TWG Prototype System status

Software:
- Completed modification of the software to control the SCL Teststand at FCC. This provides a platform to test the TWG/SCL synchronization features.

Hardware:
- No relevant changes to report.

Work in progress:
- Still working on modification of Xilinx firmware to use SCL timing for triggering [Report Dec 11 2003].
- Implementation of filtering (in the amplification stages) to limit bandwidth of output signals [Report Nov 13 2003].
- Investigating improvements of the system clock (currently 40 MHz) [Report Oct 30, 2003].
- Documentation/web page updates.

TWG System
Work in progress on:
- Specification proposal.
  Comments and ideas are very welcome [Report Nov 13 2003].

TWG Documentation (including this report):
http://www-ese.fnal.gov/D0Cal_TWG/