Test Waveform Generator System  
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TWG Prototype System status

Software:  
- No relevant changes to report.

Hardware:  
- No relevant changes to report.

Work in progress:  
- Still working on modification of Xilinx firmware to use SCL timing for triggering [Report Dec 11 2003].
- Implementation of filtering (in the amplification stages) to limit bandwidth of output signals [Report Nov 13 2003].
- Investigating improvements of the system clock (currently 40 MHz) [Report Oct 30, 2003].
- Documentation/web page updates.

TWG System

Work in progress on:  
- Specification proposal for 32 channels system.  
  Currently focused on form factor (probably VME 6U) and multiple board synchronization.  
  Comments and ideas are very welcome [Report Nov 13 2003].

TWG Documentation (including this report):  
http://www-ese.fnal.gov/D0Cal_TWG/