TWG Prototype System status

Software:
- No relevant changes to report.

Hardware:
- Added SCL interface in order to get the system synchronized for future tests.
  a) Manufactured passive adapter to connect Xilinx Test card and SCL receiver.
  b) Modified Xilinx card firmware to allow for adapter connection.

Work in progress:
- Modification of Xilinx firmware to use SCL timing for triggering.
- Implementation of filtering (in the amplification stages) to limit bandwidth of output signals [Report Nov 13 2003].
- Investigating improvements of the system clock (currently 40 MHz) [Report Oct 30, 2003].
- Documentation/web page updates.

TWG System

Work in progress on:
- Specification proposal.
  Comments and ideas are very welcome [Report Nov 13 2003].

TWG Documentation (including this report):
http://www-ese.fnal.gov/D0Cal_TWG/
SCL Passive Adapter