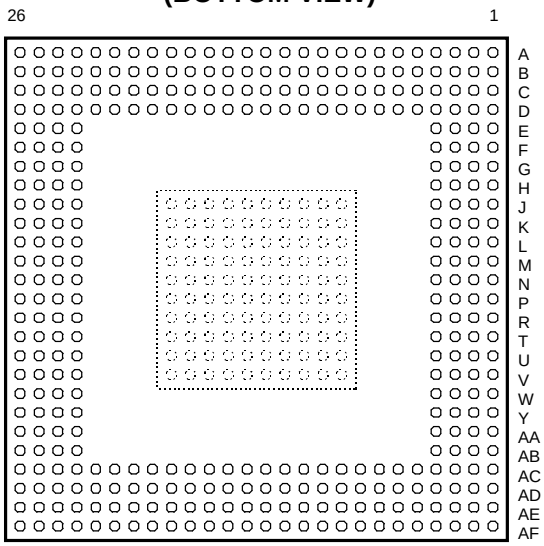
Note: The timing parameters will be disclosed in September 1997.

- **Highest Performance Fixed-Point Digital Signal Processor (DSP)**
  - **TMX320C6201:**
    5ns Instruction Cycle Time
    8 x 32-bit Instructions/Cycle
    1600 MIPS
    200 MHz Internal Clock Rate
- **VelociTI™ Advanced Very Long Instruction Word (VLIW) CPU**
  - **8 Highly Independent Functional Units:**
    6 ALUs (32- / 40-Bit)
    2 16-Bit Multipliers (32-Bit Results)
  - **Load-Store Architecture:**
    32 32-Bit General Purpose Registers
  - **Instruction Packing Reduces Code Size**
  - **100% Conditional Instructions**
- **Instruction Set Features**
  - **Data Byte Addressable (8-,16-,32-Bit Data)**
  - **32-Bit Address Range**
  - **8-Bits Overflow Protection**
  - **Saturation**
  - **Bit-Field Extract, Set, Clear**
  - **Bit Counting**
  - **Normalization**
  - **Register or 5-Bit Constant Index**
  - **15-Bit Positive/Negative Offset From Either B14 or B15 Register**
- **One Megabit On-Chip SRAM**
  - **512K Bit Internal Program/Cache**
  - **512K Bit Dual Access Internal Data**
- **32-Bit External Memory Interface**
  - **Glueless Interface To Synchronous Memories:**
    SDRAM
    SBSRAM
  - **Glueless Interface To Asynchronous Memories:**
    SRAM
    EPROM
- **4 Channel Bootloading Direct Memory Access Coprocessor (DMA)**
- **2 Multi Channel Serial Ports**
  - **Direct Interface To T1/E1 Framers**
  - **Compatible With MVIP And ST Bus**
  - **128 Channels**

PACKAGE
(BOTTOM VIEW)



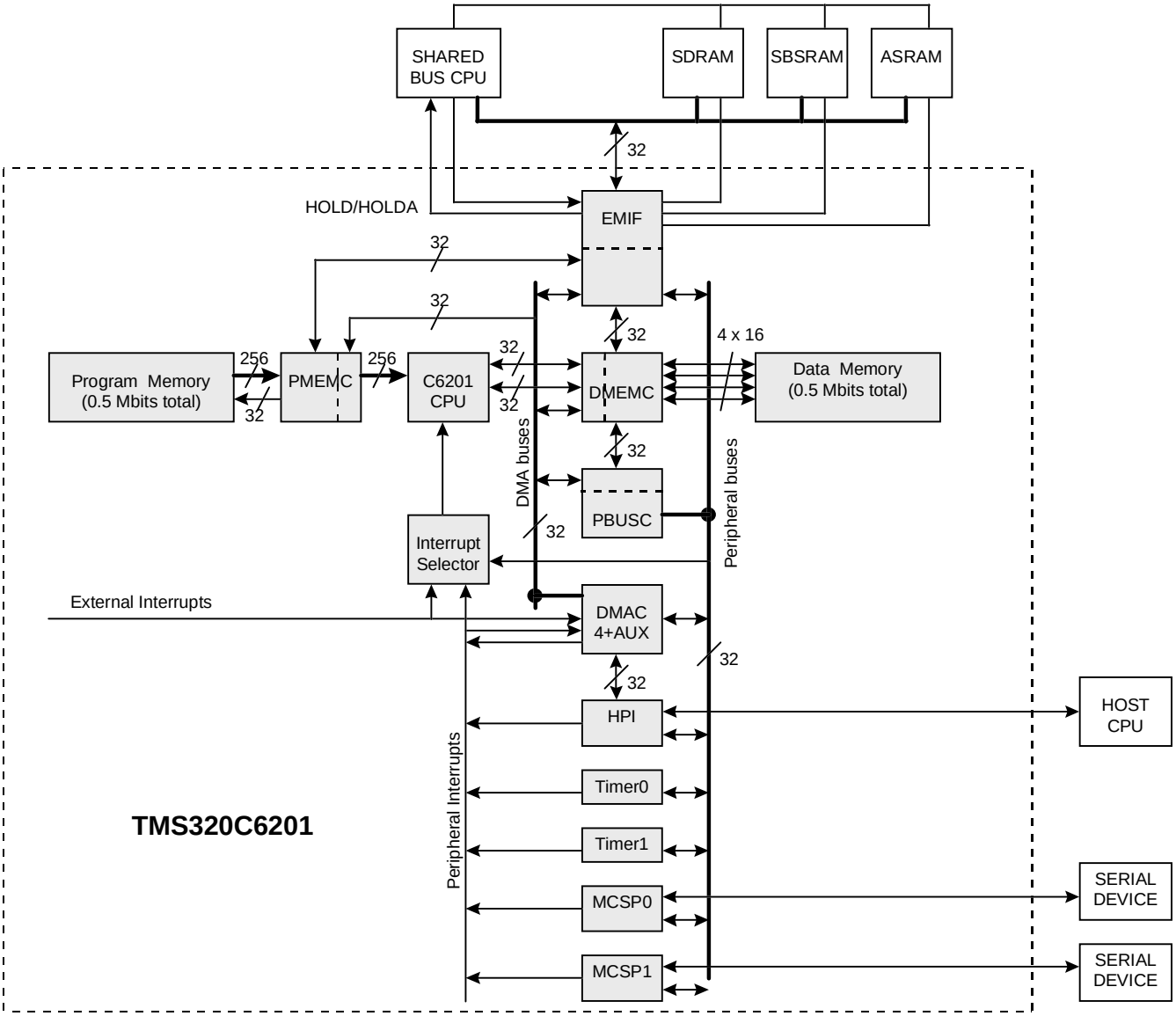
- **2 32-Bit General Purpose Timers**
- **IEEE-1149.1 (JTAG) Boundary-Scan Compatible**
- **352-Lead Ball Grid Array Package (BGA)**
- **0.25 Micron / 5-Level Metal Process**
  - **CMOS Technology**
- **3.3V I/Os, 2.5V Internal**

PRELIMINARY INFORMATION

Note: The timing parameters will be disclosed in September 1997.

PRELIMINARY INFORMATION

architecture



DMEMC - Data Memory Controller

PMEMC - Program Memory Controller

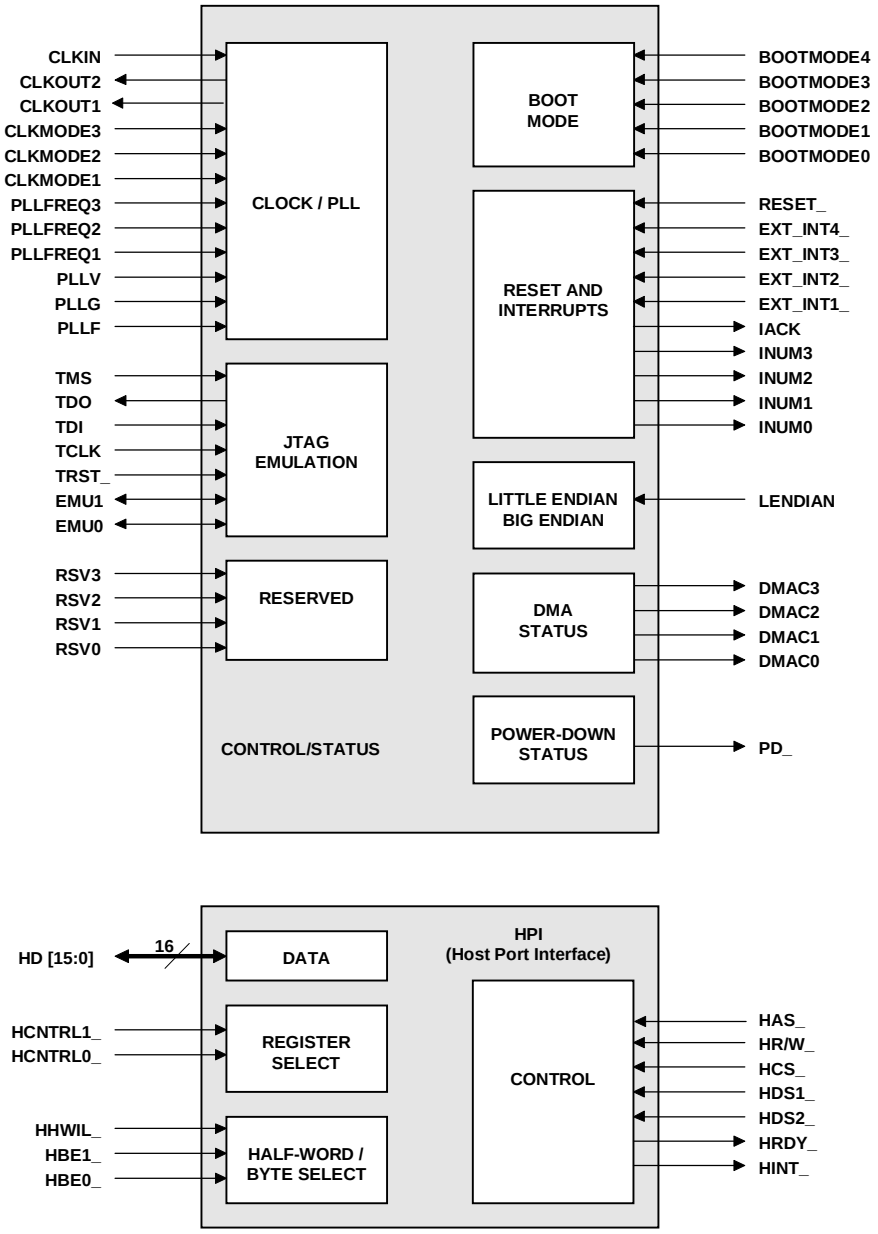
PBUSC - Peripheral Bus Controller\

DMAC - DMA Controller

HPI - HOST PORT INTERFACE

TMS320C6201 Block Diagram

signal groups

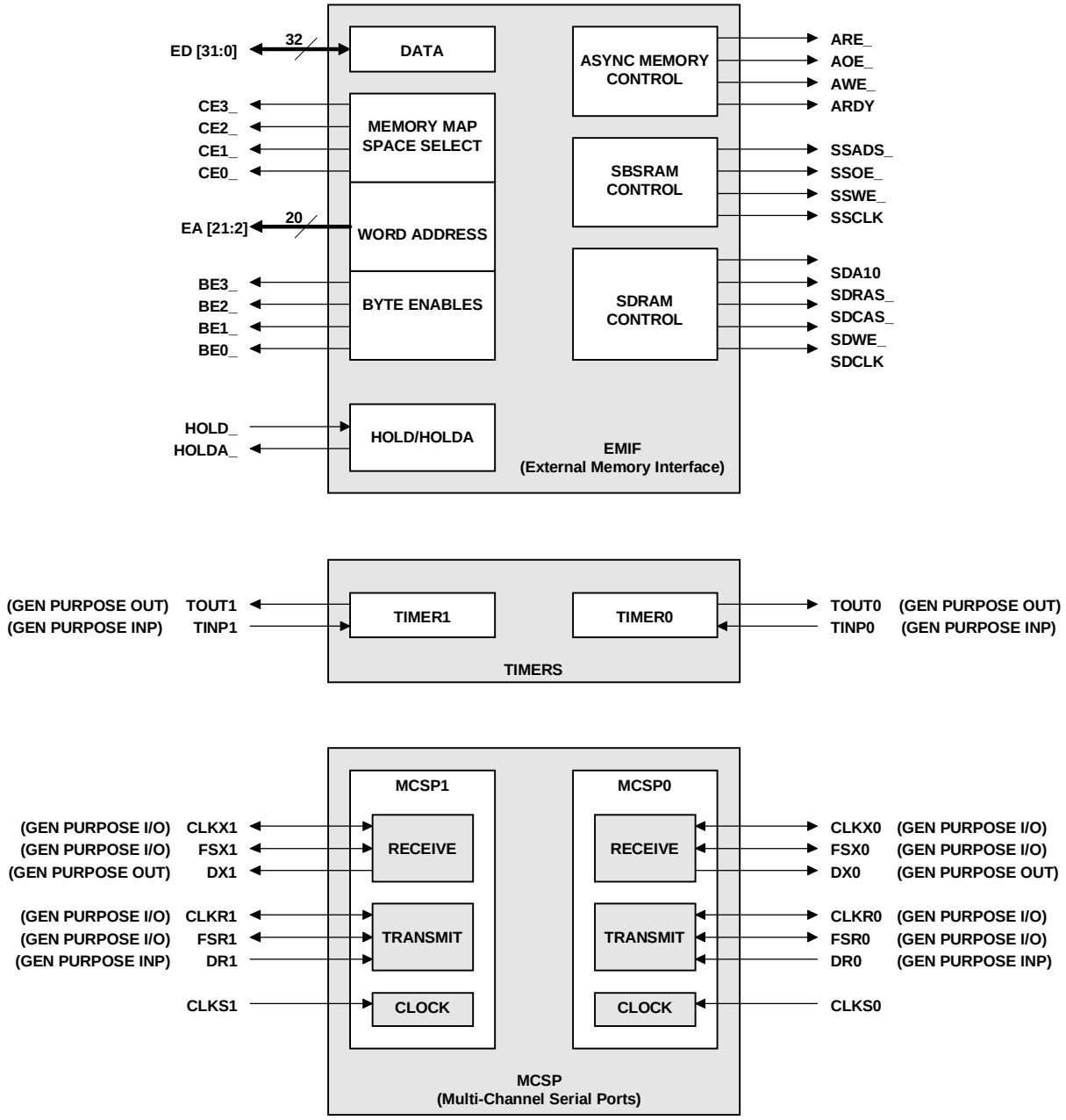


TMS320C6201 CPU and Peripheral Signals

PRELIMINARY INFORMATION

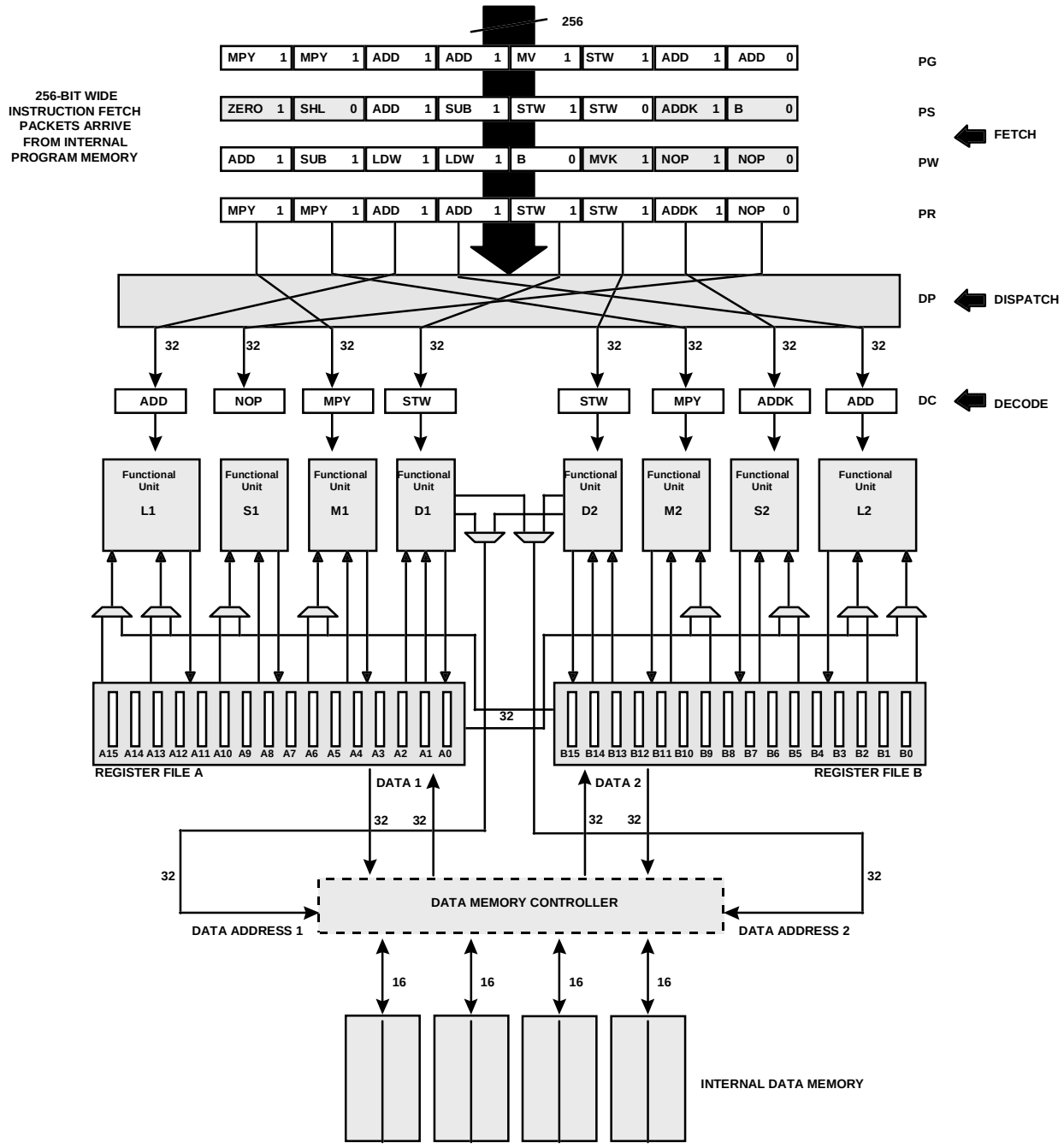
Note: The timing parameters will be disclosed in September 1997.

PRELIMINARY INFORMATION



TMS320C6201 Peripheral Signals

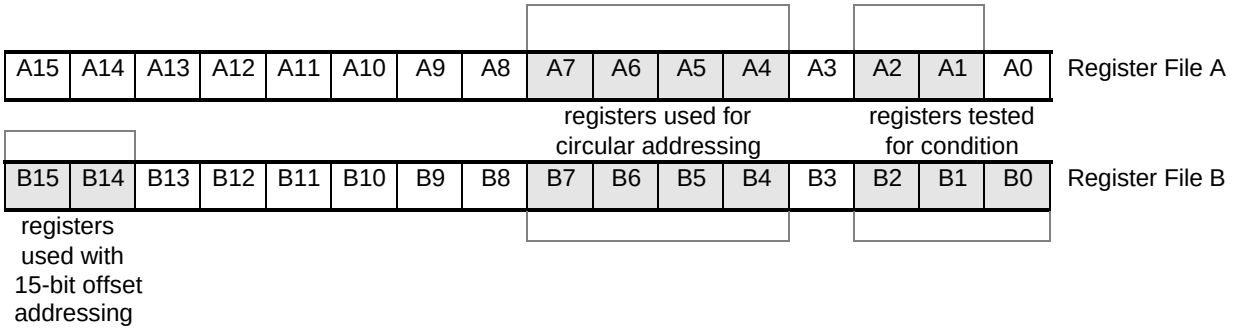
CPU



TMS320C6201 CPU Functional Diagram

PRELIMINARY INFORMATION

CPU Registers



General Purpose Register Files

Control Registers

Acronym	Name	Description
AMR	Addressing mode register	Specifies whether to use linear or circular addressing for one of eight registers. Also contains block sizes for circular addressing.
CSR	Control status register	Contains the global interrupt enable bit, cache control bits, and other miscellaneous control and status bits
PCE1	Program counter	Contains the address of the fetch packet that contains the execute packet in the E1 pipeline stage
IN	Reserved	
OUT	Reserved	
PDATA_O	Reserved	
IER	Interrupt enable register	Allows enabling/disabling of individual interrupts
IFR	Interrupt flag register	Displays status of interrupts
ISR	Interrupt set register	Allows to manually set pending interrupts
ICR	Interrupt clear register	Allows to manually clear pending interrupts
ISTP	Interrupt service table pointer	Points to the beginning of the interrupt service routine
IRP	Interrupt return pointer	Contains the address to be used to return from a maskable interrupt
NRP	Non-maskable interrupt return pointer	Contains the address to be used to return from non-maskable interrupt

PRELIMINARY INFORMATION

	31 26	25 21	20 16	15 14	13 12	11 10	9 8	7 6	5 4	3 2	1 0
AMR	rsv	BK1	BK0	B7m	B6m	B5m	B4m	A7m	A6m	A5m	A4m
	reserved	block size 1	block size 0	linear or circular addressing mode select							

	31 24	23 16	15 10	9	8	7 5	4 2	1	0
CSR	CPU ID	REVISION ID	PWRD	SAT	EN	PCC	DCC †	PGIE	GIE
	CPU type identification	silicon identification	power-down modes	saturate status	endian control	program cache control	data cache control	previous GIE state	global interrupt enable

† not used on 320C6201 (reserved)

	31 0
PCE1	Program Counter (address of Fetch Packet containing Execute Packet in the E1 pipeline stage)
IN	Reserved
OUT	Reserved
PDATA_O	Reserced

	31 16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IER	reserved	IE15	IE14	IE13	IE12	IE11	IE10	IE9	IE8	IE7	IE6	IE5	IE4	rsv	rsv	NMIE	0

	31 16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IFR	reserved	IF15	IF14	IF13	IF12	IF11	IF10	IF9	IF8	IF7	IF6	IF5	IF4	rsv	rsv	NMIF	0

	31 16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ISR	reserved	IS15	IS14	IS13	IS12	IS11	IS10	IS9	IS8	IS7	IS6	IS5	IS4	rsv	rsv	rsv	rsv

	31 16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ICR	reserved	IC15	IC14	IC13	IC12	IC11	IC10	IC9	IC8	IC7	IC6	IC5	IC4	rsv	rsv	rsv	rsv

	31 10	9 5	4	3	2	1	0
ISTP	ISTB	HPENT	0	0	0	0	0
	interrupt service table base	highest priority IE-enabled interrupt	intr service packet size				
	address of the Interrupt Service Fetch Packet (ISFP) for the highest priority pending interrupt						

	31 0
IRP	Interrupt Return Address

	31 0
NRP	Non-maskable Interrupt Return Address

Note:

only 0's are permitted to be written to reserved fields of the registers.

PRELIMINARY INFORMATION

Note: The timing parameters will be disclosed in September 1997.

PRELIMINARY INFORMATION

Instructions

Instruction Set Summary

Functional Units						
.L unit		.M unit	.S unit			.D unit
ABS	NORM	MPY	ADD	EXT	SET	ADD
ADD	NOT	SMPY	ADDK	EXTU	SHL	ADDA
AND	OR		ADD2	MVC †	SHR	LD mem
CMPEQ	SADD		AND	MV	SHRU	LD mem (15-bit offset) ‡
CMPGT	SAT		B disp	MVK	SSHL	MV
CMPGTU	SSUB		B IRP †	MVKH	STP †	NEG
CMPLT	SUB		B NRP †	NEG	SUB	ST mem
CMPLTU	SUBC		B reg	NOT	SUB2	ST mem (15-bit offset) ‡
LMBD	XOR		CLR	OR	XOR	SUB
MV	ZERO				ZERO	SUBA
NEG						ZERO

† .S2 only ‡ .D2 only

Instruction Execute Phases

instruction type		number of delay slots	execute phases used
Branch	(from E1 of branch to E1 of 1st instruction after branch)	5	E1, , , , , E1
Load	(incoming data)	4	E1, E2, E3, E4, E5
Multiply		1	E1, E2
Load	(address modification)	0	E1
Single-cycle	(ADD, for example)	0	E1
Store		0	E1
NOP	(no execution)	-	-

Pipeline Description

Pipeline stage	pipeline phase	symbol	during this stage:
Program Fetch	Program Address Generate	PG	Address of the Fetch Packet is determined
	Program Address Send	PS	Address of the Fetch Packet is sent to memory
	Program Wait	PW	Program memory read is performed
	Program Data Receive	PR	Fetch packet is expected at CPU boundary
Program Decode	Execute Packet Dispatch	DP	Next Execute Packet sent to Functional Units
	Decode	DC	Instructions are decoded in Functional Units
Execute	Execute 1	E1	Instruction conditions evaluated, operands read Load/Store addresses computed/modified Branches affect Fetch Packet in PG stage Single -cycle results written to register file
	Execute 2	E2	Load address is sent to memory Store/STP address and data are sent to memory Single-cycle instructions may set the SAT bit Multiply results written to the register file
	Execute 3	E3	Load memory reads are continuing Multi-cycle instruction may set the SAT bit
	Execute 4	E4	Load data arrives at the CPU boundary
	Execute 5	E5	Load data is placed in the register

PRELIMINARY INFORMATION

Note: The timing parameters will be disclosed in September 1997.

CPU instruction opcode map

.L unit

31–29	28	27–23	22–18	17–13	12	11–5	4	3	2	1	0
creg	*z*	*dst*	*src2*	*src1/cst*	*x*	*op*	1	1	0	*s*	*p*

.M unit

31–29	28	27–23	22–18	17–13	12	11–7	6	5	4	3	2	1	0
creg	*z*	*dst*	*src2*	*src1/cst*	*x*	*op*	0	0	0	0	0	*s*	*p*

.S unit

31–29	28	27–23	22–18	17–13	12	11–6	5	4	3	2	1	0
creg	*z*	*dst*	*src2*	*src1/cst*	*x*	*op*	1	0	0	0	*s*	*p*

.S unit

31–29	28	27–23	22–7	6	5	4	3	2	1	0
creg	*z*	*dst*	*cst*	1	0	1	0	0	*s*	*p*

MOVK and ADDK instructions

.D unit

31–29	28	27–23	22–18	17–13	12–7	6	5	4	3	2	1	0
creg	*z*	*dst*	*src2*	*src1/cst*	*op*	1	0	0	0	0	*s*	*p*

.D unit

31–29	28	27–23	22–8	7	6–4	3	2	1	0
creg	*z*	*dst/src*	*cst*	*y*	*ld/st*	1	1	*s*	*p*

Load/Store with 15 bit offset

.D unit

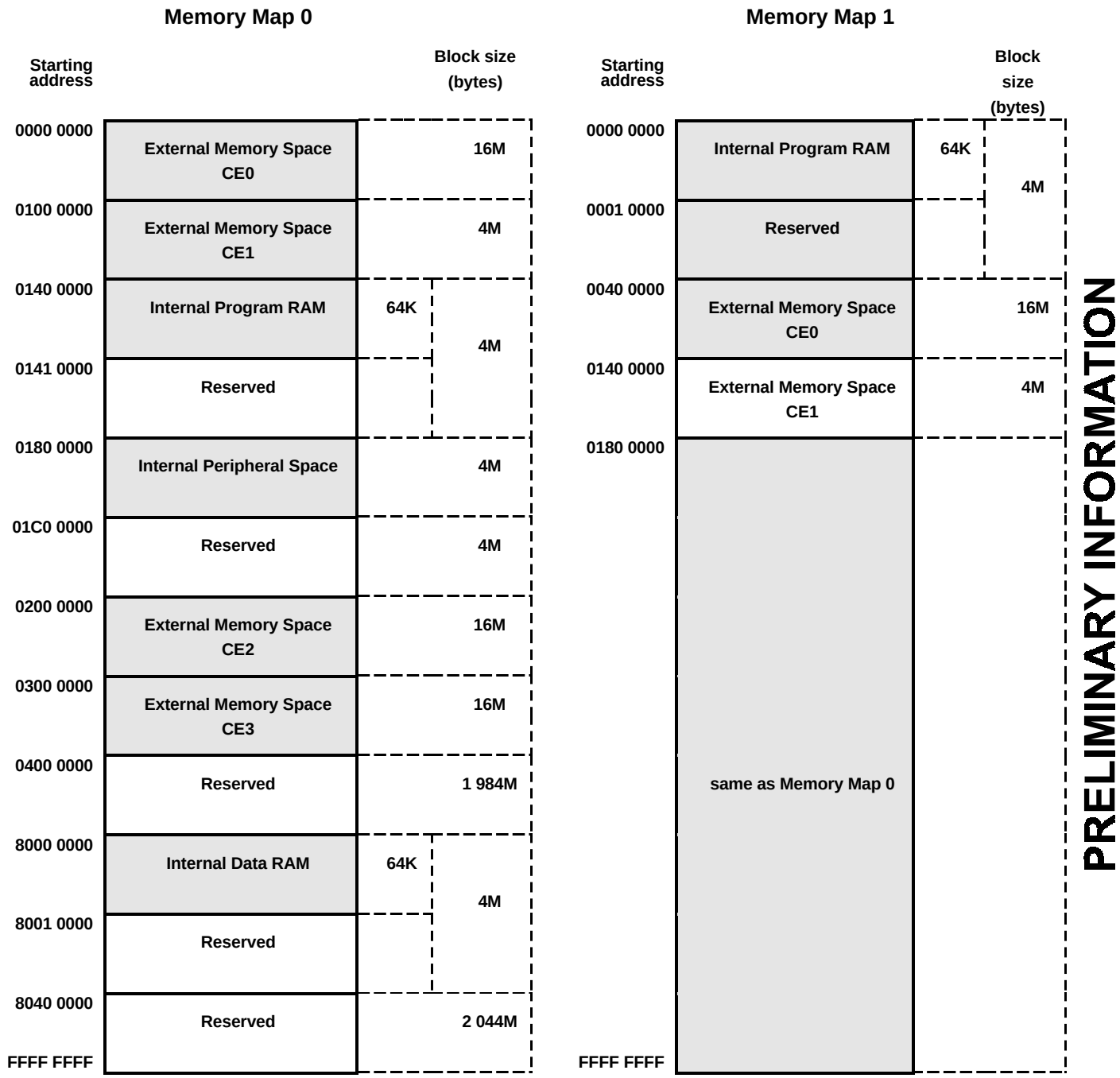
31–29	28	27–23	22–18	17–13	12–9	8	7	6–4	3	2	1	0
creg	*z*	*dst/src*	*base R*	*offset R/cst*	*mode*	*r*	*y*	*ld/st*	0	1	*s*	*p*

Load/Store ‘base R’ + ‘offsetR/cst’

p	parallel instruction	*creg*	condition register (A1, A2, B1, B2, B3, 0000b - always true)
s	destination file A or B	*dst*	destination register
x	cross path	*op*	functional unit operation code
y	base addr in B14 or B15	*cst*	constant
z	test for zero or non-zero	*ld/st*	types of load/store (signed, unsigned, half etc.)
r	reserved	*mode*	addressing mode (linear, circular)

PRELIMINARY INFORMATION

memory map


Memory Map 0
Starting address
Block size (bytes)
0000 0000
External Memory Space CE0
16M
0100 0000
External Memory Space CE1
4M
0140 0000
Internal Program RAM
64K
4M
0141 0000
Reserved
0180 0000
Internal Peripheral Space
4M
01C0 0000
Reserved
4M
0200 0000
External Memory Space CE2
16M
0300 0000
External Memory Space CE3
16M
0400 0000
Reserved
1 984M
8000 0000
Internal Data RAM
64K
4M
8001 0000
Reserved
8040 0000
Reserved
2 044M
FFFF FFFF
Memory Map 1
Starting address
Block size (bytes)
0000 0000
Internal Program RAM
64K
4M
0001 0000
Reserved
0040 0000
External Memory Space CE0
16M
0140 0000
External Memory Space CE1
4M
0180 0000
same as Memory Map 0
FFFF FFFF
PRELIMINARY INFORMATION

Note: The timing parameters will be disclosed in September 1997.

clock characteristics and timing

The 320C6201 uses an external oscillator to drive the on-chip PLL (Phase-Locked Loop) circuit that generates the internal CPU clock. The PLL typically multiplies the external oscillator frequency by 4 and feeds the resulting clock to CLKOUT1 output pin. Other clocks such as CLKOUT2, SDCLK, SSCLK are derived from the internal CPU clock. Most timing parameters of this device are defined relative to the CLKOUT1 clock and specifically to it's rising edge. SDRAM timings are specified relative to SDCLK and SSRAM timings are specified relative to SSCLK.

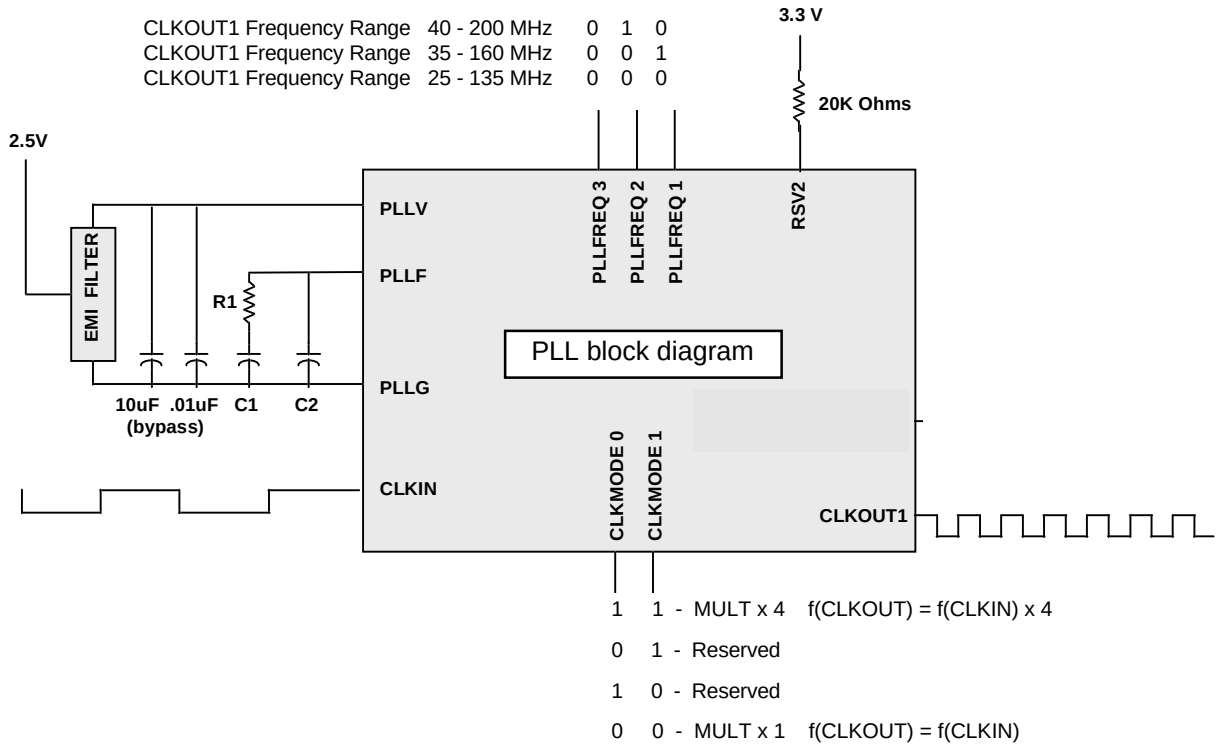
In addition to x4 mode, the clock circuit can operate in multiply by 1 mode, where the internal CPU clock is the same as the CLKIN frequency. The factors to consider in choosing the multiply factor include board level noise and clock jitter. The x4 mode will minimize the board noise, while the x1 mode will reduce the jitter. The clock mode is controlled by two CLKMODE pins.

The amount of time that the PLL needs to synchronize to the output frequency depends on the CLKIN and CLKOUT1 frequencies and is typically in the range of tens of microseconds. See the PLL Component Selection table for the exact time. The synchronization time affects the duration of the Reset signal in that the Reset has to be asserted long enough for the PLL to synchronize to the programmed output frequency.

Three PLLFREQ pins identify the range of CLKOUT1 frequencies that the PLL is expected to synchronize to. The PLL also requires 2 bypass capacitors (between PLLV and PLLG), external low-pass filter components (R1, C1 ,C2) and the EMI filter. The values for R1, C1, C2 and the filter depend on the CLKIN and CLKOUT1 frequencies. Refer to the PLL Component Selection table to chose correct values for the PLL external components and the EMI filter.

PRELIMINARY INFORMATION

clock PLL



Note:

1. For CLKMODE x4, values for C1, C2 and R2 depend on CLKIN and CLKOUT frequencies.

2. For CLKMODE x1, the PLL is by-passed and all six external PLL components can be removed. For this case, the PLLV terminal has to be connected to a clean 2.5V supply and the PLLG and PLLF terminals should be tied together.

3. Due to overlap of frequency ranges when choosing the PLLFREQ more that one frequency range can contain the CLKOUT1 frequency. Choose the lowest frequency range including the desired frequency. For example, for CLKOUT1 = 133MHz, chose PLLFREQ value of 001b. For CLKOUT1 = 166 or 200MHz choose PLLFREQ value of 010b. PLLFREQ values other then 000b, 001b and 010b are reserved.

PRELIMINARY INFORMATION

Note: The timing parameters will be disclosed in September 1997.

PLL component selection table

cycle time (ns)	CLKMODE	CLKIN (MHz)	CLKOUT1 (MHz)	R1 (Ω)	C1 (uF)	C2 (pF)	EMI filter part no.	Lock Time (us) †
5	x4	50	200	16.9	.15	2700	TDK #153	59
5.5	x4	45.5	181.8	13.7	.18	3900	TDK #153	49
6	x4	41.6	166.7	17.4	.15	3300	TDK #153	68
6.5	x4	38.5	153.8	16.2	.18	3900	TDK #153	70
7	x4	35.7	142.9	15	.22	3900	TDK #153	72
7.5	x4	33.3	133.3	16.2	.22	3900	TDK #153	84
8	x4	31.3	125	14	.27	4700	TDK #153	77
8.5	x4	29.4	117.7	11.8	.33	6800	TDK #153	67
9	x4	27.7	111.1	11	.39	6800	TDK #153	68
9.5	x4	26.3	105.3	10.5	.39	8200	TDK #153	65
10	x4	25	100	10	.47	8200	TDK #153	68

‡ full EMI filter part number : ACF 451832-153-T

† Under some operating conditions, the maximum PLL lock time may vary as much as 150% from the specified typical value. For example if the typical lock time is specified as 100 us, its maximum value may be as long as 250 us.

Note: For CLKMODE x1, the PLL is by-passed and all six external PLL components can be removed. For this case, the PLLV terminal has to be connected to a clean 2.5V supply and the PLLG and PLLF terminals should be tied together.

PRELIMINARY INFORMATION

Power Supply Sequencing

Since there are two supplies, an additional issue to consider by system designers is power supply sequencing. Ideally the two supplies (DVdd and CVdd) should be brought up simultaneously. However, in some cases this is not possible. If the two supplies cannot be brought up simultaneously, the DVdd should not exceed the CVdd supply during power-up by more than 2V and the CVdd should not exceed the DVdd supply by more than 0.5V. Both supplies should be linked together so that if one fails, the other one is shut down as well. To accomplish that, the “powergood” signal of one supply can be connected to the “inhibit” pin of the other.

thermal considerations

Like most high-performance processors, the 320C6201 can dissipate some thermal energy during normal operation. The high level of integration, high clock frequency and large on-chip memory arrays have an increased effect on the silicon junction temperature (Tj) compared with a lower performance DSP. To ensure proper operation and device reliability, the silicon junction temperature must not exceed maximum junction temperature (related to maximum case temperature Tc_{max}). Under operating conditions, system level thermal management is needed to assist with dissipating the heat away from the chip package. A passive heat sink provides a reliable and cost effective method for removing the excess heat. The size and shape of the heat sink depend on the operating conditions of the ‘320C6201 device and the characteristics of the system within which it operates.

‘320C6201 device operating conditions that can affect power dissipation:

- operating frequency
- chip manufacturing process type
- use of power-down (idle) modes
- amount of on-chip activity :

  number of functional units exercised every cycle
  frequency of the internal data memory accesses
  frequency of the internal program memory accesses
  rate at which the internal buses charged and discharged
  activity level of on-chip peripherals (DMAs, Serial Ports, etc.)
  rate at which data is being driven on and off the chip

system considerations for choosing a heat sink:

- air flow rate over the board housing the ‘320C6201
- ambient air temperature
- area / type of joint between package and the heat sink
- board design and layout

PRELIMINARY INFORMATION

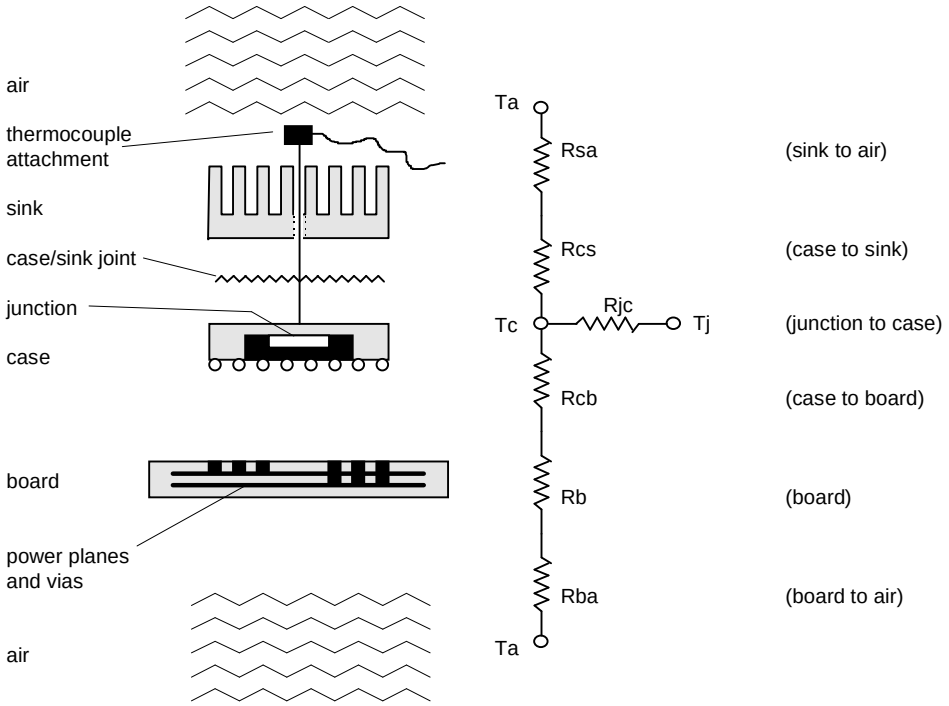
PRELIMINARY INFORMATION

thermal analysis and heat sink selection

Most of the current consumed by CMOS devices is Alternate Current (AC), which is charging and discharging the capacitances of internal nodes, pins and the external pin loads. The current flowing through the 320C6201 causes the temperature of the silicon die to rise. In order to maintain device reliability and proper operation, the junction temperature must not exceed the maximum specified junction temperature. As the heat is transferred from the die to the package, the case temperature of the package also rises. The junction to case thermal resistance RΘjc, together with the maximum junction temperature are parameters that determine the maximum case temperature Tc_{max}. Because of these factors, the specification of temperature is given in terms of Tc_{max} in the recommended operating conditions section of this document.

From the case, the heat typically flows to the surrounding air up through the heat sink and down through the pins and the board. The heat dissipation through the board material largely depends on the number of power and ground layers inside the board. The portion of the power that is dissipated by the heat sink must first propagate through the case-sink joint. The thermal resistance of case to sink joint can vary depending on the type of joint used such as thermal epoxy or double-sided adhesive pads. The rate at which the heat is transferred from the sink to the ambient air, to a large degree depends on the velocity of the air at the heat sink. The heat flow from the sink rises with the speed of the airflow. The objective of the examples in this section is to present a method for first order approximation of the size of the heat sink needed to keep the maximum case temperature from exceeding the Tc_{max} during maximum system operating conditions. Following heat sink installation, the actual case temperature should be measured to verify that it doesn't exceed theTc_{max} value.

Heat transfer analysis can be a complex task depending on the degree of accuracy required in modeling of system components. A number of computational fluid dynamics and heat transfer tools are available to provide highly accurate results. Experimental methods could be used as well for analyzing heat flow. This document uses a simplified approach to select a heat sink that matches a particular operating environment. The driving parameter in determining the heat flow is the maximum case temperature which must stay below Tc_{max} at all times during device operation. The system parameters that have first order effect on the case temperature are the average device power dissipation, ambient air temperature and air approach velocity. The choice of the heat sink largely depends on those factors as showed in the following examples. Other factors that may affect the heat dissipation include board design/materials and case to sink attachment method. The relatively long Time Constant of the case/sink combination (around 2 minutes) can effectively smooth out any power peaks that may occur. To validate proper operation of the heat sink, a small hole should be drilled in the center of the sink in order to place a miniature thermocouple directly on the case (center top surface) for measuring the actual case temperature under system's maximum expected operating conditions.



Thermal model used for heat flow analysis

PRELIMINARY INFORMATION

heat sink selection example 1

- Specify operating conditions (this system reflects a typical PC operating environment using a production version of the 320C6201 with high performance internal memory arrays)

Pa = 4.2 W	average power dissipated by the case
Ta_{max} = 40 ºC	ambient air temperature
Va_{min} = 85 LFM	air approach velocity (linear feet per minute)
h_{max} = 9mm	height limit for the heat sink (system requirement)
RΘcs = 0.5 ºC/W	case to sink thermal resistance (using thermal epoxy)
Tc_{max} = 90 ºC	case temperature

- Estimate the total power that needs to be dissipated by the heat sink, Ps

Ps = Pa -1W (assume 1W dissipation through the board)

Ps = 4.2 - 1 = 3.2 W

- Compute the maximum heat sink to air thermal resistance RΘsa that will maintain the case temperature below Tc_{max} for the operating conditions specified above.

RΘsa + RΘcs = (Tc -Ta) / Ps

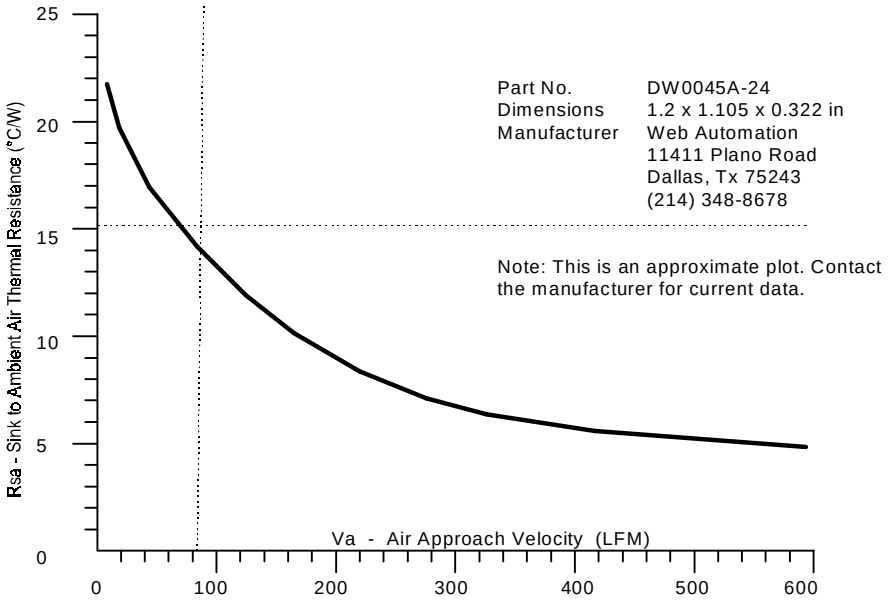
RΘsa = {(Tc -Ta) / Ps} - RΘcs

RΘsa = {(90 - 40) / 3.2} - 0.5

RΘsa = 15.1 ºC/W

- Choose the heat sink based on the computed maximum sink to air resistance RΘsa and the minimum air approach velocity inside the enclosure. The heat sink performance plot below verifies that at 85 LFM minimum air velocity, the sink to air thermal resistance will indeed stay at or below the Rsa value of 15.1 ºC/W that is required to maintain the case temperature below Tc_{max} for the listed operating conditions. Actual experimental measurement of the case temperature should be performed next to verify heat sink performance.

PRELIMINARY INFORMATION



Heat Sink Performance Plot

PRELIMINARY INFORMATION

PRELIMINARY INFORMATION

heat sink selection example 2

- Specify operating conditions (this example uses a pre-production version of the 320C6201)

Pa = 6.9 W	average power dissipated by the case
Ta_{max} = 55 ºC	ambient air temperature
Va_{min} = 140 LFM	air approach velocity (linear feet per minute)
h_{max} = 17mm	height limit for the heat sink (system requirement)
RΘcs = 0.2 ºC/W	case to sink thermal resistance (using thermal grease)
Tc_{max} = 90 ºC	case temperature

- Estimate the total power that needs to be dissipated by the heat sink, Ps

Ps = Pa - 2W (assume 2W dissipation through the board)

Ps = 6.9 - 2 = 4.9 W

- Compute the maximum heat sink to air thermal resistance RΘsa that will maintain the case temperature below Tc_{max} for the operating conditions specified above.

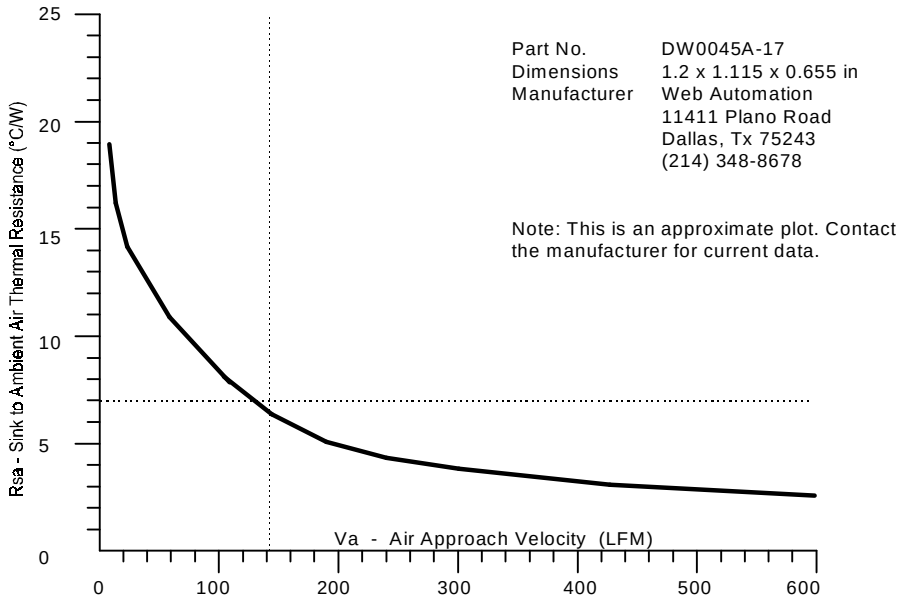
RΘsa + RΘcs = (Tc -Ta) / Ps

RΘsa = {(Tc -Ta) / Ps} - RΘcs

RΘsa = {(90 - 55) / 4.9} - 0.2

RΘsa = 6.9 ºC/W

- Choose the heat sink based on the computed sink to air resistance RΘsa and the minimum air approach velocity inside the enclosure. The heat sink performance plot below verifies that at 140 LFM minimum air velocity, the sink to air thermal resistance will indeed stay at or below the Rsa value of 6.9 ºC/W that is required to maintain the case temperature below Tc_{max} for the listed operating conditions. Actual experimental measurement of the case temperature should be performed next to verify heat sink performance.



Heat Sink Performance Plot

PRELIMINARY INFORMATION

Note: The timing parameters will be disclosed in September 1997.

PRELIMINARY INFORMATION

absolute maximum ratings over operating free–air temperature range (unless otherwise noted)†

Supply voltage range, CV_{DD} (see Note 1) . . . . . -0.3 to 3V
Supply voltage range, DV_{DD} (see Note 1) . . . . . -0.3 to 4V
Input voltage range . . . . . -0.3 to 4V
Output voltage range . . . . . -0.3 to 4V
Operating case temperature range, T_C . . . . . 0°C to 90°C
Storage temperature range, T_{stg} . . . . . -55°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE1: All voltage values are with respect to $V_{SS.}$

TMX320C6201 recommended operating conditions

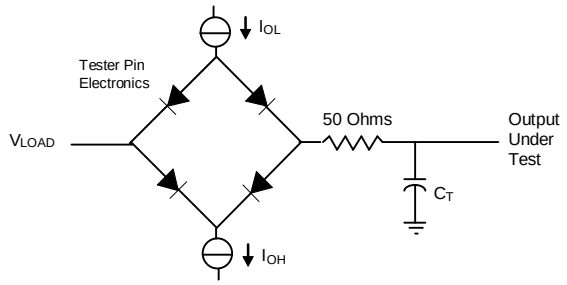
PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
CV_{DD}	Supply voltage		2.38	2.50	2.62	V
DV_{DD}	Supply voltage		3.14	3.30	3.46	V
V_{SS}	Supply voltage		0	0	0	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current				-12	mA
I_{OL}	Low-level output current				12	mA
T_C	Case temperature		0		90	° C

TMX320C6201 electrical characteristics over recommended ranges of supply voltage and operating case temperature

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	DV_{DD} = MIN	I_{OH}= MAX	2.4			V
V_{OL}	Low-level output voltage	DV_{DD} = MIN	I_{OL}= MAX			0.5	V
I_I	Input current	V_I = V_{SS} to DV_{DD}				±10	uA
I_{OZ}	Off-state output current	V_O = DV_{DD} or 0V				±10	uA
I_{DD2V}	Supply current	CV_{DD} = MAX	200 MHz		1.8 †	TBD	A
I_{DD3V}	Supply current	DV_{DD} = MAX	200 MHz		258	TBD	mA
C_I	Input capacitance					10	pF
C_O	Output capacitance					10	pF

† Note: I_{DD2V} parameter will be smaller in future revisions of 320C6201

parameter measurement information

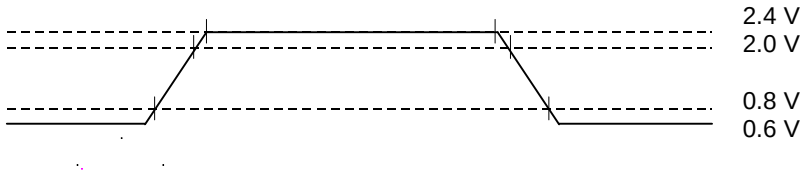


TTL-Level Outputs

Where:	I_{OL}	=	12 mA (all outputs)
	I_{OH}	=	-12 mA (all outputs)
	V_{LOAD}	=	2.1 V
	C_T	=	30 pF typical distributed load circuit capacitance

signal transition levels

TTL-output levels are driven to a minimum logic-high level of 2.4 V and to a maximum logic-low level of 0.6 V Figure 3.1 shows the TTL-level outputs.

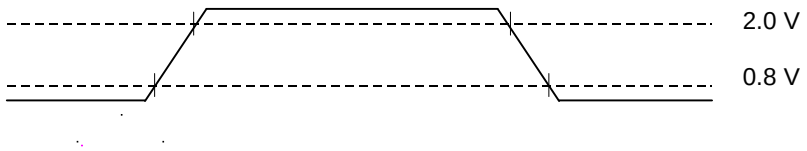


TTL-Level Outputs

TTL-compatible output transition times are specified as follows:

- For a high-to-low transition, the level at which the output is said to be no longer high is 2 V, and the level at which the output is said to be low is 0.8 V.
- For a low-to-high transition, the level at which the output is said to be no longer low is 0.8 V, and the level at which the output is said to be high is 2 V.

Figure 3.2 shows the TTL-level inputs.



TTL-Level Inputs

TTL-compatible input transition times are specified as follows:

- For a high-to-low transition on an input signal, the level at which the input is said to be no longer high is 2 V, and the level at which the input is said to be low is 0.8 V.
- For a low-to-high transition on an input signal, the level at which the input is said to be no longer low is 0.8 V, and the level at which the input is said to be high is 2 V.

PRELIMINARY INFORMATION

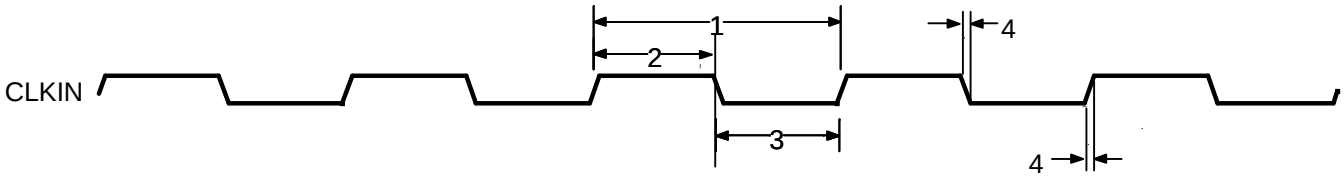
Note: The timing parameters will be disclosed in September 1997.

PRELIMINARY INFORMATION

input and output clocks

CLKIN timing parameters

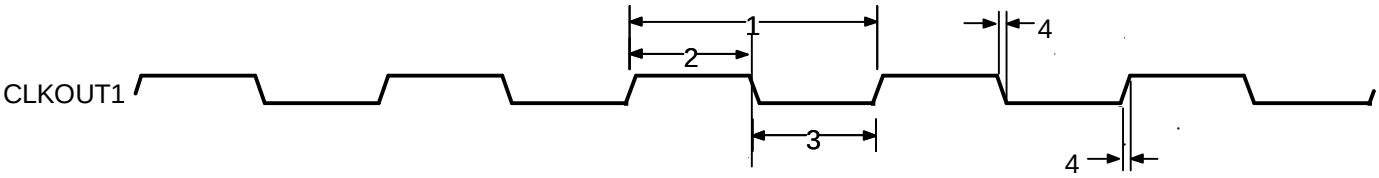
NO			CLKMODE = x4		CLKMODE = x2		CLKMODE = x1		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
1	t_c(CLKIN)	Period of CLKIN							ns
2	t_w(CLKIN)	Pulse duration of CLKIN high							ns
3	t_w(CLKIN)	Pulse duration of CLKIN low							ns
4	t_T(CLKIN)	Transition time of CLKIN							ns



CLKIN Timing

CLKOUT1 timing parameters

NO			MIN	TYP	MAX	UNIT
1	t_c(CKO1)	Period of CLKOUT1	†			ns
2	t_w(CKO1)	Pulse duration of CLKOUT1 high				ns
3	t_w(CKO1)	Pulse duration of CLKOUT1 low				ns
4	t_T(CKO1)	Transition time of CLKOUT1				ns

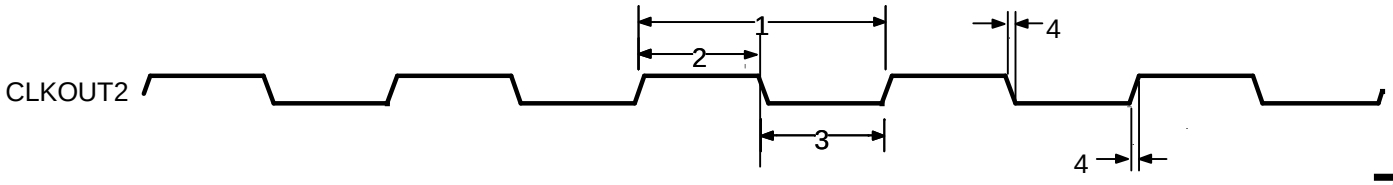


CLKOUT1 Timing

† This parameter is a functional minimum and is not tested

CLKOUT2 timing parameters

NO			MIN	MAX	UNIT
1	t_c(CKO2)	Period of CLKOUT2			ns
2	t_w(CKO2)	Pulse duration of CLKOUT2 high			ns
3	t_w(CKO2)	Pulse duration of CLKOUT2 low			ns
4	t_T(CKO2)	Transition time of CLKOUT2			ns



CLKOUT2 Timing

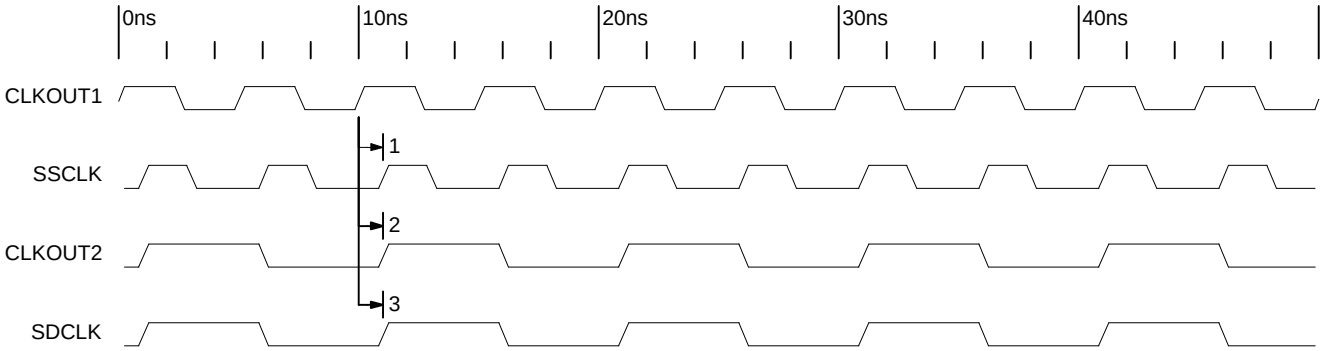
SDCLK, SSCLK timing parameters

SDCLK timing parameters are the same as CLKOUT2 parameters

SSCLK timing parameters are the same as CLKOUT1 or CLKOUT2 parameters, depending on SSCLK configuration

relation of SDCLK, SSCLK and CLKOUT2 to CLKOUT1

NO			MIN	MAX	UNIT
1	t_d(CKO1-CKOUT2)	Delay from CLKOUT1 edge to CLKOUT2 edge			ns
2	t_D(CKO1-SSCLK)	Delay from CLKOUT1 edge to SSCLK edge			ns
3	t_D(CKO1-SDCLK)	Delay from CLKOUT1 edge to SDCLK edge			ns



Relation of CLKOUT2, SDCLK and SSCLK to CLKOUT1

PRELIMINARY INFORMATION

Note: The timing parameters will be disclosed in September 1997.

asynchronous memory timing

timing requirements for Asynchronous Memory cycles

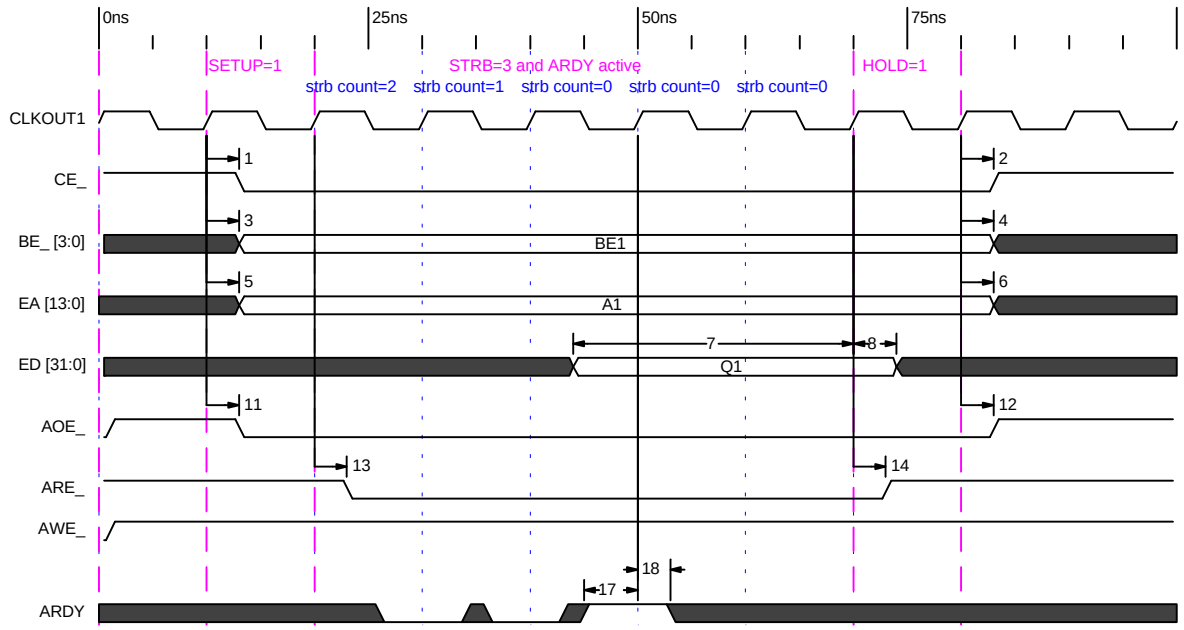
NO			MIN	MAX	UNIT
7	t_{su}(D-CKH)	Setup time, read D before CLKOUT1 high			ns
8	t_h(CKH-D)	Hold time, read D valid after CLKOUT1 high			ns
17	t_{su}(ARDY-CKH)	Setup time, ARDY before CLKOUT1 high			ns
18	t_h(CKH-ARDY)	Hold time, ARDY valid after CLKOUT1 high			ns

switching characteristics for Asynchronous Memory cycles

NO			MIN	MAX	UNIT
1	t_d(CKH-CE)	Delay time, CLKOUT1 high to CE_ low			ns
2	t_h(CKH-CE)	Hold time, CLKOUT1 high to CE_ low			ns
3	t_d(CKH-BE)	Delay time, CLKOUT1 high to BE_ valid			ns
4	t_h(CKH-BE)	Hold time, CLKOUT1 high to BE_ valid			ns
5	t_d(CKH-A)	Delay time, CLKOUT1 high to EA valid			ns
6	t_h(CKH-A)	Hold time, CLKOUT1 high to EA valid			ns
9	t_d(CKH-D)	Delay time, CLKOUT1 high to ED valid			ns
10	t_h(CKH-D)	Hold time, CLKOUT1 high to ED valid			ns
11	t_d(CKH-OE)	Delay time, CLKOUT1 high to AOE_ low			ns
12	t_h(CKH-OE)	Hold time, CLKOUT1 high to AOE_ low			ns
13	t_d(CKH-RE)	Delay time, CLKOUT1 high to ARE_ low			ns
14	t_h(CKH-RE)	Hold time, CLKOUT1 high to ARE_ low			ns
15	t_d(CKH-WE)	Delay time, CLKOUT1 high to AWE_ low			ns
16	t_h(CKH-WE)	Hold time, CLKOUT1 high to AWE_ low			ns

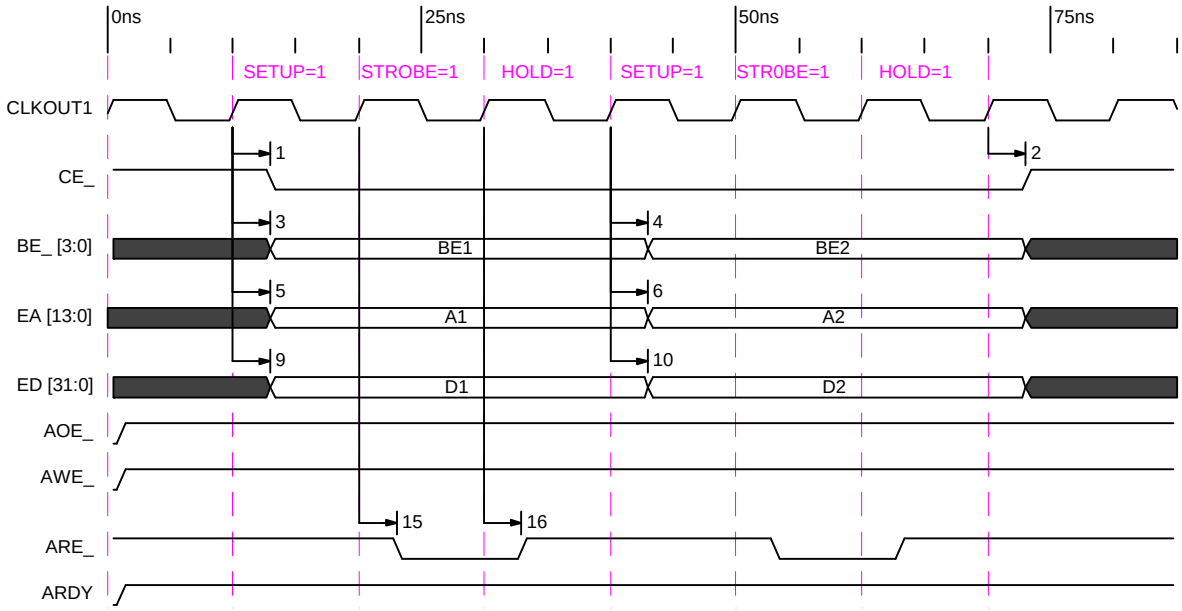
† Values specified by design and not tested

PRELIMINARY INFORMATION



ASYNCHRONOUS MEMORY READ TIMING WITH INACTIVE/ACTIVE ARDY

Note: If during a rising edge of CLKOUT1 the STROBE count is 1 or 0, and the ARDY signal was active during the previous edge, the next edge of CLKOUT1 will end the ARE_ or AWE_ strobes. Otherwise the read or write cycle will be extended by at least one more CLKOUT1 period.



ASYNCHRONOUS MEMORY WRITE TIMING WITH ARDY TIED HIGH

Note: The minimum strobe width value is 3 if inactive (low) ARDY is used to extend the asynchronous read or write cycles (see the read timing diagram). Otherwise, if the ARDY is always active (high), the minimum strobe width is 1(see the write timing diagram).

PRELIMINARY INFORMATION

Note: The timing parameters will be disclosed in September 1997.

sync-burst memory timing

timing requirements for Synchronous Burst Memory cycles

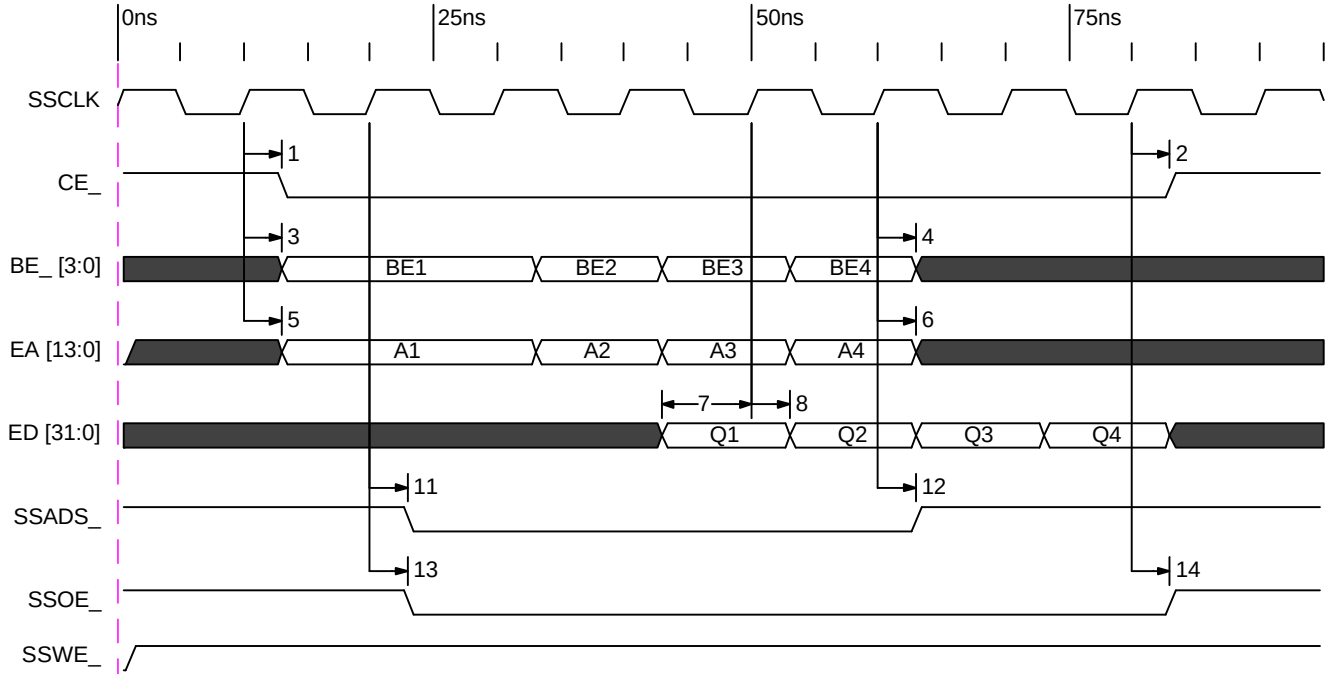
NO			MIN	MAX	UNIT
7	t_{su}(D-CKH)	Setup time, read D before CLKOUT1 high			ns
8	t_h(CKH-D)	Hold time, read D valid after CLKOUT1 high			ns

switching characteristics for Synchronous Burst SRAM (SBSRAM) cycles

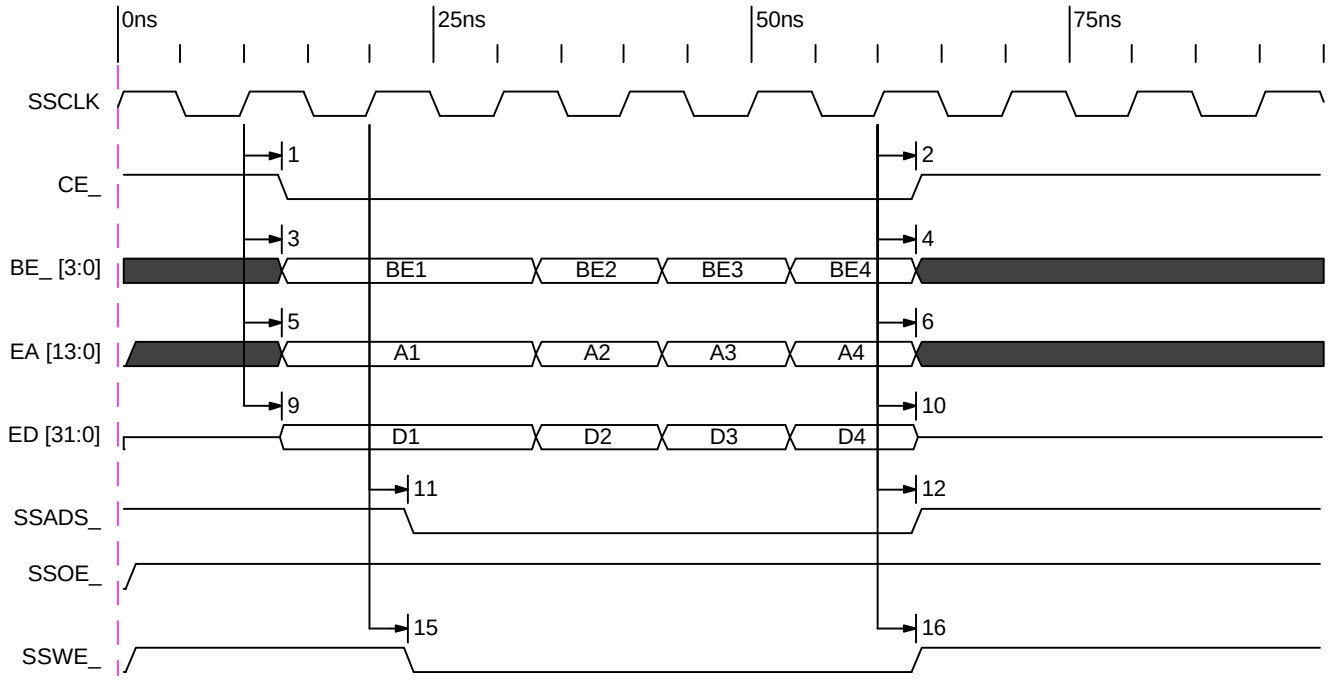
NO			MIN	MAX	UNIT
1	t_d(CKH-CE)	Delay time, CLKOUT1 high to CE_ low			ns
2	t_h(CKH-CE)	Hold time, CLKOUT1 high to CE_ low			ns
3	t_d(CKH-BE)	Delay time, CLKOUT1 high to BE_ valid			ns
4	t_h(CKH-BE)	Hold time, CLKOUT1 high to BE_ valid			ns
5	t_d(CKH-A)	Delay time, CLKOUT1 high to EA valid			ns
6	t_h(CKH-A)	Hold time, CLKOUT1 high to EA valid			ns
9	t_d(CKH-D)	Delay time, CLKOUT1 high to ED valid			ns
10	t_h(CKH-D)	Hold time, CLKOUT1 high to ED valid			ns
11	t_d(CKH-ADS)	Delay time, CLKOUT1 high to SSADS_ low			ns
12	t_h(CKH-ADS)	Hold time, CLKOUT1 high to SSADS_ low			ns
13	t_d(CKH-SSOE)	Delay time, CLKOUT1 high to SSOE_ low			ns
14	t_h(CKH-SSOE)	Hold time, CLKOUT1 high to SSOE_ low			ns
15	t_d(CKH-SSWE)	Delay time, CLKOUT1 high to SSWE_ low			ns
16	t_h(CKH-SSWE)	Hold time, CLKOUT1 high to SSWE_ low			ns

† Values specified by design and not tested

PRELIMINARY INFORMATION



SBSRAM READ TIMING



SBSRAM WRITE TIMING

PRELIMINARY INFORMATION

Note: The timing parameters will be disclosed in September 1997.

synchronous DRAM timing

timing requirements for Synchronous DRAM (SDRAM) cycles

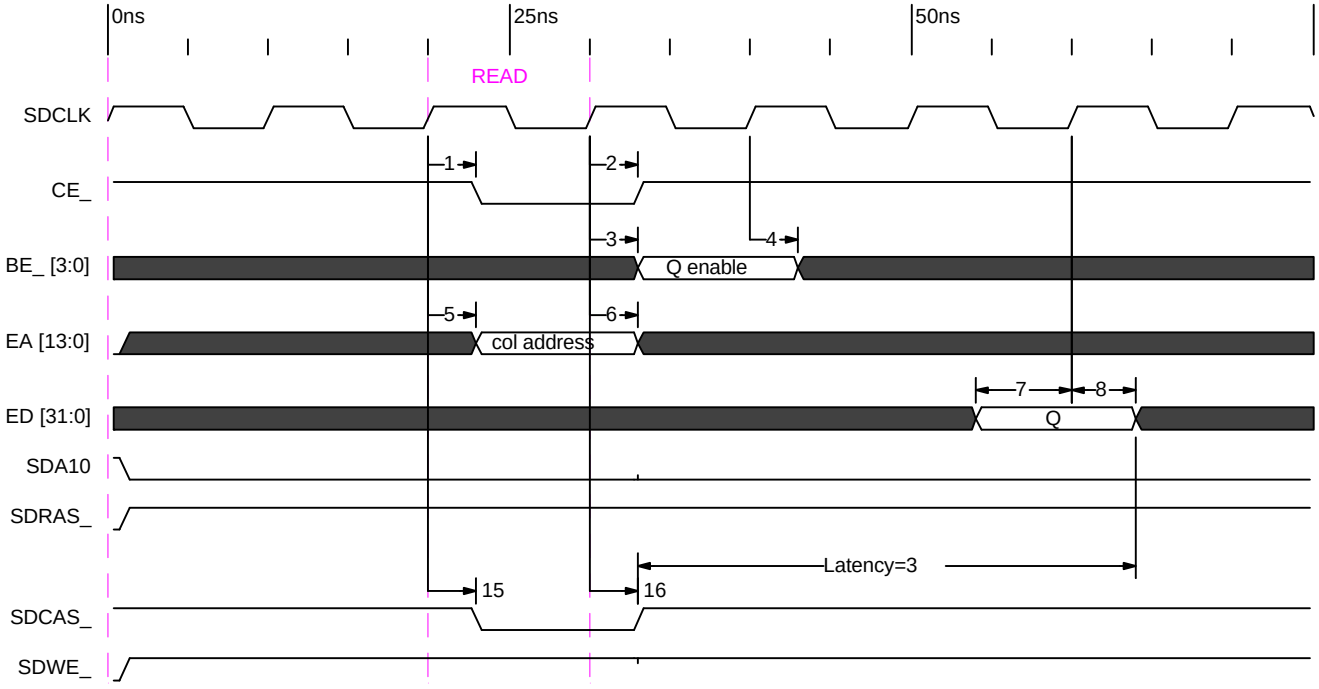
NO			MIN	MAX	UNIT
7	t_{su}(D-CKH)	Setup time, read D before CLKOUT1 high			ns
8	t_h(CKH-D)	Hold time, read D valid after CLKOUT1 high			ns

PRELIMINARY INFORMATION

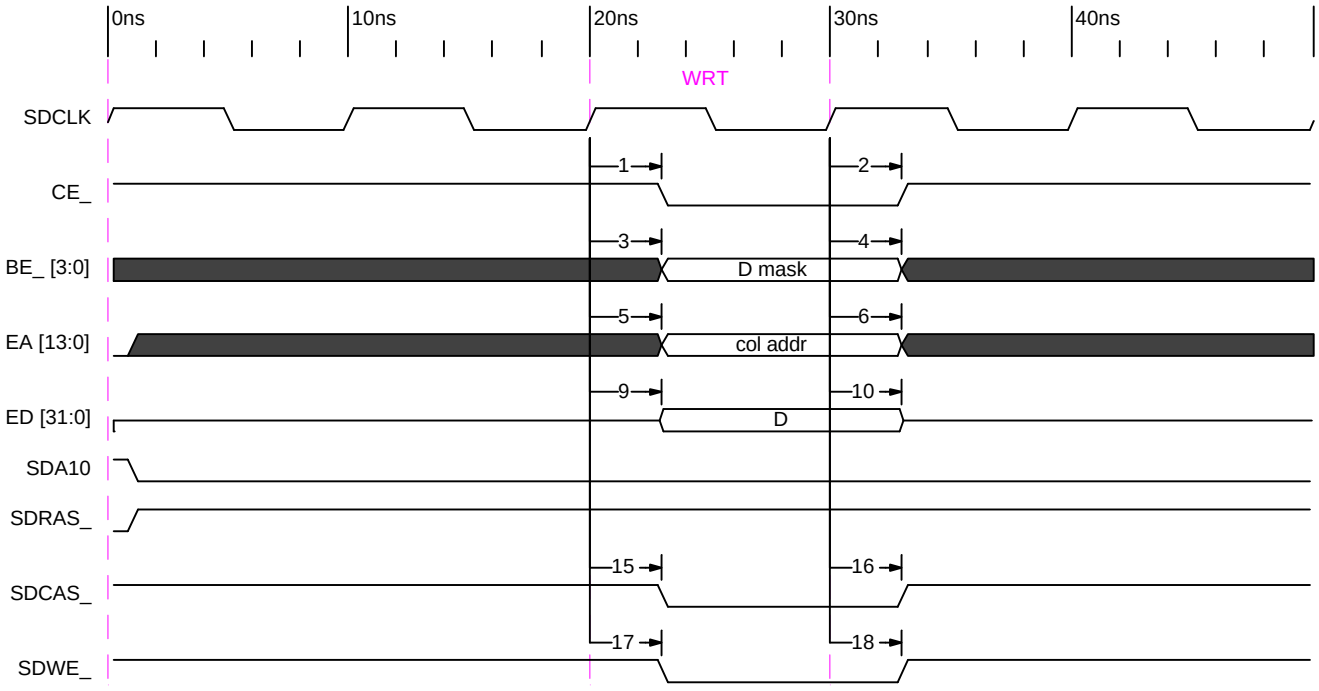
switching characteristics for Synchronous DRAM (SDRAM) cycles

NO			MIN	MAX	UNIT
1	t_d(CKH-CE)	Delay time, CLKOUT1 high to CE_ low			ns
2	t_h(CKH-CE)	Hold time, CLKOUT1 high to CE_ low			ns
3	t_d(CKH-BE)	Delay time, CLKOUT1 high to BE_ valid			ns
4	t_h(CKH-BE)	Hold time, CLKOUT1 high to BE_ valid			ns
5	t_d(CKH-A)	Delay time, CLKOUT1 high to EA valid			ns
6	t_h(CKH-A)	Hold time, CLKOUT1 high to EA valid			ns
9	t_d(CKH-D)	Delay time, CLKOUT1 high to ED valid			ns
10	t_h(CKH-D)	Hold time, CLKOUT1 high to ED valid			ns
11	t_d(CKH-SDA10)	Delay time, CLKOUT1 high to SDA10_ valid			ns
12	t_h(CKH-SDA10)	Hold time, CLKOUT1 high to SDA10_ valid			ns
13	t_d(CKH-SDRAS)	Delay time, CLKOUT1 high to SDRAS_ low			ns
14	t_h(CKH-SDRAS)	Hold time, CLKOUT1 high to SDRAS_ low			ns
15	t_d(CKH-SDCAS)	Delay time, CLKOUT1 high to SDCAS_ low			ns
16	t_h(CKH-SDCAS)	Hold time, CLKOUT1 high to SDCAS_ low			ns
17	t_d(CKH-SDWE)	Delay time, CLKOUT1 high to SDWE_ low			ns
18	t_h(CKH-SDWE)	Hold time, CLKOUT1 high to SDWE_ low			ns

† Values specified by design and not tested



SDRAM READ COMMAND

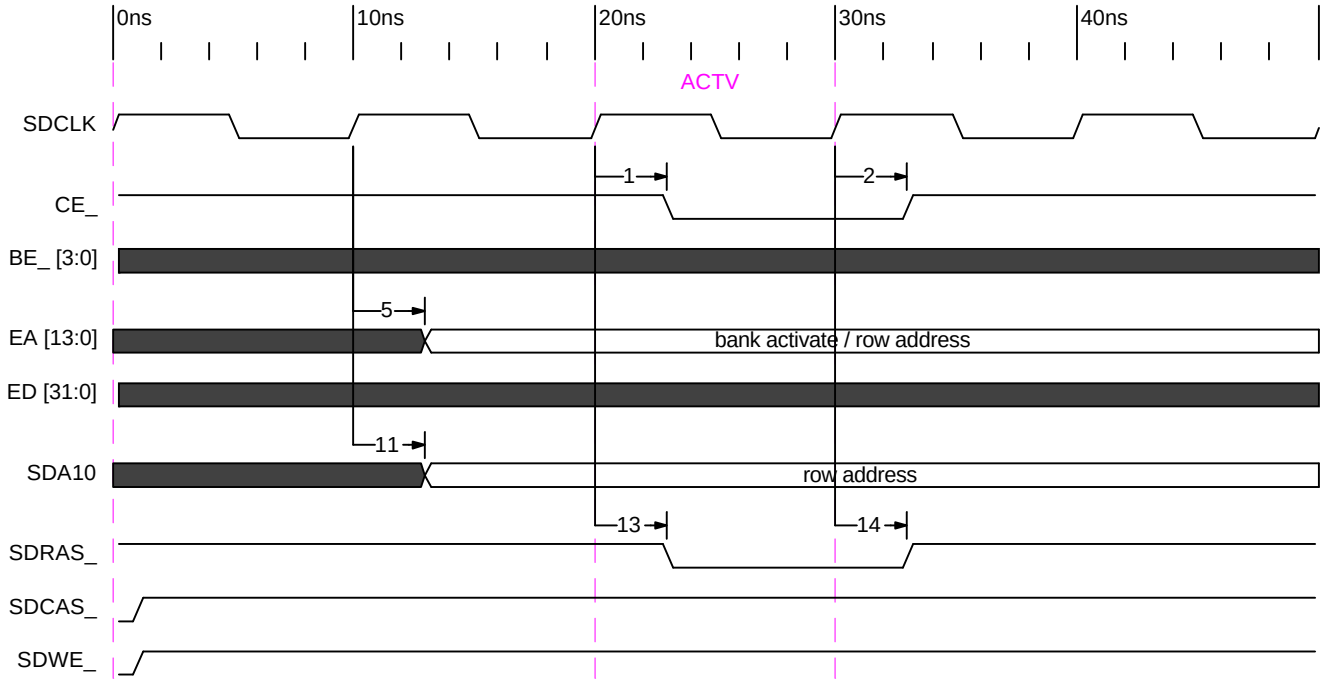


SDRAM WRT COMMAND

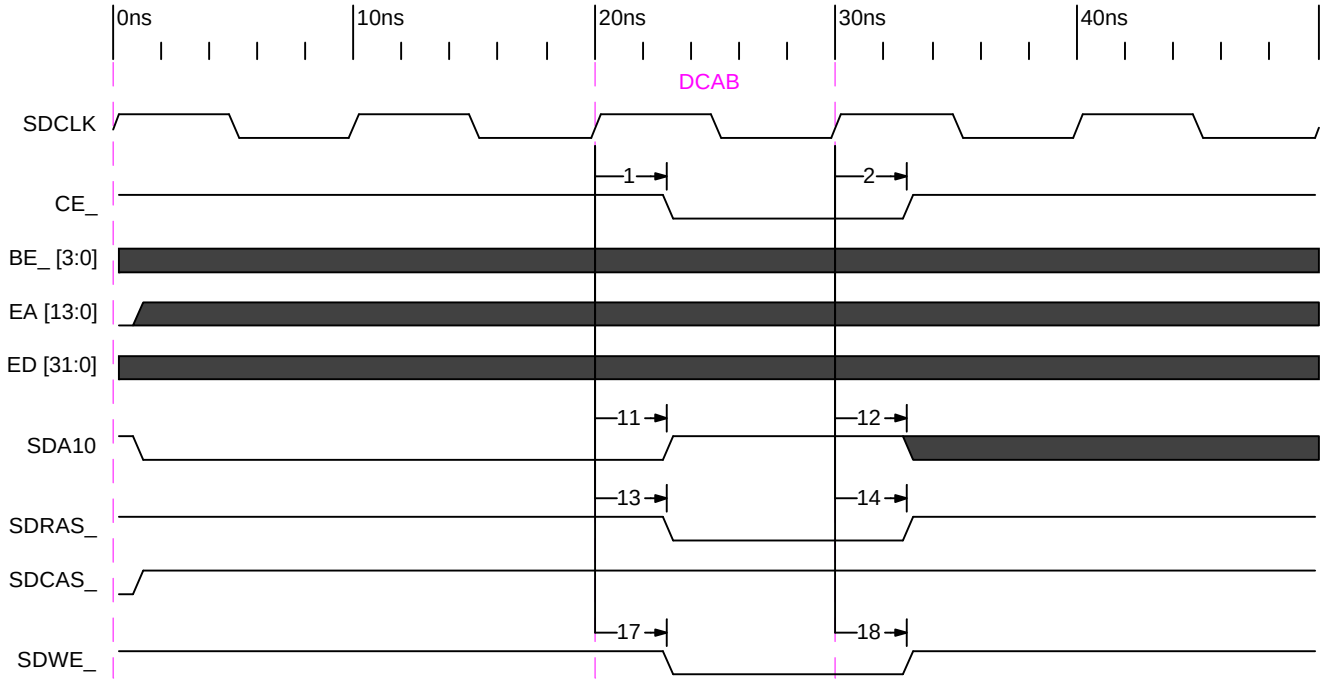
PRELIMINARY INFORMATION

Note: The timing parameters will be disclosed in September 1997.

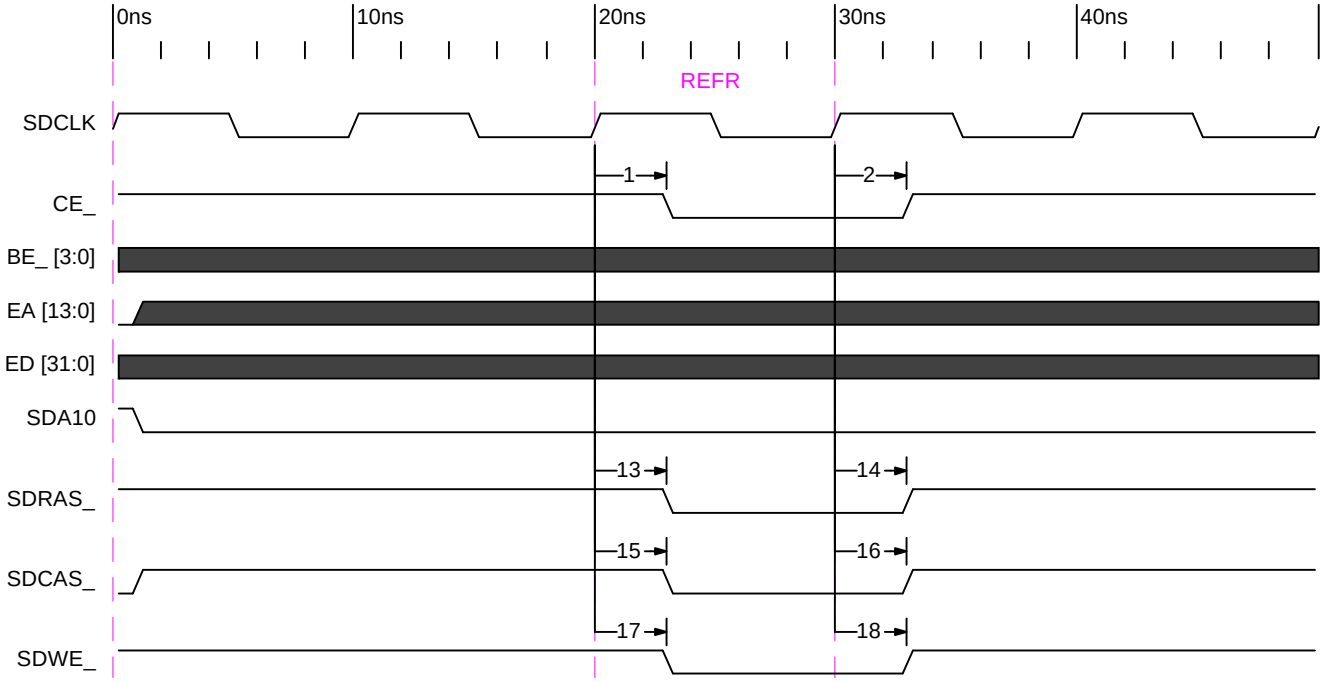
PRELIMINARY INFORMATION



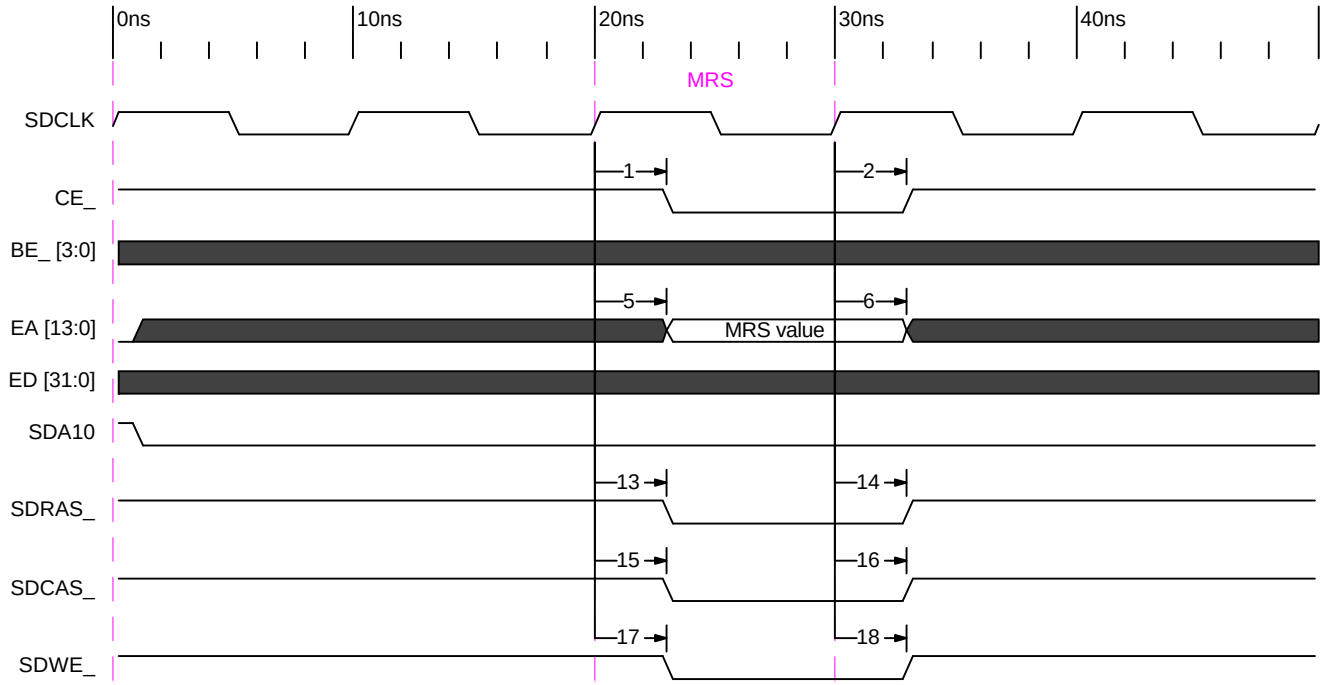
SDRAM ACTV COMMAND



SDRAM DCAB COMMAND



SDRAM REFR COMMAND

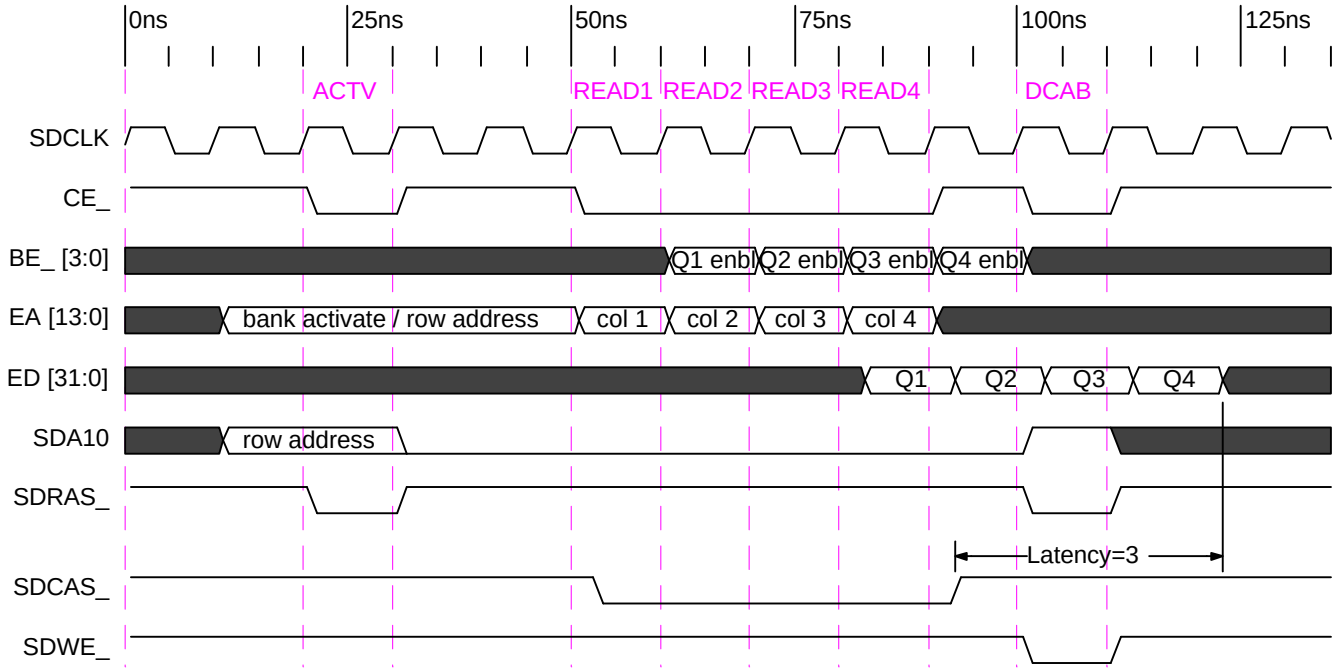


SDRAM MRS COMMAND

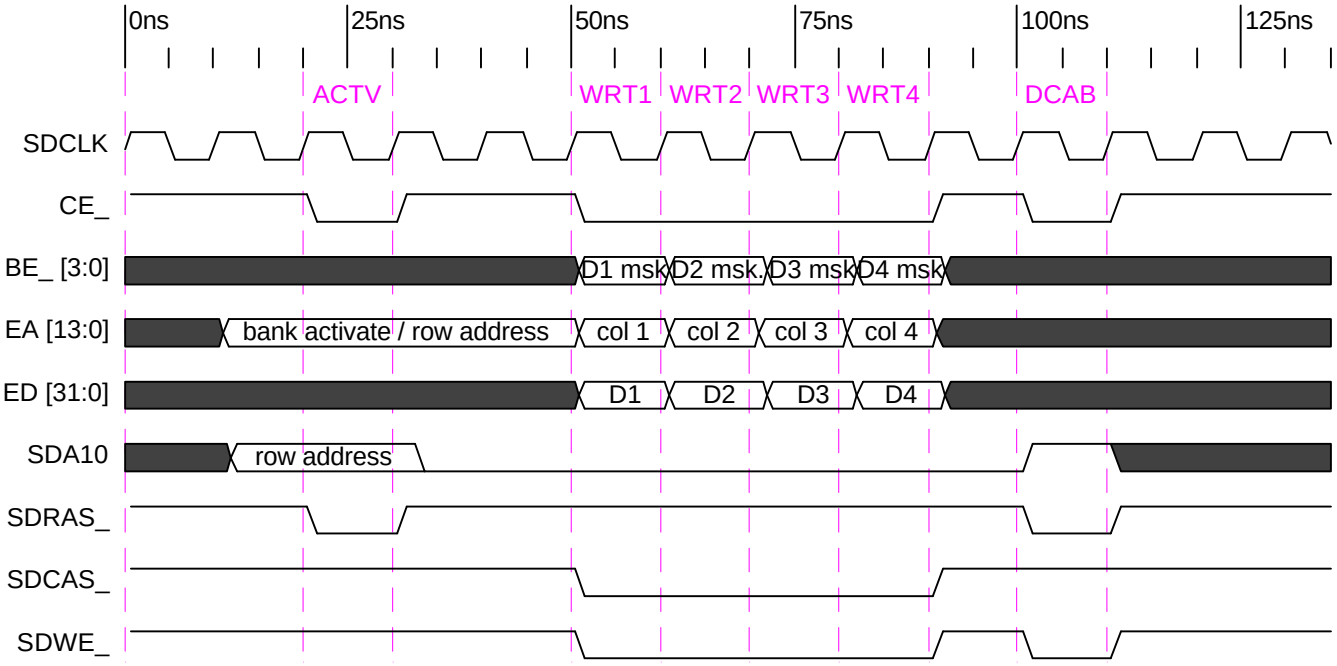
PRELIMINARY INFORMATION

Note: The timing parameters will be disclosed in September 1997.

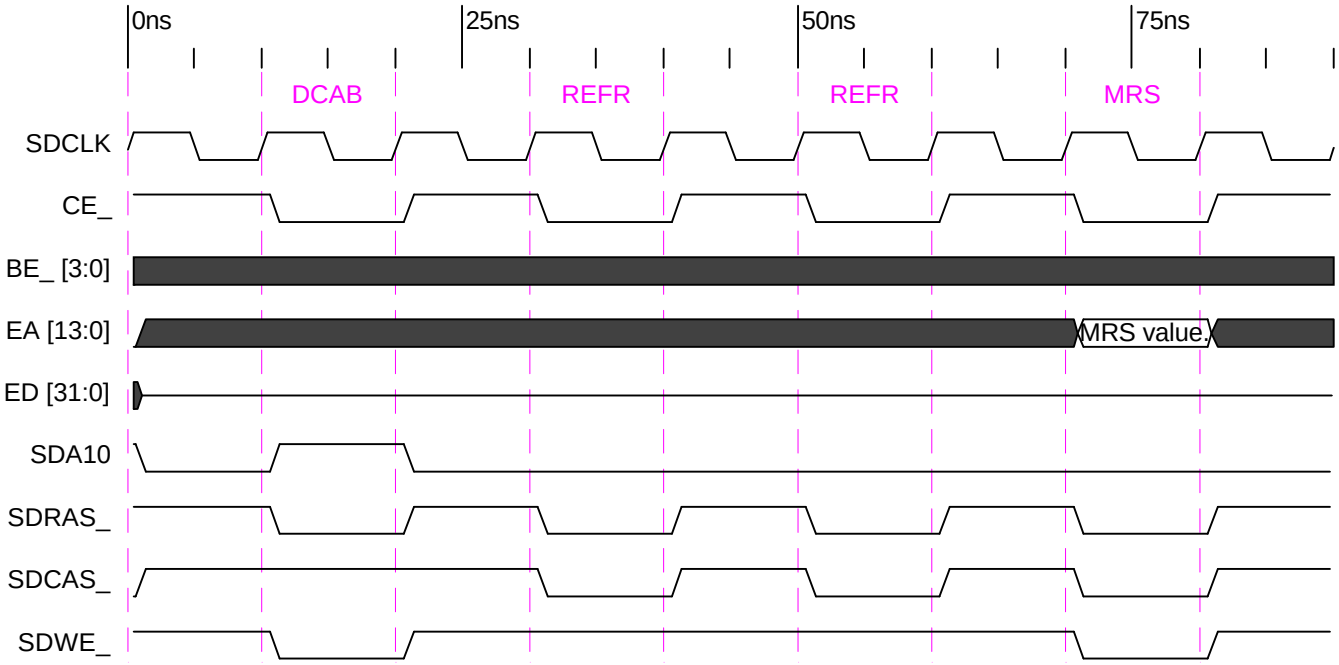
PRELIMINARY INFORMATION



SDRAM READ SEQUENCE



SDRAM WRITE SEQUENCE



SDRAM POWER-UP TIMING

PRELIMINARY INFORMATION

Note: The timing parameters will be disclosed in September 1997.

HOLD / HOLDA timing

timing requirements for the Hold / Hold Acknowledge cycles

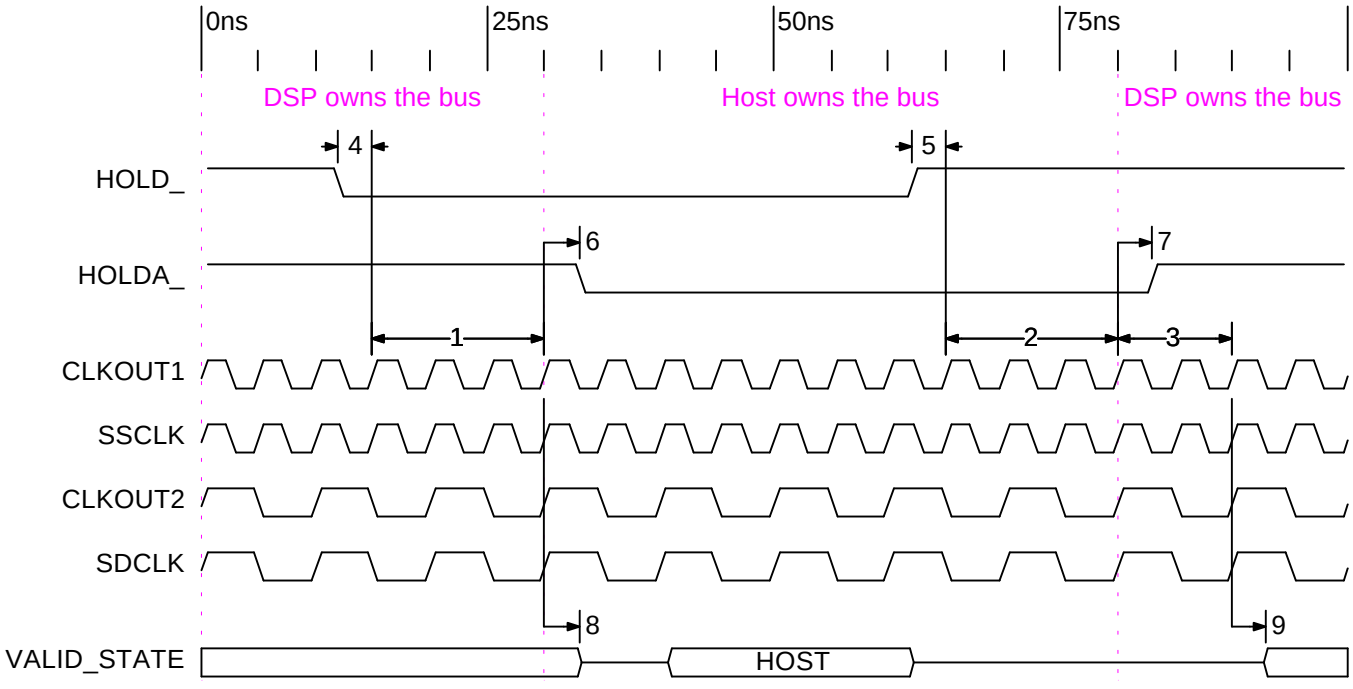
NO			MIN	MAX	UNIT
4	t_{su}(CKH-HOLDH)	Setup time, HOLD_ low before CLKOUT1 high			ns
5	t_{su}(CKH-HOLDL)	Setup time, HOLD_ high before CLKOUT1 high			ns

switching characteristics for the Hold / Hold Acknowledge cycles

NO			MIN	MAX	UNIT
1	t_r(HOLDAL)	Response time, HOLD_ low to HOLDA_ low			cycles
2	t_r(HOLDAH)	Response time, HOLD_ high to HOLDA_ high			cycles
3	t_r(BUS)	Delay time, HOLDA_ high to EMIF bus driven			cycles
6	t_d(CKH-HOLDAL)	Delay time, CLKOUT1 high to HOLDA_ low			ns
7	t_d(CKH-HOLDAH)	Delay time, CLKOUT1 high to HOLDA_ high			ns
8	t_d(CKH-TRI)	Delay time, CLKOUT1 high to EMIF tri-stated			ns
9	t_d(CKH-DRV)	Delay time, CLKOUT1 high to EMIF driven with valid state			ns

‡ Values derived from characterization data and not tested

PRELIMINARY INFORMATION



HOLD_/HOLDA_ TIMING

VALID_STATE = EA[21:2]
ED[31:0]C
E[3:0]
BE[3:0]

ARE_
AOE_
AWE_
ARDY_

SSADS_
SSOE_
SSWE_

SDA10
SDRAS_
SDCAS_
SDWE_

PRELIMINARY INFORMATION

Note: The timing parameters will be disclosed in September 1997.

reset timing

timing requirements for reset

NO			MIN	MAX	UNIT
4	t_{su}(CKH-HOLDH)	Setup time, HOLD_ low before CLKOUT1 high			ns
5	t_{su}(CKH-HOLDL)	Setup time, HOLD_ high before CLKOUT1 high			ns

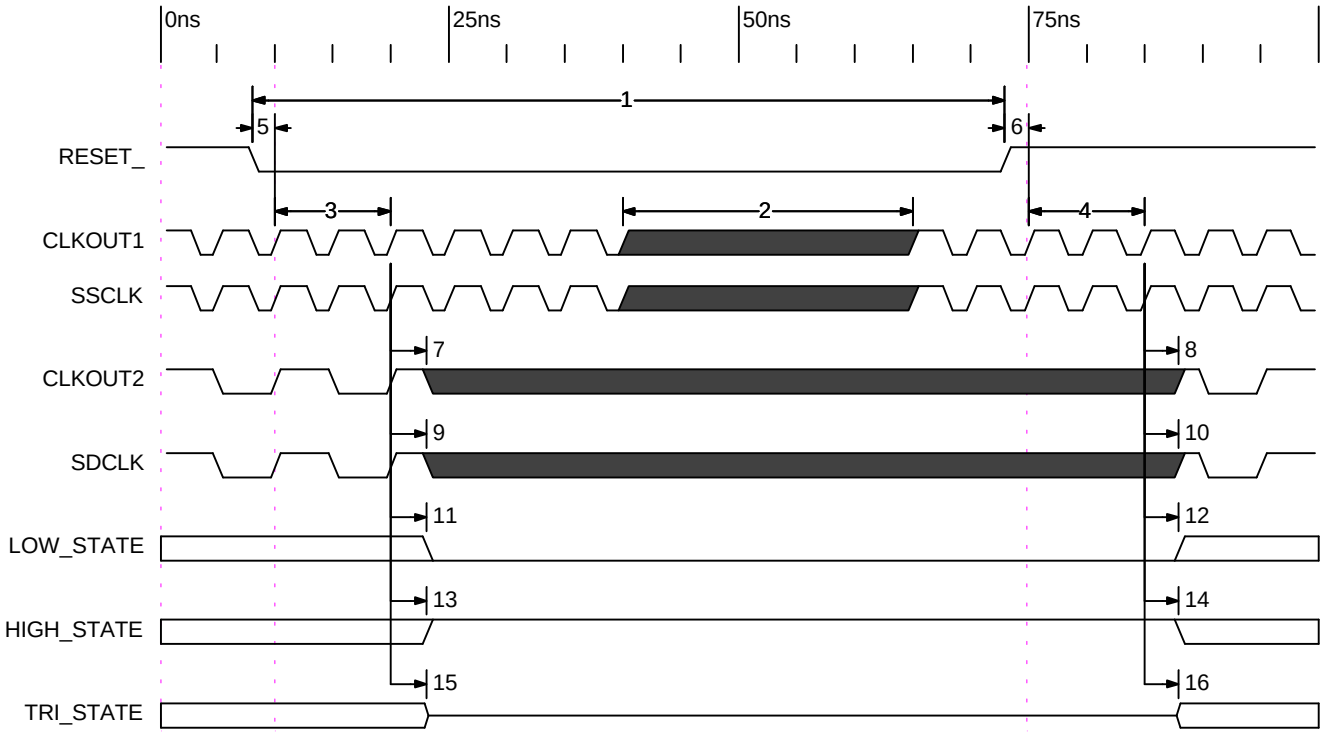
PRELIMINARY INFORMATION

switching characteristics during reset

NO			MIN	MAX	UNIT
5	t_{su}(RESETL-CKH)	Setup time, RESET_ low before CLKOUT1 high			ns
6	t_{su}(RESETH-CKH)	Setup time, RESET_ high before CLKOUT1 high			ns
1	t_w(RESET)	Width of the RESET_ pulse (PLL stable)			cycles
2	t_w(PLL)	Width of the RESET_ pulse (PLL needs to sync up)			us
3	t_r (RESETON)	Response time, reset takes effect after RESET_ pulse asserted			cycles
4	t_r (RESETOFF)	Response time, out of reset after RESET_ pulse deasserted			cycles
7	t_h(CKH-CK2)	Hold time, CLKOUT1 high to CLKOUT2 valid			ns
8	t_d(CKH-CK2)	Delay time, CLKOUT1 high to CLKOUT2 valid			ns
9	t_h(CKH-SDCLK)	Hold time, CLKOUT1 high to SDCLK valid			ns
10	t_d(CKH-SDCLK)	Delay time, CLKOUT1 high to SDCLK valid			ns
11	t_h(CKH-LOW)	Hold time, CLKOUT1 high to LOW signal group valid			ns
12	t_d(CKH-LOW)	Delay time, CLKOUT1 high to LOW signal group valid			ns
13	t_h(CKH-HIGH)	Hold time, CLKOUT1 high to HIGH signal group valid			ns
14	t_d(CKH-HIGH)	Delay time, CLKOUT1 high to HIGH signal group valid			ns
15	t_h(CKH-TRI)	Hold time, CLKOUT1 high to TRI signal group valid			ns
16	t_d(CKH-TRI)	Delay time, CLKOUT1 high to TRI signal group valid			ns

‡ Values derived from characterization data and not tested

† The RESET_ signal is not connected internally to the clock PLL circuit. The PLL, however, may need up to 250 us to stabilize following device power-up or after PLL configuration has been changed. During that time, RESET_ must be asserted to ensure proper device operation. See the PLL section for PLL lock times.



RESET TIMING

LOW signal group = IACK, INUM[3:0], DMAC[3:0], PD_

HIGH signal group = HRDY_, HINT_

TRI signal group = EA[21:2], ED[31:0], CE[3:0], BE[3:0], ARE_, AOE_, AWE_, ARDY_, SSADS_, SSOE_, SSWE_, SDA10, SDRAS_, SDCAS_, SDWE_, HD[15:0], TIM0, TIM1, CLKX0, CLKX1, FSX0, FSX1, DX0 DX1, CLKR0, CLKR1, FSR0, FSR1

Outputs not affected by Reset = HOLDA_

PRELIMINARY INFORMATION

Note: The timing parameters will be disclosed in September 1997.

external interrupt/reset timing

timing requirements for interrupt responce cycles

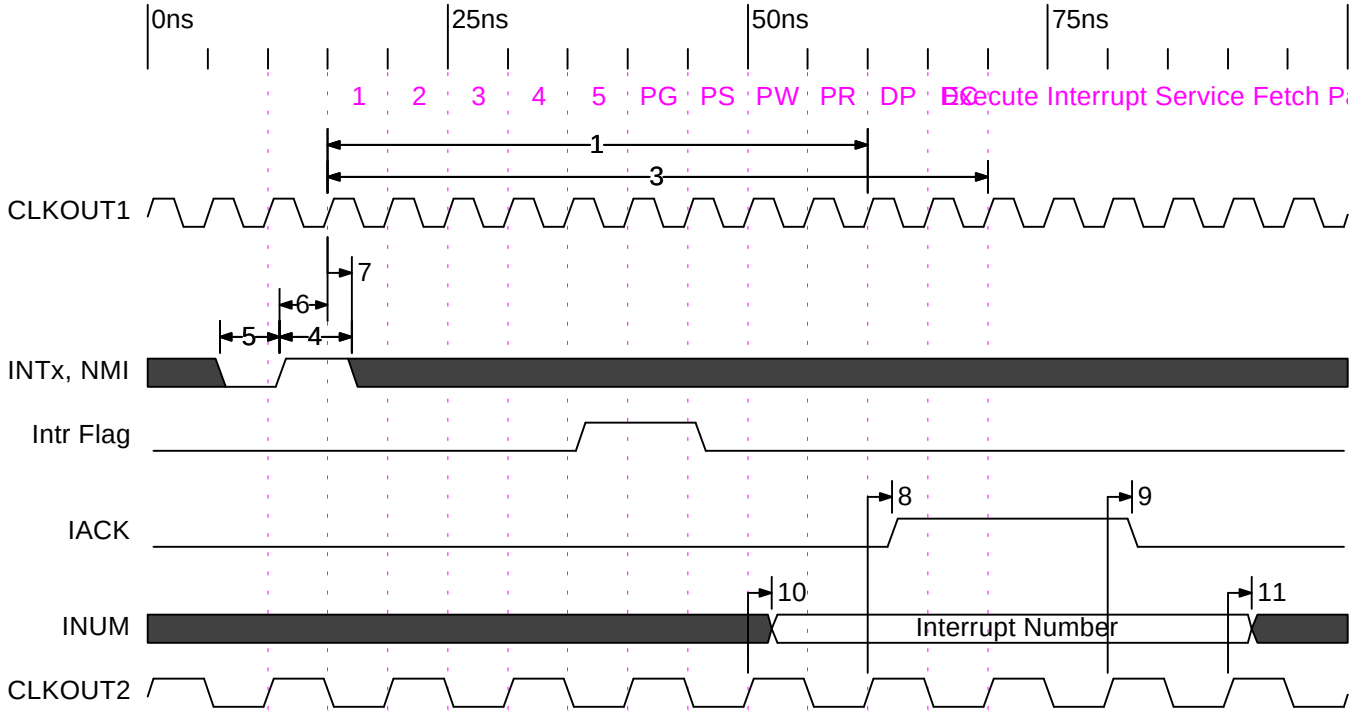
NO			MIN	MAX	UNIT
4	t_w(IHIGH)	Width of the interrupt pulse high			cycles
5	t_w(ILOW)	Width of the interrupt pulse low			cycles
6	t_{su}(IHIGH-CKH)	Setup time, INTx high before CLKOUT1 high			ns
7	t_h(CKH-ILOW)	Hold time, INTx high after CLKOUT1 high			ns

switching characteristics during interrupt responce cycles

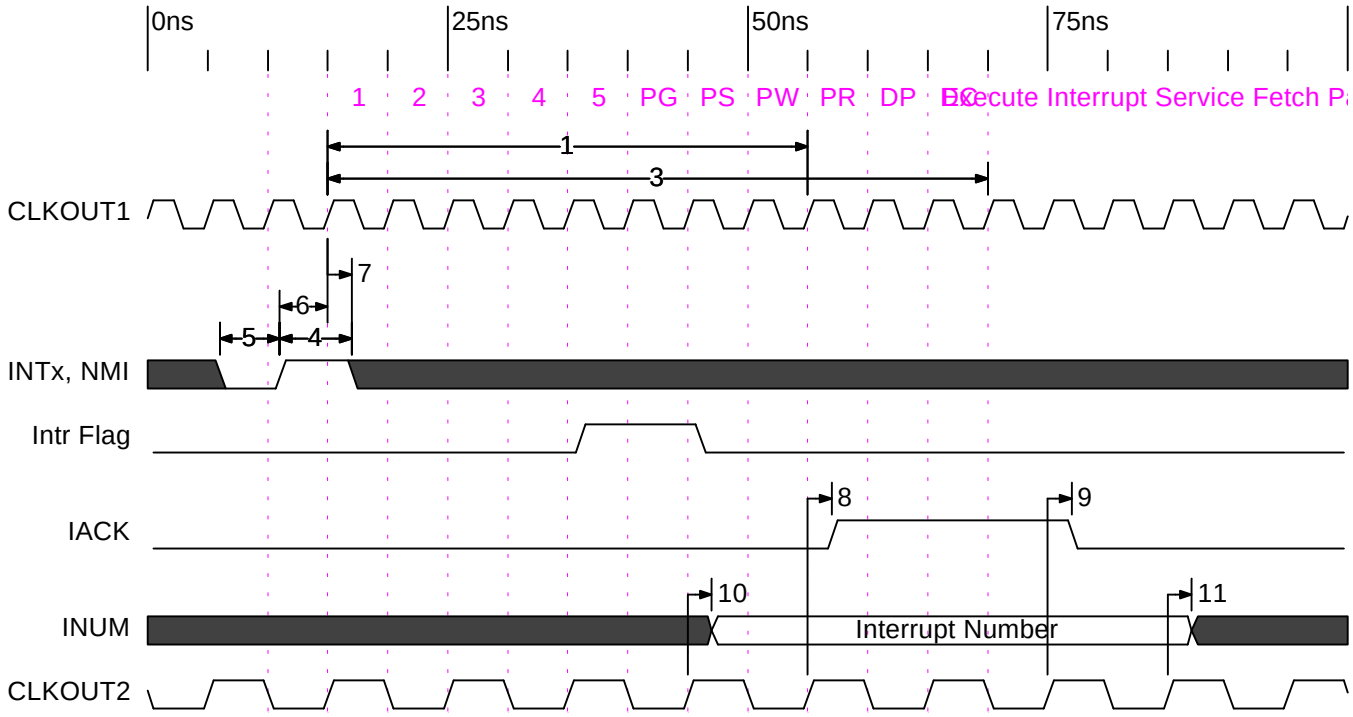
NO			MIN	MAX	UNIT
1	t_r(IACK)	Response time, IACK high after INTx high			cycles
3	t_r(ISFP)	Response time, Interrupt Service Fetch Packet execution after INTX high			cycles
8	t_d(CKH-IACKH)	Delay time, CLKOUT1 high to IACK high			ns
9	t_h(CKH-IACKL)	Hold time, CLKOUT1 high to IACK high			ns
10	t_d(CKH-INUM)	Delay time, CLKOUT1 high to INUM valid			ns
11	t_h(CKH-INUM)	Hold time, CLKOUT1 high to INUM valid			ns

† Add 1 cycle to parameters 1 and 3 if the interrupt is recognized during the low half of CLKOUT2

PRELIMINARY INFORMATION



INTERRUPT TIMING A



INTERRUPT TIMING B

PRELIMINARY INFORMATION

Note: The timing parameters will be disclosed in September 1997.

PRELIMINARY INFORMATION

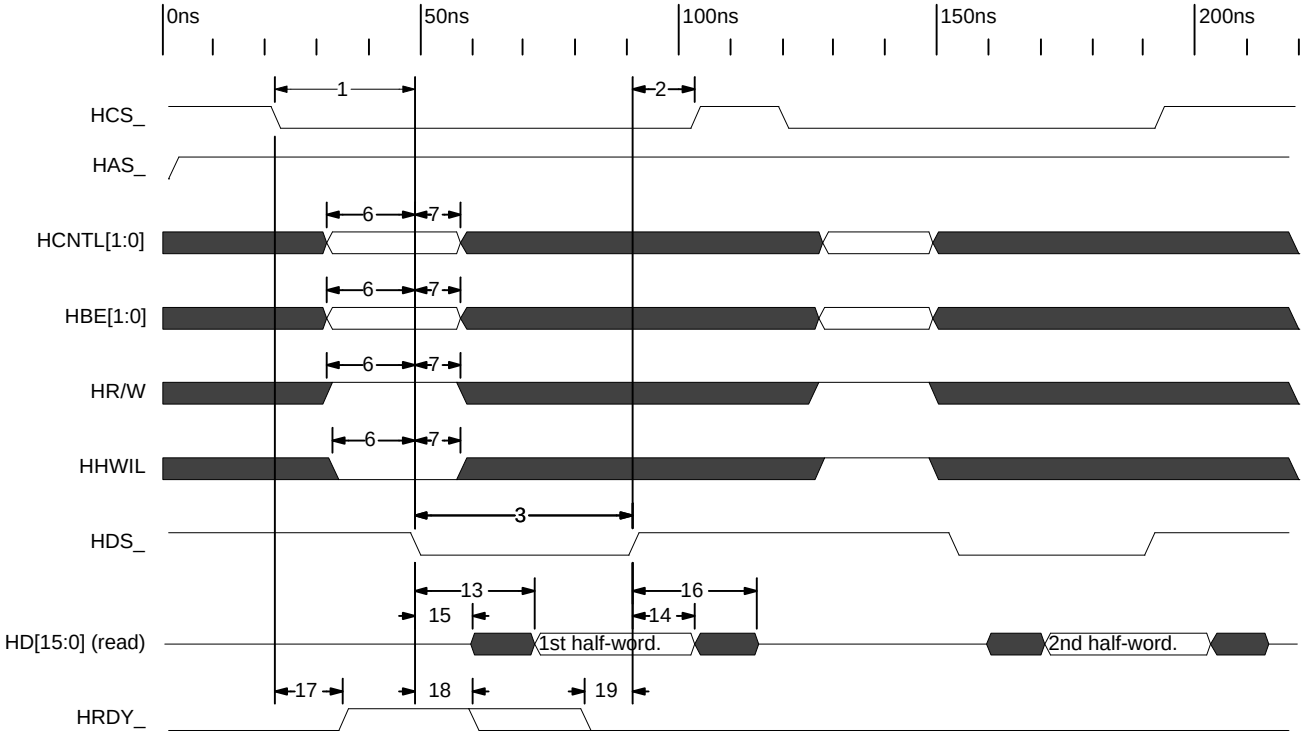
Host Port timing

timing requirements for Host Port Interface cycles

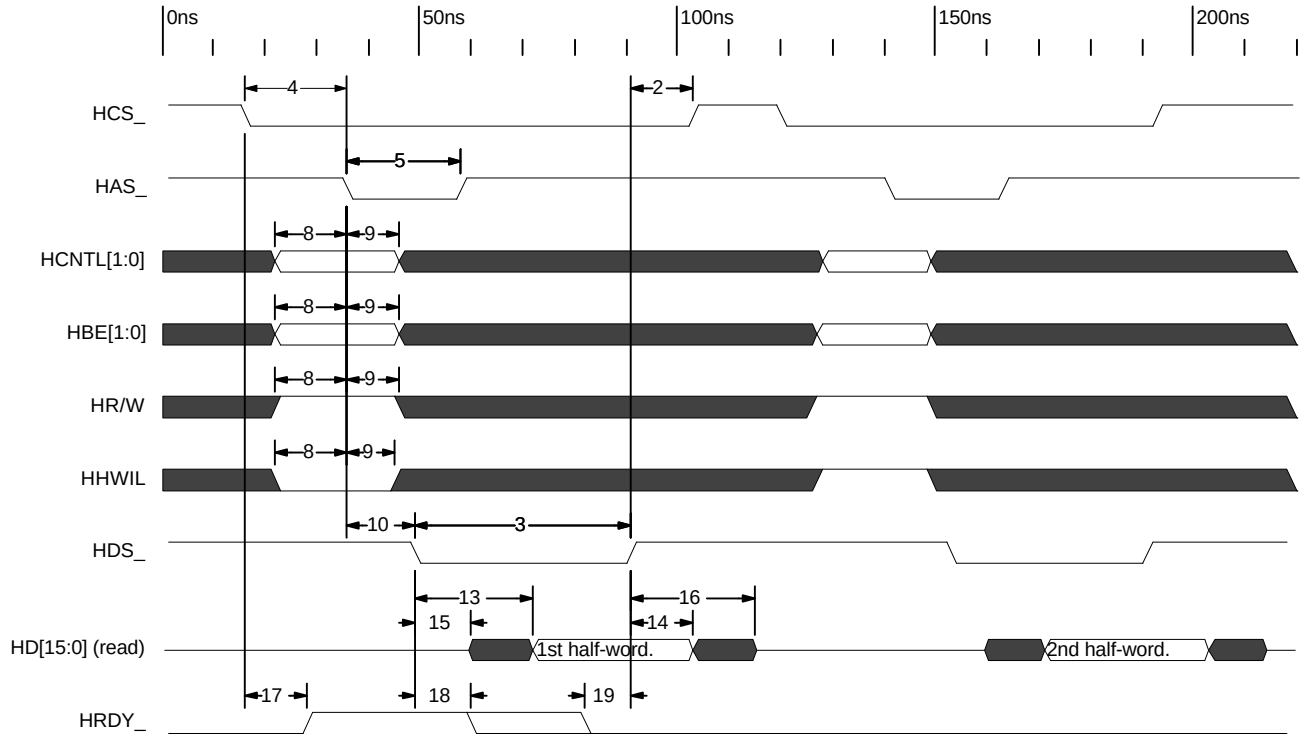
NO			MIN	MAX	UNIT
1	t_{su}(HCSL-HDSL)	Setup time, HCS_ low before HDS_ low			ns
2	t_h(HDSH-HCSL)	Hold time, HCS_ low after HDS_ high			ns
3	t_w(HDS)	Pulse width of HDS_ low			ns
4	t_{su}(HCSL-HASH)	Setup time, HCS_ low before HAS_			ns
5	t_w(HAS)	Pulse width of HAS_ low			ns
6	t_{su}(SEL-HDSL)	Setup time, Select Signals valid before HDS_ low			ns
7	t_h(HDSL-SEL)	Hold time, Select Signals valid after HDS_ low			ns
8	t_{su}(SEL-HASL)	Setup time, Select Signals valid before HAS_ low			ns
9	t_h(HASL-SEL)	Hold time, Select Signals valid after HAS_ low			ns
10	t_d(HASL-HDSL)	Delay time, HAS_ low to HDS_ low			ns
11	t_{su}(HD-HDSH)	Setup time, Host Data valid before HDS_ high			ns
12	t_h(HA-HRW)	Hold time, Host Data valid after HDS_ high			ns

switching characteristics during Host Port Interface cycles

NO			MIN	MAX	UNIT
13	t_d(HDSL-HD)	Delay time, HDS_ low to Host Data valid			ns
14	t_h(HDSH-HD)	Hold time, HDS_ high to Host Data Valid			ns
15	t_h(HDSL-TRI)	Hold time, HDS_ low to Host Data not driven			ns
16	t_d(HDSH-HD)	Delay time, HDS_ high to Host Data not driven			ns
17	t_d(HCSL-HRDYH)	Delay time, HCS_ low to HRDY high			ns
18	t_d(HDSL-HRDY)	Delay time, HDS_ low to HRDY valid			ns
19	t_d(HRDYL-HDSH)	Delay time, HRDY low to HDS_ high			ns



HPI READ TIMING

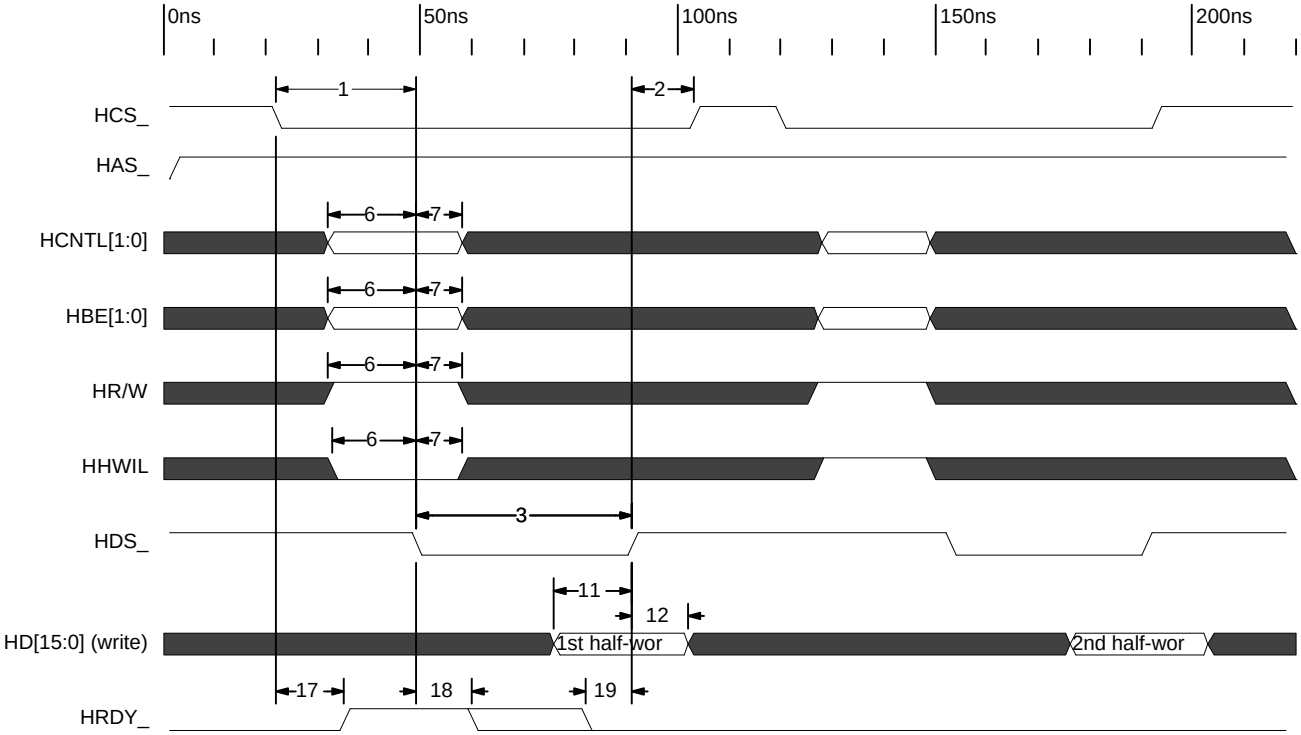


HPI READ TIMING (EARLY ADDRESS)

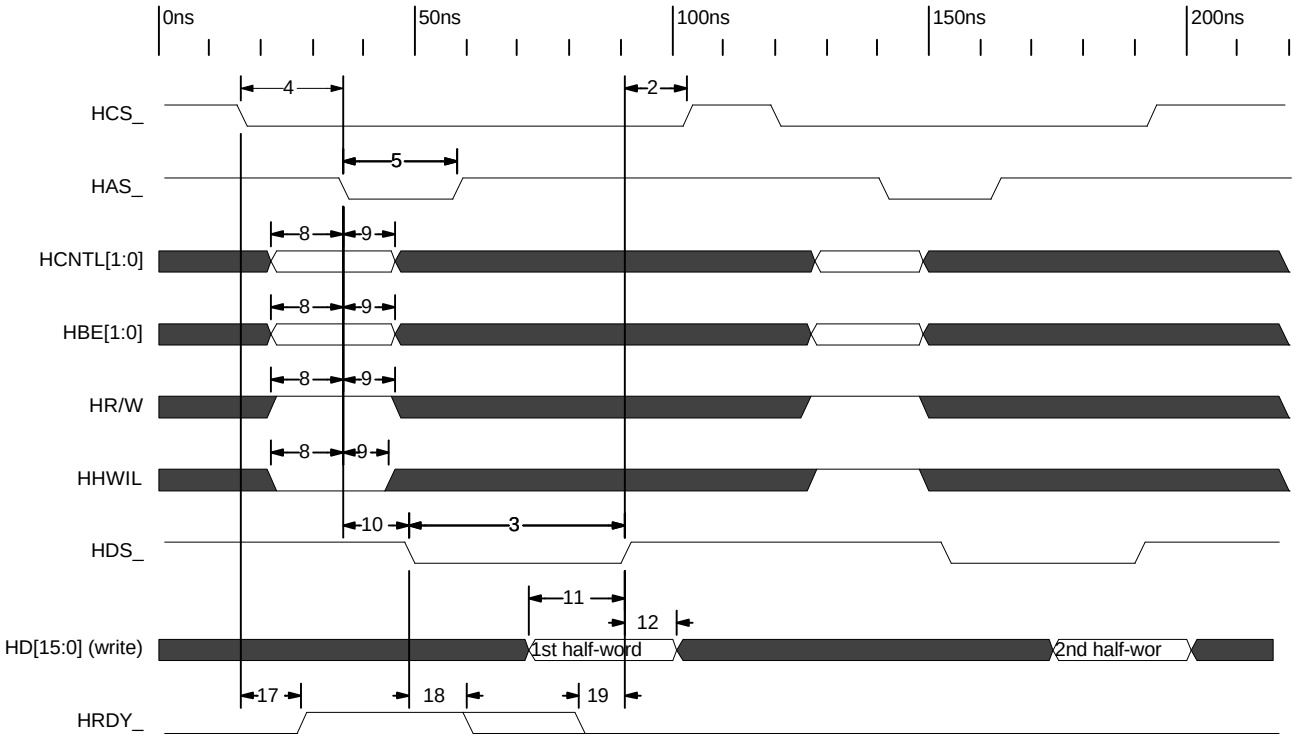
PRELIMINARY INFORMATION

Note: The timing parameters will be disclosed in September 1997.

PRELIMINARY INFORMATION



HPI WRITE TIMING



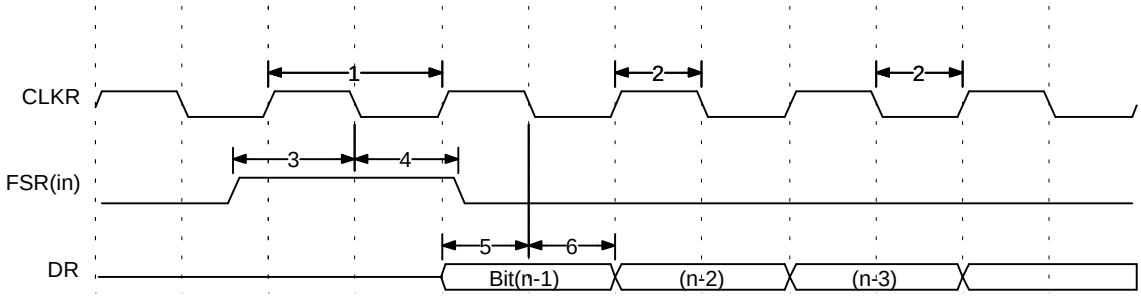
HPI WRITE TIMING (EARLY ADDRESS)

Multi-Channel Serial Port timing

timing requirements for Receive cycles:
Internal or External Clock, External Frame Sync (Input)

NO.	PARAMETER			'C6201 - 200MHz Min	Max	UNIT
1	t_c(SCK)	Period of CLKR	CLKR int			ns
			CLKR ext			ns
2	t_w(SCK)	Pulse duration of CLKR high or CLKR low	CLKR int			ns
			CLKR ext			ns
3	t_{su}(FRH-SCKL)	Setup time, FSR high to CLKR low	CLKR int			ns
			CLKR ext			ns
4	t_h(SCKL-FRH)	Hold time, FSR high after CLKR low	CLKR int			ns
			CLKR ext			ns
5	t_{su}(DRV-SCKL)	Setup time, DR valid to CLKR low	CLKR int			ns
			CLKR ext			ns
6	t_h(SCKL-DRV)	Hold time, DR valid after CLKR low	CLKR int			ns
			CLKR ext			ns

Note: (1) CLKRP=CLKXP=FSRP=FSXP=0 (2) RDATDLY=1



Receive Timing: Internal or External Clock, External Frame Sync (Input)

PRELIMINARY INFORMATION

Note: The timing parameters will be disclosed in September 1997.

PRELIMINARY INFORMATION

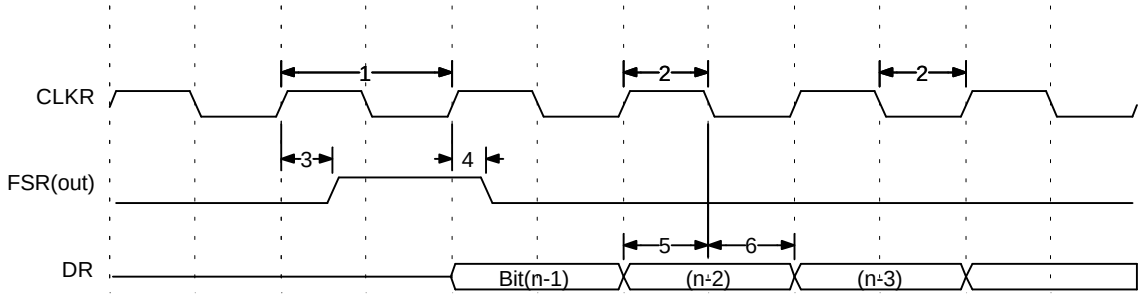
timing requirements for Receive cycles:
Internal or External Clock, Internal Frame Sync (Output)

NO.	PARAMETER			'C6201 - 200MHz Min	Max	UNIT
1	t_c(SCK)	Period of CLKR	CLKR int			ns
			CLKR ext			
2	t_w(SCK)	Pulse duration of CLKR high or CLKR low	CLKR int			ns
			CLKR ext			
5	t_{su}(DRV-SCKL)	Setup time, DR valid to CLKR low	CLKR int			ns
			CLKR ext			
6	t_h(SCKL-DRV)	Hold time, DR valid after CLKR low	CLKR int			ns
			CLKR ext			

switching characteristics for Receive cycles:
Internal or External Clock, Internal Frame Sync (Output)

NO.	PARAMETER			'C6201 - 200MHz Min	Max	UNIT
3	t_{su}(FRH-SCKL)	Delay time, CLKR high to FSR high	CLKR int			ns
			CLKR ext			
4	t_h(SCKL-FRH)	Hold time, FSR high after CLKR low	CLKR int			ns
			CLKR ext			

Note: (1) CLKRP=CLKXP=FSRP=FSXP=0
(2) RDATDLY=1



Receive Timing: Internal or External Clock, Internal Frame Sync (Output)

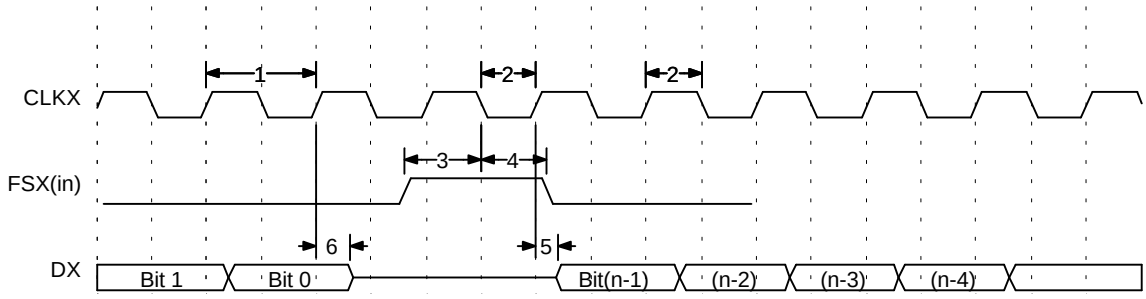
timing requirements for Transmit cycles:
Internal or External Clock, External Frame Sync (Input)

NO.	PARAMETER			'C6201 - 200MHz Min	Max	UNIT
1	t_c(SCK)	Period of CLKX	CLKR int			ns
			CLKR ext			
2	t_w(SCK)	Pulse duration of CLKX high or CLKX low	CLKR int			ns
			CLKR ext			
4	t_h(SCKL-FXH)	Hold time, FSX high after CLKX low	CLKR int			ns
			CLKR ext			

switching characteristics for Transmit cycles:
Internal or External Clock, External Frame Sync (Input)

NO.	PARAMETER			'C6201 - 200MHz Min	Max	UNIT
5	t_d(SCKH-DXV)	Delay time, DX valid after CLKX high	CLKR int			ns
			CLKR ext			
6	t_{dis}(SCKH-DXZ)	Delay or disable time, CLKX high to DX high impedance following last data bit	CLKR int			ns
			CLKR ext			

Note: (1) CLKRP=CLKXP=FSRP=FSXP=0
(2) XDATDLY=1



Transmit Timing: Internal or External Clock, External Frame Sync (Input)

PRELIMINARY INFORMATION

Note: The timing parameters will be disclosed in September 1997.

PRELIMINARY INFORMATION

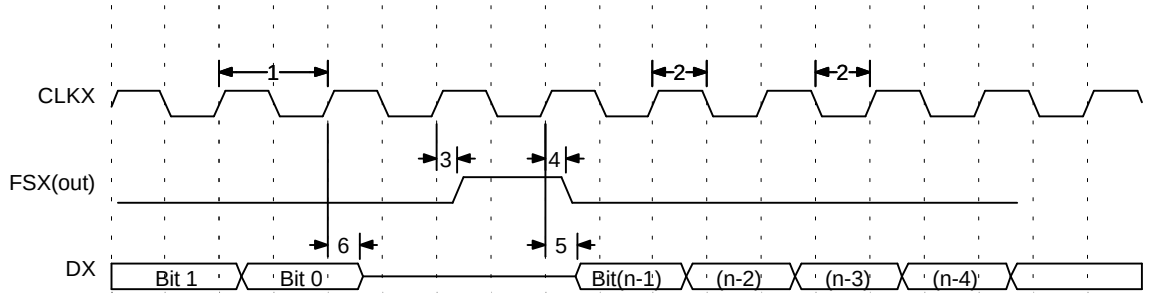
timing requirements for Transmit cycles:
Internal or External Clock, Internal Frame Sync(Output)

NO.	PARAMETER			'C6201 - 200MHz Min	Max	UNIT
1	t_c(SCK)	Period of CLKX	CLKR int			ns
			CLKR ext			
2	t_w(SCK)	Pulse duration of CLKX high or CLKX low	CLKR int			ns
			CLKR ext			

switching characteristics for Transmit cycles:
Internal or External Clock, Internal Frame Sync(Output)

NO.	PARAMETER			'C6201 - 200MHz Min	Max	UNIT
3	t_d(SCKH-FXH)	Delay time, CLKX high to FSX valid high	CLKR int			ns
			CLKR ext			
4	t_h(SCKL-FXH)	Hold time, FSX high after CLKX low	CLKR int			ns
			CLKR ext			
5	t_d(SCKH-DXV)	Delay time, DX valid after CLKX high	CLKR int			ns
			CLKR ext			
6	t_{dis}(SCKH-DXZ)	Delay or disable time, CLKX high to DX high impedance following last data bit	CLKR int			ns
			CLKR ext			

Note: (1) CLKRP=CLKXP=FSRP=FSXP=0
(2) XDATDLY=1



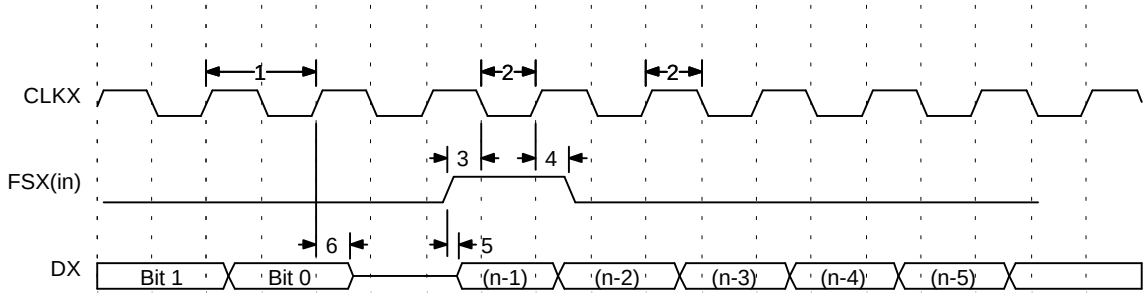
Transmit Timing: Internal or External Clock, Internal Frame Sync(Output)

timing requirements for Zero Data Delay Transmit cycles: Internal or External Clock, External Frame Sync(Input)

NO.	PARAMETER			'C6201 - 200MHz Min	Max	UNIT
1	t_c(SCK)	Period of CLKX	CLKR int			ns
			CLKR ext			
2	t_w(SCK)	Pulse duration of CLKX high or CLKX low	CLKR int			ns
			CLKR ext			
3	t_{su}(SCKL-FXH)	Setup time, CLKX high to FSX high	CLKR int			ns
			CLKR ext			
4	t_h(SCKH-FXH)	Hold time, FSX high after CLKX high	CLKR int			ns
			CLKR ext			

switching characteristics for Zero Data Delay Transmit cycles: Internal or External Clock, External Frame Sync(Input)

NO.	PARAMETER			'C6201 - 200MHz Min	Max	UNIT
5	t_d(SCKH-DXV)	Delay time, DX valid after FSX high	CLKR int			ns
			CLKR ext			
6	t_{dis}(SCKH-DXZ)	Delay or disable time, CLKX high to DX high impedance following last data bit	CLKR int			ns
			CLKR ext			



PRELIMINARY INFORMATION

Note: The timing parameters will be disclosed in September 1997.

Zero Data Delay Transmit Timing: Internal or External Clock, External Frame Sync(Input)

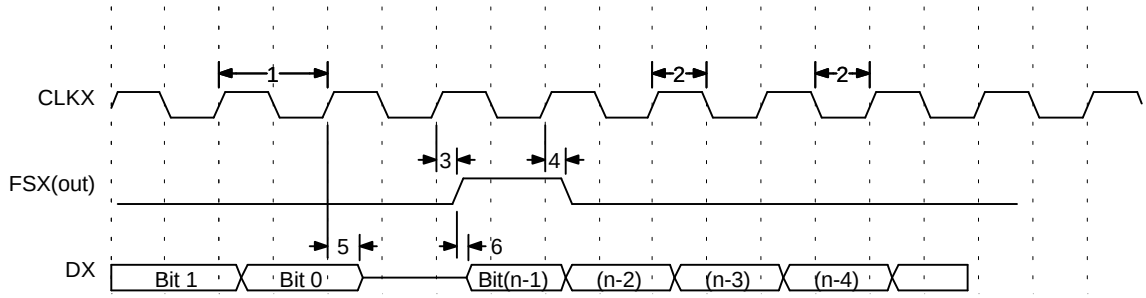
PRELIMINARY INFORMATION

timing requirements for Zero Data Delay Transmit cycles: Internal or External Clock, Internal Frame Sync(Output)

NO.	PARAMETER			'C6201 - 200MHz Min	Max	UNIT
1	t_c(SCK)	Period of CLKX	CLKR int			ns
			CLKR ext			
2	t_w(SCK)	Pulse duration of CLKX high or CLKX low	CLKR int			ns
			CLKR ext			

switching characteristics for Zero Data Delay Transmit cycles: Internal or External Clock, Internal Frame Sync(Output)

NO.	PARAMETER			'C6201 - 200MHz Min	Max	UNIT
3	t_{su}(SCKL-FXH)	Setup time, CLKX high to FSX high	CLKR int			ns
			CLKR ext			
4	t_h(SCKH-FXL)	Hold time, FSX high after CLKX high	CLKR int			
			CLKR ext			
5	t_{dis}(SCKH-DXZ)	Delay or disable time, CLKX high to DX high impedance following last data bit	CLKR int			ns
			CLKR ext			
6	t_d(FXH-DXV)	Delay time, DX valid after FSX high	CLKR int			
			CLKR ext			



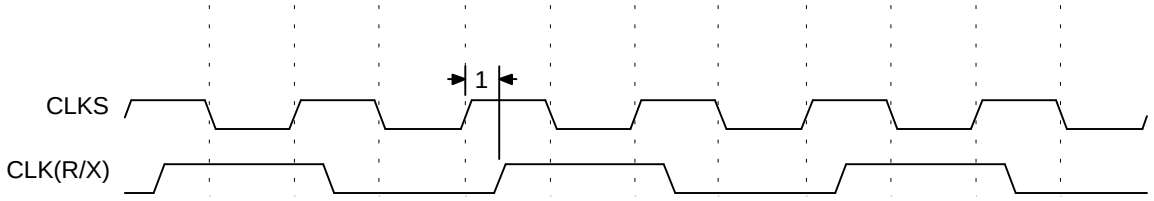
Zero Data Delay Transmit Timing: Internal or External Clock, Internal Frame Sync(Output)

PRELIMINARY INFORMATION

Note: The timing parameters will be disclosed in September 1997.

switching characteristics for Shift Clock with External Clock (CLKSM=1):

NO.	PARAMETER		'C6201 - 200MHz Min	Max	UNIT
1	t_d(CKEH-SCKH)	Delay time, CLKR and CLKX high after CLKS high			ns



Shift Clock timing with External Clock (CLKSM=1)

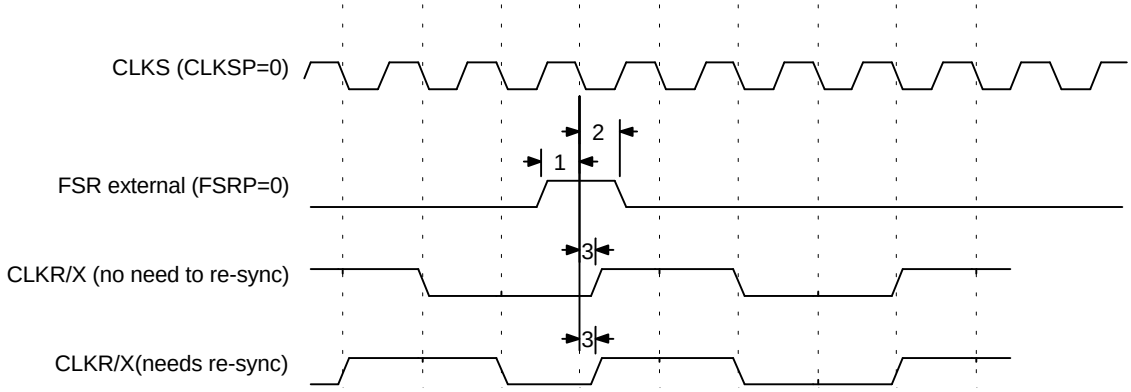
PRELIMINARY INFORMATION

timing requirements for Shift Clock with External Clock and GSYNC=1:

NO.	PARAMETER		'C6201 - 200MHz Min	Max	UNIT
1	t_{su}(FXH-SCKL)	Setup time, FSX high to CLKX low			ns
2	t_h(SCKH-FXL)	Hold time, FSX high after CLKX low			

switching characteristics for Shift Clock with External Clock and GSYNC=1:

NO.	PARAMETER		'C6201 - 200MHz Min	Max	UNIT
3	t_d(CKEH-SCKH)	Delay time, CLKR or CLKX high after CLKS low			



Shift Clock timing with External Clock and GSYNC=1

PRELIMINARY INFORMATION

Note: The timing parameters will be disclosed in September 1997.

PRELIMINARY INFORMATION

timing requirements for MCSP as SPI Master or Slave: CLKSTP=100b

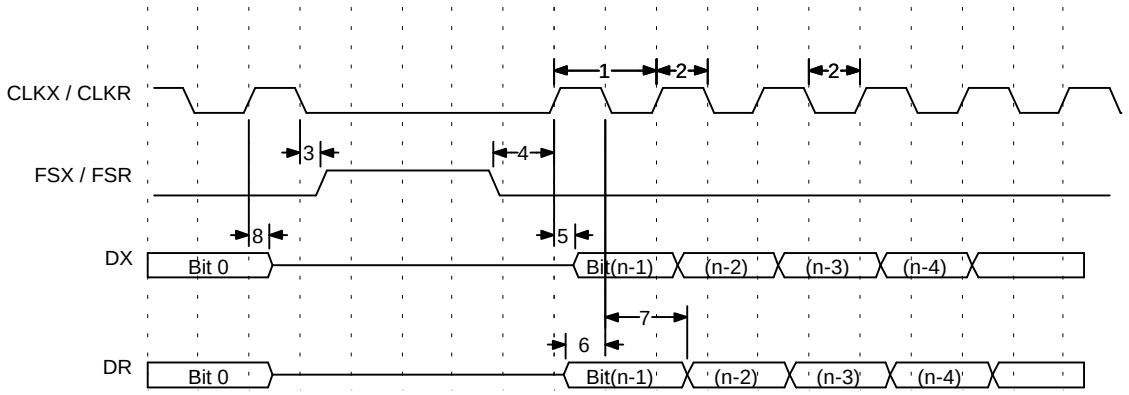
NO.	PARAMETER		'C6201 - 200MHz Min	Max	UNIT
6	t_{su}(DRV-SCKL)	Setup time, DR valid to CLKX low			ns
7	t_h(SCKL-DRV)	Hold time, DR valid after CLKX low			ns

switching characteristics for MCSP as SPI Master or Slave: CLKSTP=100b

NO.	PARAMETER		'C6201 - 200MHz Min	Max	UNIT
1	t_c(SCK)	Period of CLKX			ns
2	t_w(SCK)	Pulse duration of CLKX high or CLKX low			ns
3	t_h(SCKL-FXH)	Hold time, FSX low after CLKX low			ns
4	t_{su}(FXL-SCKH)	Setup time, FSX valid low before CLKX low[1]			ns
5	t_d(SCKH-DXV)	Delay time, CLKX high to DX valid			ns
8	t_{dis}(SCKH-DXZ)	Disable time, CLKX high to DX hi-Z			ns

Notes:

1. FSRP=FSXP=1; As a SPI master, FSX is inverted to provide active low slave enable. FSX input to FSR is inverted to provide an internal active high signal. As a slave, the active low signal input on FSX and FSR is inverted before being used internally.
2. CLKSTP = 100b
3. CLKXM=FSXM=1, CLKRM=FSRM=0 for Master MCSP
4. CLKXM=CLKRM=FSXM=FSRM=0 for Slave MCSP



MCSP Timing as SPI Master or Slave: CLKSTP=100b

[1] FSX should be low before rising edge of clock to enable slave devices and then begin a SPI transfer at the rising edge of master clock (CLKX).

timing requirements for MCSP as SPI Master or Slave: CLKSTP=101b

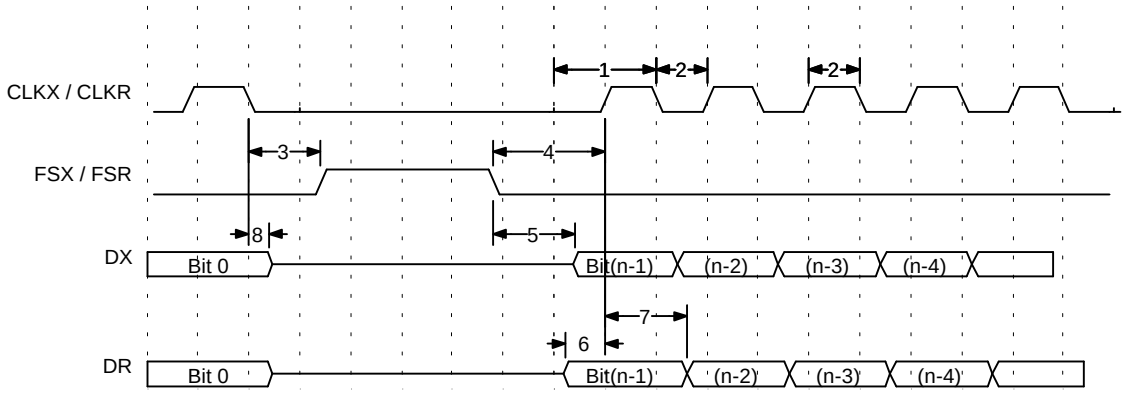
NO.	PARAMETER		'C6201 - 200MHz Min	Max	UNIT
6	t_{su}(DRV-SCKH)	Setup time, DR valid to CLKX high			ns
7	t_h(SCKH-DRV)	Hold time, DR valid after CLKX high			ns

switching characteristics for MCSP as SPI Master or Slave: CLKSTP=101b

NO.	PARAMETER		'C6201 - 200MHz Min	Max	UNIT
1	t_c(SCK)	Period of CLKX			ns
2	t_w(SCK)	Pulse duration of CLKX high or CLKX low			ns
3	t_h(SCKL-FXH)	Hold time, FSX low after CLKX low			ns
4	t_{su}(FXL-SCKH)	Setup time, FSX valid low before CLKX high[2]			ns
5	t_d(FXL-DXV)	Delay time, FSX low to DX valid			ns
8	t_{dis}(SCKL-DXZ)	Disable time, CLKX low to DX hi-Z			ns

Notes:

1. FSRP=FSXP=1; As a SPI master, FSX is inverted to provide active low slave enable. FSX input to FSR is inverted to provide an internal active high signal. As a slave, the active low signal input on FSX and FSR is inverted before being used internally.
2. CLKSTP = 101b
3. CLKXM=FSXM=1, CLKRM=FSRM=0 for Master MCSP
4. CLKXM=CLKRM=FSXM=FSRM=0 for Slave MCSP



MCSP Timing as SPI Master or Slave: CLKSTP=101b

[2] Slave should be enabled before beginning a transfer.

PRELIMINARY INFORMATION

Note: The timing parameters will be disclosed in September 1997.

PRELIMINARY INFORMATION

timing requirements for MCSP as SPI Master or Slave: CLKSTP=110b

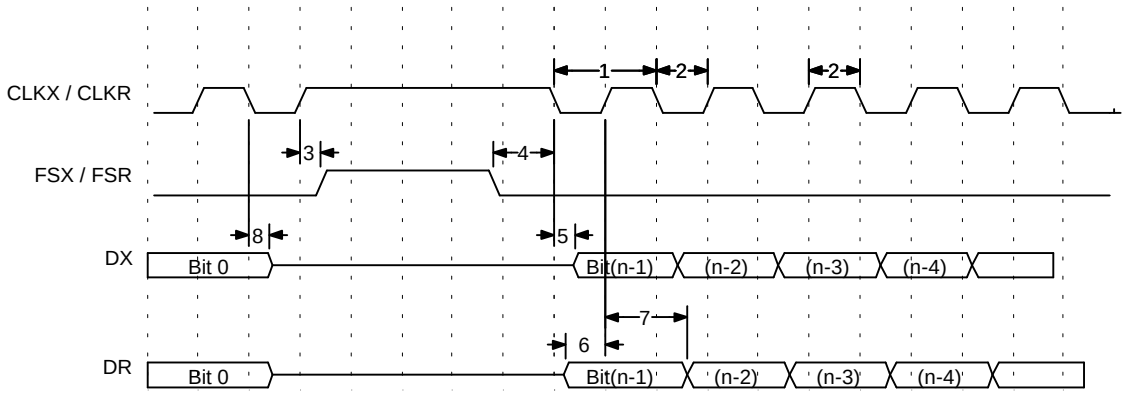
NO.	PARAMETER		'C6201 - 200MHz Min	Max	UNIT
6	t_{su}(DRV-SCKH)	Setup time, DR valid to CLKX high			ns
7	t_h(SCKH-DRV)	Hold time, DR valid after CLKX high			ns

switching characteristics for MCSP as SPI Master or Slave: CLKSTP=110b

NO.	PARAMETER		'C6201 - 200MHz Min	Max	UNIT
1	t_c(SCK)	Period of CLKX			ns
2	t_w(SCK)	Pulse duration of CLKX high or CLKX low			ns
3	t_h(SCKH-FXL)	Hold time, FSX low after CLKX high			ns
4	t_{su}(FXL-SCKL)	Setup time, FSX valid low before CLKX low[3]			ns
5	t_d(SCKL-DXV)	Delay time, CLKX low to DX valid			ns
8	t_{dis}(SCKH-DXZ)	Disable time, CLKX high to DX hi-Z			ns

Notes:

1. FSRP=FSXP=1; As a SPI master, FSX is inverted to provide active low slave enable. FSX input to FSR is inverted to provide an internal active high signal. As a slave, the active low signal input on FSX and FSR is inverted before being used internally.
2. CLKSTP = 110b
3. CLKXM=FSXM=1, CLKRM=FSRM=0 for Master MCSP
4. CLKXM=CLKRM=FSXM=FSRM=0 for Slave MCSP



MCSP Timing as SPI Master or Slave: CLKSTP=110b

[3] Slave should be enabled first before beginning a transfer.

timing requirements for MCSP as SPI Master or Slave: CLKSTP=111b

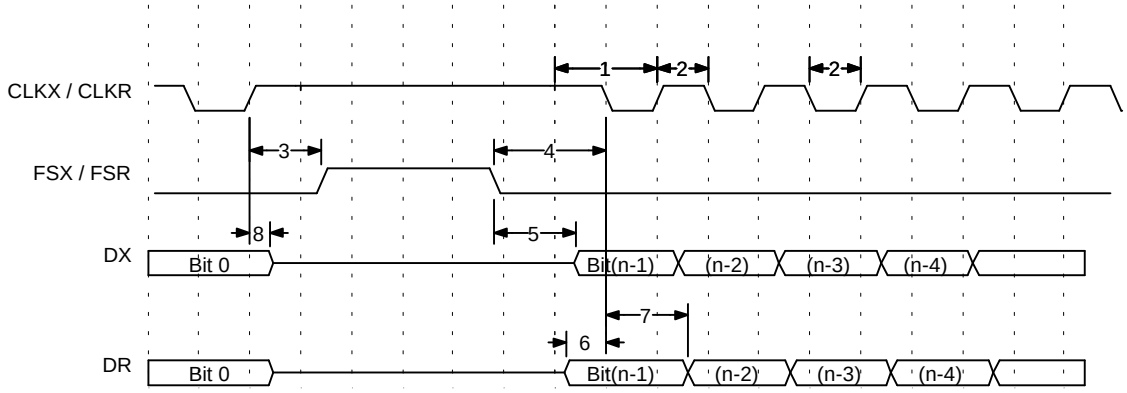
NO.	PARAMETER		'C6201 - 200MHz Min	Max	UNIT
6	t_{su}(DRV-SCKL)	Setup time, DR valid to CLKX low			ns
7	t_h(SCKL-DRV)	Hold time, DR valid after CLKX low			ns

switching characteristics for MCSP as SPI Master or Slave: CLKSTP=111b

NO.	PARAMETER		'C6201 - 200MHz Min	Max	UNIT
1	t_c(SCK)	Period of CLKX			ns
2	t_w(SCK)	Pulse duration of CLKX high or CLKX low			ns
3	t_h(SCKH-FXL)	Hold time, FSX low after CLKX high			ns
4	t_{su}(FXL-SCKL)	Setup time, FSX valid low before CLKX low[4]			ns
5	t_d(FXL-DXV)	Delay time, FSX low to DX valid			ns
8	t_{dis}(SCKH-DXZ)	Disable time, CLKX high to DX hi-Z			ns

Notes:

1. FSRP=FSXP=1; As a SPI master, FSX is inverted to provide active low slave enable. FSX input to FSR is inverted to provide an internal active high signal. As a slave, the active low signal input on FSX and FSR is inverted before being used internally.
2. CLKSTP = 111b
3. CLKXM=FSXM=1, CLKRM=FSRM=0 for Master MCSP
4. CLKXM=CLKRM=FSXM=FSRM=0 for Slave MCSP



MCSP Timing as SPI Master or Slave: CLKSTP=111b

[4] Slave should be enabled first before beginning a transfer.

PRELIMINARY INFORMATION

Note: The timing parameters will be disclosed in September 1997.

PRELIMINARY INFORMATION

signal/pin assignments

NAME	PIN NO.	TYPE	DESCRIPTION
Clock / PLL			
CLKIN	C10	I	Clock Input
CLKOUT1	AF22	O	Clock output at full device speed
CLKOUT2	AF20	O	Clock output at half of device speed
CLKMODE1	C6	I	Clock mode select
CLKMODE0	C5	I •	Selects whether the output clock frequency = input clock freq x4, x2 or x1
PLLFREQ3	A9	I	PLL Frequency Range
PLLFREQ2	D11	I •	Selects one of 5 frequency ranges bounding the CLKOUT1 signal.
PLLFREQ1	B10	I •	CLKOUT1 frequency determines the 3-bit value for the PLLFREQ pins.
RSV2	C11	I	Reserved (pull-high with a dedicated 20KΩ resistor)
PLLV	D12	A †	PLL analog VCC connection for the low-pass filter
PLLG	C12	A †	PLL analog GND connection for the low-pass filter
PLLF	A11	A †	PLL low-pass filter connection to external components and a bypass capacitor
			† A = Analog Signal (PLL Filter)
JTAG Emulation			
TMS	L3	I	JTAG test port mode select (features an internal pull-up)
TDO	W2	O/Z	JTAG test port data out
TDI	R4	I	JTAG test port data in (features an internal pull-up)
TCLK	R3	I	JTAG test port clock
TRST-	T1	I	JTAG test port reset (features an internal pull-down)
EMU1	Y1	I/O/Z	Emulation pin 1, pull-up with a dedicated 20KΩ resistor
EMU0	W3	I/O/Z	Emulation pin 0, pull-up with a dedicated 20KΩ resistor
Control			
RSV0	T2	I	Reserved for testing, pull-up with a dedicated 20KΩ resistor
RSV1	G2	I	Reserved for testing, pull-down with a dedicated 20KΩ resistor
RSV3	B9	I	Reserved. Pull-up with a 20KOhm resistor
RESET-	K2	I	Device Reset
NMI	L2	I	Non-Maskable interrupt
EXT_INT7	U3	I	External interrupts
EXT_INT6	V2	I	
EXT_INT5	W1	I •	Edge driven (programmable edge)
EXT_INT4	U4	I	
IACK	Y2	O	Interrupt acknowledge for all active interrupts serviced by the CPU
INUM3	AA1	O	Active interrupt identification number
INUM2	W4	O •	Valid during IACK for all active interrupts (not just external)
INUM1	AA2	O •	Encoding order follows the Interrupt Service Fetch Packet ordering
INUM0	AB1	O	
LENDIAN	H3	I	If high, selects Little Endian byte/half-word addressing order within a word If low, selects Big Endian addressing
PD-	D3	O	Power-down mode2 and 3 active if low

NAME	PIN NO.	TYPE	DESCRIPTION
Host Port Interface (HPI)			
HINT-	H26	O/Z	Host Interrupt (from DSP to Host)
HCNTRL1	F23	I	Host control - selects between Control, Address or Data registers
HCNTRL0	D25	I	Host control - selects between Control, Address or Data registers
HHWIL	C26	I	Host halfword select - first or second halfword (not necessarily high or low order)
HBE1	E23	I	Host byte select within word or half-word
HBE0	D24	I	Host byte select within word or half-word
HR/W-	C23	I	Host read or write select
HD15	B13	I/O/Z	Host Port Data (used for transfer of data, address and control)
HD14	B14	I/O/Z	
HD13	C14	I/O/Z	
HD12	B15	I/O/Z	
HD11	D15	I/O/Z	
HD10	B16	I/O/Z	
HD9	A17	I/O/Z	
HD8	B17	I/O/Z	
HD7	D16	I/O/Z	
HD6	B18	I/O/Z	
HD5	A19	I/O/Z	
HD4	C18	I/O/Z	
HD3	B19	I/O/Z	
HD2	C19	I/O/Z	
HD1	B20	I/O/Z	
HD0	B21	I/O/Z	
HAS-	C22	I	Host address strobe
HCS-	B23	I	Host chip select
HDS1-	D22	I	Host data strobe 1
HDS2-	A24	I	Host data strobe 2
HRDY-	J24	O	Host ready (from DSP to Host)
Boot mode			
RSV4	A6	I	Reserved for testing, pull-down with a dedicated 20KΩ resistor
BOOTMODE4	D8	I	Boot mode
BOOTMODE3	B4	I	
BOOTMODE2	A3	I	
BOOTMODE1	D5	I	
BOOTMODE0	C4	I	

PRELIMINARY INFORMATION

Note: The timing parameters will be disclosed in September 1997.

NAME	PIN NO.	TYPE	DESCRIPTION
EMIF - control signals common to all types of memory			
CE3-	AE22	O/Z	
CE2-	AD26	O/Z	Memory space enables
CE1-	AB24	O/Z•	enabled by bits 24 and 25 of the word address
CE0-	AC26	O/Z	only one asserted during any external data access
BE3-	AB25	O/Z	Byte enable control (decoded from the 2 lowest bits of the internal address)
BE2-	AA24	O/Z•	byte write enables for most types of memory
BE1-	Y23	O/Z•	can be directly connected to SDRAM read and write mask signal (SDQM)
BE0-	AA26	O/Z	
EMIF - Address			
EA21	J26	O/Z	External Address (word address)
EA20	K25	O/Z	
EA19	L24	O/Z	
EA18	K26	O/Z	
EA17	M26	O/Z	
EA16	M25	O/Z	
EA15	P25	O/Z	
EA14	P24	O/Z	
EA13	R25	O/Z	
EA12	T26	O/Z	
EA11	R23	O/Z	
EA10	U26	O/Z	
EA9	U25	O/Z	
EA8	T23	O/Z	
EA7	V26	O/Z	
EA6	V25	O/Z	
EA5	W26	O/Z	
EA4	V24	O/Z	
EA3	W25	O/Z	
EA2	Y26	O/Z	

PRELIMINARY INFORMATION

NAME	PIN NO.	TYPE	DESCRIPTION
EMIF - Data			
ED31	AB2	I/O/Z	External Data
ED30	AC1	I/O/Z	
ED29	AA4	I/O/Z	
ED28	AD1	I/O/Z	
ED27	AC3	I/O/Z	
ED26	AD4	I/O/Z	
ED25	AF3	I/O/Z	
ED24	AE4	I/O/Z	
ED23	AD5	I/O/Z	
ED22	AF4	I/O/Z	
ED21	AE5	I/O/Z	
ED20	AD6	I/O/Z	
ED19	AE6	I/O/Z	
ED18	AD7	I/O/Z	
ED17	AC8	I/O/Z	
ED16	AF7	I/O/Z	
ED15	AD9	I/O/Z	
ED14	AD10	I/O/Z	
ED13	AF9	I/O/Z	
ED12	AC11	I/O/Z	
ED11	AE10	I/O/Z	
ED10	AE11	I/O/Z	
ED9	AF11	I/O/Z	
ED8	AE14	I/O/Z	
ED7	AF15	I/O/Z	
ED6	AE15	I/O/Z	
ED5	AF16	I/O/Z	
ED4	AC15	I/O/Z	
ED3	AE17	I/O/Z	
ED2	AF18	I/O/Z	
ED1	AF19	I/O/Z	
ED0	AC17	I/O/Z	

PRELIMINARY INFORMATION

Note: The timing parameters will be disclosed in September 1997.

PRELIMINARY INFORMATION

NAME	PIN NO.	TYPE	DESCRIPTION
EMIF - Asynchronous SRAM control			
ARE-	Y24	O/Z	Asynchronous Memory read strobe
AOE-	AC24	O/Z	Asynchronous Memory output enable
AWE-	AD23	O/Z	Asynchronous Memory write enable
ARDY-	W23	I	Asynchronous Memory ready signal
EMIF - Synchronous Burst SRAM control			
SSADS-	AC20	O/Z	SBSRAM address strobe
SSOE-	AF21	O/Z	SBSRAM output enable
SSWE-	AD19	O/Z	SBSRAM write enable
SSCLK	AD17	O/Z	SBSRAM clock
EMIF - Synchronous DRAM control			
SDA10	AD21	O/Z	SDRAM address 10 (separate for refresh)
SDRAS-	AF24	O/Z	SDRAM row address strobe
SDCAS-	AD22	O/Z	SDRAM column address strobe
SDWE-	AF23	O/Z	SDRAM write enable
SDCLK	AE20	O/Z	SDRAM clock
EMIF - Bus arbitration			
HOLD-	AA25	I	Hold request from the host
HOLDA-	A7	O	Hold request acknowledge to the host

NAME	PIN NO.	TYPE	DESCRIPTION
Timers			
TOUT1	H24	O/Z	Timer 1 or general purpose output
TINP1	K24	I	Timer 1 or general purpose input
TOUT0	M4	O/Z	Timer 0 or general purpose output
TINP0	K4	I	Timer 0 or general purpose input
DMA Action Complete			
DMAC3	D2	O	DMA Action Complete
DMAC2	F4	O	
DMAC1	D1	O	
DMAC0	E2	O	
Multi Channel Serial Port 1 (MCSP1)			
CLKS1	E25	I	External clock (as opposed to internal)
CLKR1	H23	I/O/Z	Receive clock
CLKX1	F26	I/O/Z	Transmit clock
DR1	D26	I	Receive data
DX1	G23	O/Z	Transmit data
FSR1	E26	I/O/Z	Receive frame sync
FSX1	F25	I/O/Z	Transmit frame sync
Multi Channel Serial Port 0 (MCSP0)			
CLKS0	L4	I	External clock (as opposed to internal)
CLKR0	M2	I/O/Z	Receive clock
CLKX0	L1	I/O/Z	Transmit clock
DR0	J1	I	Receive data
DX0	R1	O/Z	Transmit data
FSR0	P4	I/O/Z	Receive frame sync
FSX0	P3	I/O/Z	Transmit frame sync

PRELIMINARY INFORMATION

Note: The timing parameters will be disclosed in September 1997.

NAME	PIN NO.	TYPE	DESCRIPTION
Remaining unconnected pins			
	K3		unconnected pins
	J2		
	H1		
	H2		
	G1		
	E4		
	R2		
	C8		
	C21		
	B22		
	D21		
	A23		
	D10		
	C9		
	A8		
	B8		

PRELIMINARY INFORMATION

3.3V Supply Voltage	PIN NO.
DVdd	B7
DVdd	A10
DVdd	A15
DVdd	A18
DVdd	D17
DVdd	A21
DVdd	A22
DVdd	G24
DVdd	G25
DVdd	H25
DVdd	J25
DVdd	L25
DVdd	N23
DVdd	R26
DVdd	T24
DVdd	U24
DVdd	W24
DVdd	AB26
DVdd	AC25
DVdd	AC22
DVdd	AC21
DVdd	AE21
DVdd	AC19
DVdd	AD18
DVdd	AE18
DVdd	AF17
DVdd	AD15
DVdd	AD13
DVdd	AD11
DVdd	AC10
DVdd	AF6
DVdd	AF5
DVdd	AC6
DVdd	AB4
DVdd	AB3
DVdd	Y4
DVdd	N3
DVdd	M3
DVdd	F3
DVdd	C1

2.5V Supply Voltage	PIN NO.
CVdd	D6
CVdd	D7
CVdd	A5
CVdd	B6
CVdd	B11
CVdd	B12
CVdd	A12
CVdd	C15
CVdd	A16
CVdd	A20
CVdd	C20
CVdd	D20
CVdd	K23
CVdd	M24
CVdd	N25
CVdd	AD14
CVdd	AF12
CVdd	AE12
CVdd	AC12
CVdd	AE8
CVdd	AD8
CVdd	T4
CVdd	T3
CVdd	U1
CVdd	P2
CVdd	M1
CVdd	K1
CVdd	F1
CVdd	H4
CVdd	E1

2.5V Supply Voltage	PIN NO.
CVdd	B2
CVdd	C3
CVdd	D4
CVdd	AE2
CVdd	AD3
CVdd	AC4
CVdd	D23
CVdd	C24
CVdd	B25
CVdd	AC23
CVdd	AD24
CVdd	AE25
CVdd	D9
CVdd	D14
CVdd	D18
CVdd	J23
CVdd	P23
CVdd	V23
CVdd	J4
CVdd	N4
CVdd	V4
CVdd	AC9
CVdd	AC13
CVdd	AC18

PRELIMINARY INFORMATION

Note: PLLV and PLLG signals are not part of External Voltage Supply or Ground. See the CLOCK/PLL documentation for information on how to connect those pins.

Note: The timing parameters will be disclosed in September 1997.

PRELIMINARY INFORMATION

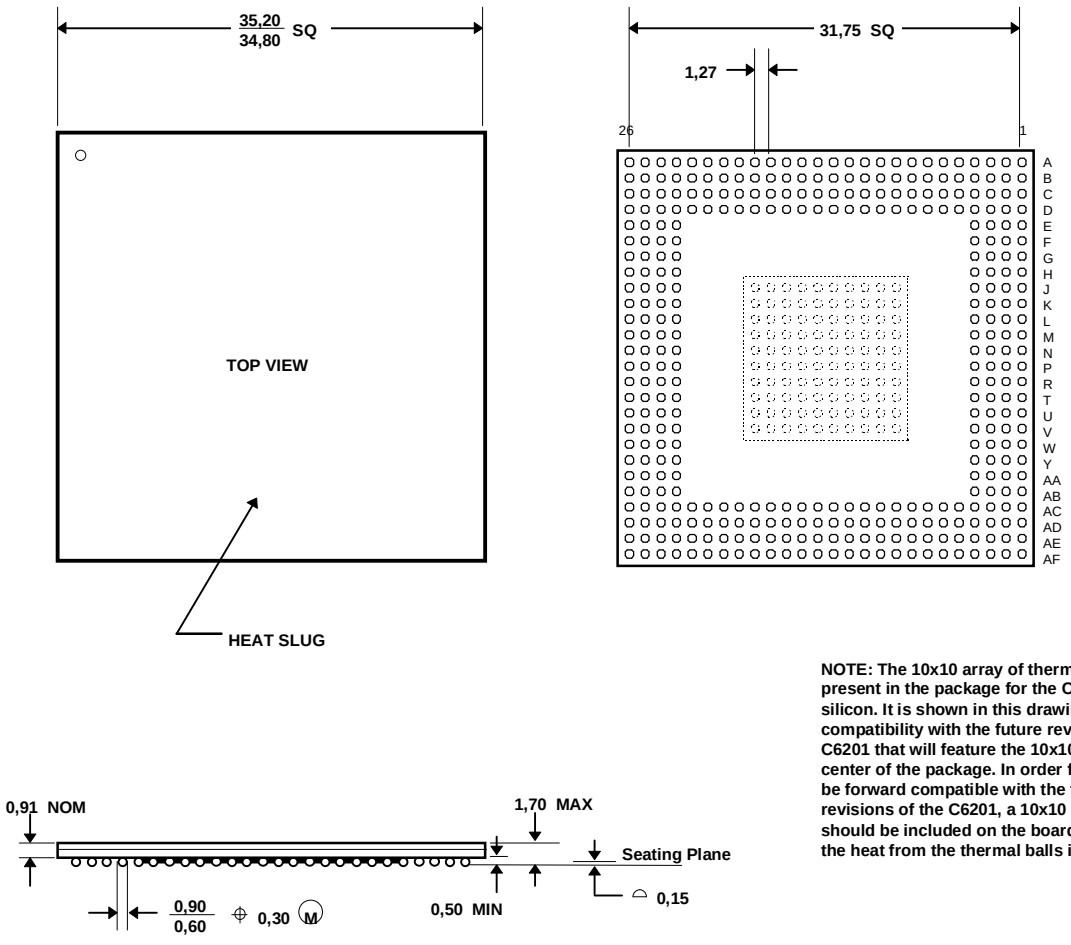
Ground	PIN NO.
Vss	A4
Vss	B5
Vss	C7
Vss	D13
Vss	C13
Vss	C16
Vss	C17
Vss	D19
Vss	E24
Vss	F24
Vss	G26
Vss	L23
Vss	M23
Vss	L26
Vss	N24
Vss	R24
Vss	T25
Vss	U23
Vss	Y25
Vss	AA23
Vss	AB23
Vss	AE23
Vss	AD20
Vss	AE19
Vss	AC16
Vss	AD16
Vss	AE16
Vss	AC14
Vss	AE13
Vss	AD12
Vss	AF10
Vss	AE9
Vss	AF8
Vss	AE7
Vss	AC7
Vss	AC5
Vss	AC2
Vss	AA3
Vss	Y3
Vss	V3

Ground	PIN NO.
Vss	V1
Vss	U2
Vss	N2
Vss	J3
Vss	G3
Vss	F2
Vss	G4
Vss	E3

Ground	PIN NO.
Vss	A1
Vss	B1
Vss	A2
Vss	C2
Vss	B3
Vss	AE1
Vss	AF1
Vss	AD2
Vss	AF2
Vss	AE3
Vss	A25
Vss	A26
Vss	B26
Vss	C25
Vss	B24
Vss	AF25
Vss	AF26
Vss	AE24
Vss	AE26
Vss	AD25
Vss	A13
Vss	A14
Vss	AF13
Vss	AF14
Vss	N1
Vss	P1
Vss	N26
Vss	P26

Note: PLLV and PLLG signals are not part of External Voltage Supply or Ground. See the CLOCK/PLL documentation for information on how to connect those pins.

mechanical data



NOTE: The 10x10 array of thermal balls is not present in the package for the C6201 revision 2 silicon. It is shown in this drawing for compatibility with the future revisions of the C6201 that will feature the 10x10 array in the center of the package. In order for a design to be forward compatible with the future revisions of the C6201, a 10x10 array of pads should be included on the board to channel the heat from the thermal balls into the board.

NOTES : A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Thermally enhanced die down plastic package with top surface metal heat slug

PRELIMINARY INFORMATION

Note: The timing parameters will be disclosed in September 1997.

Thermal Resistance Characteristics for TMX320C6201(SBGA package, 4 layer board, power=5W)

NO			°C/W	Air Flow LFPM †
1	$R\Theta_{JC}$	Junction-to-case		N/A
2	$R\Theta_{JA}$	Junction-to-free air		0
3	$R\Theta_{JA}$	Junction-to-free air		100
4	$R\Theta_{JA}$	Junction-to-free air		250
5	$R\Theta_{JA}$	Junction-to-free air		500

† LFPM = Linear Feet Per Minute

PRELIMINARY INFORMATION