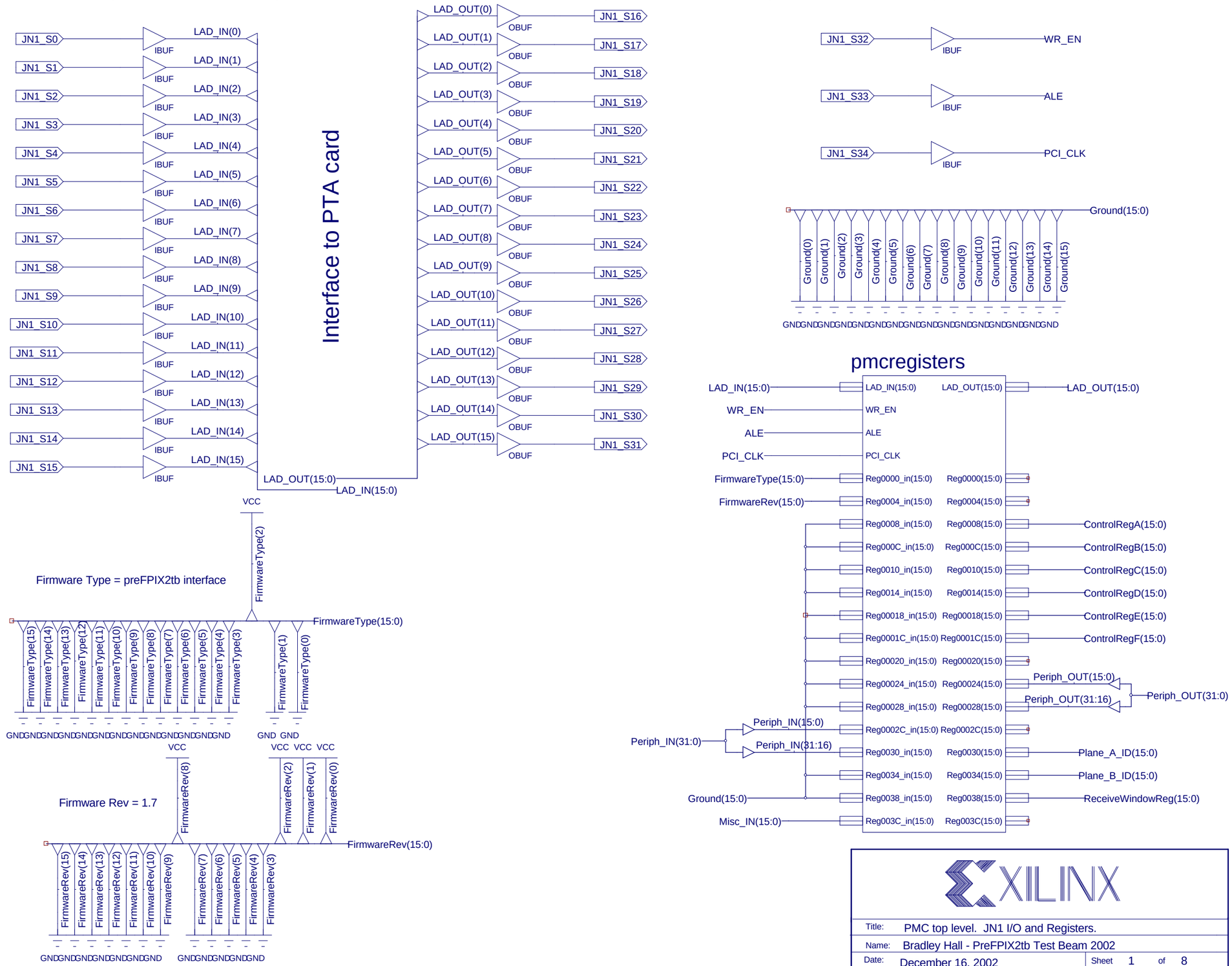
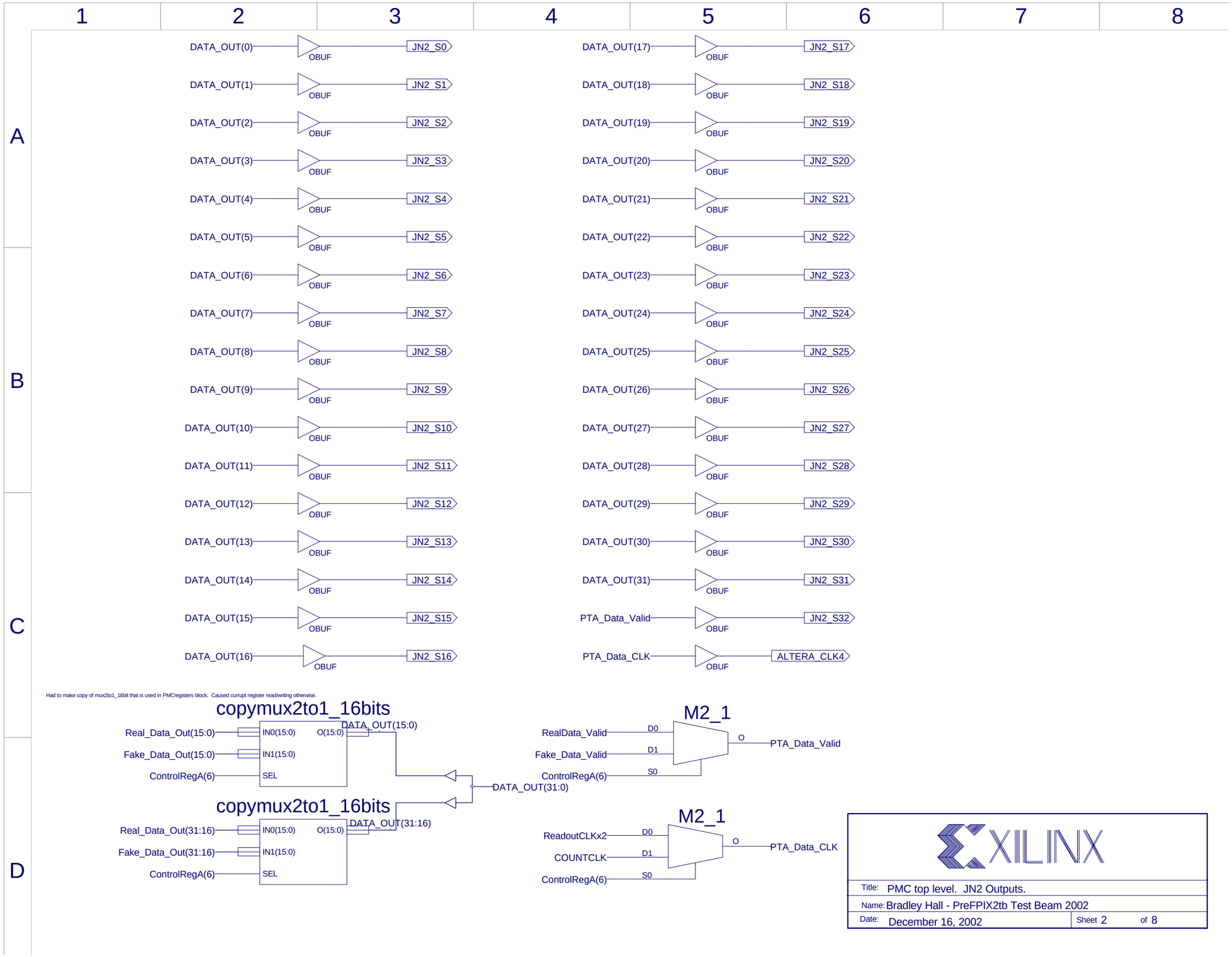
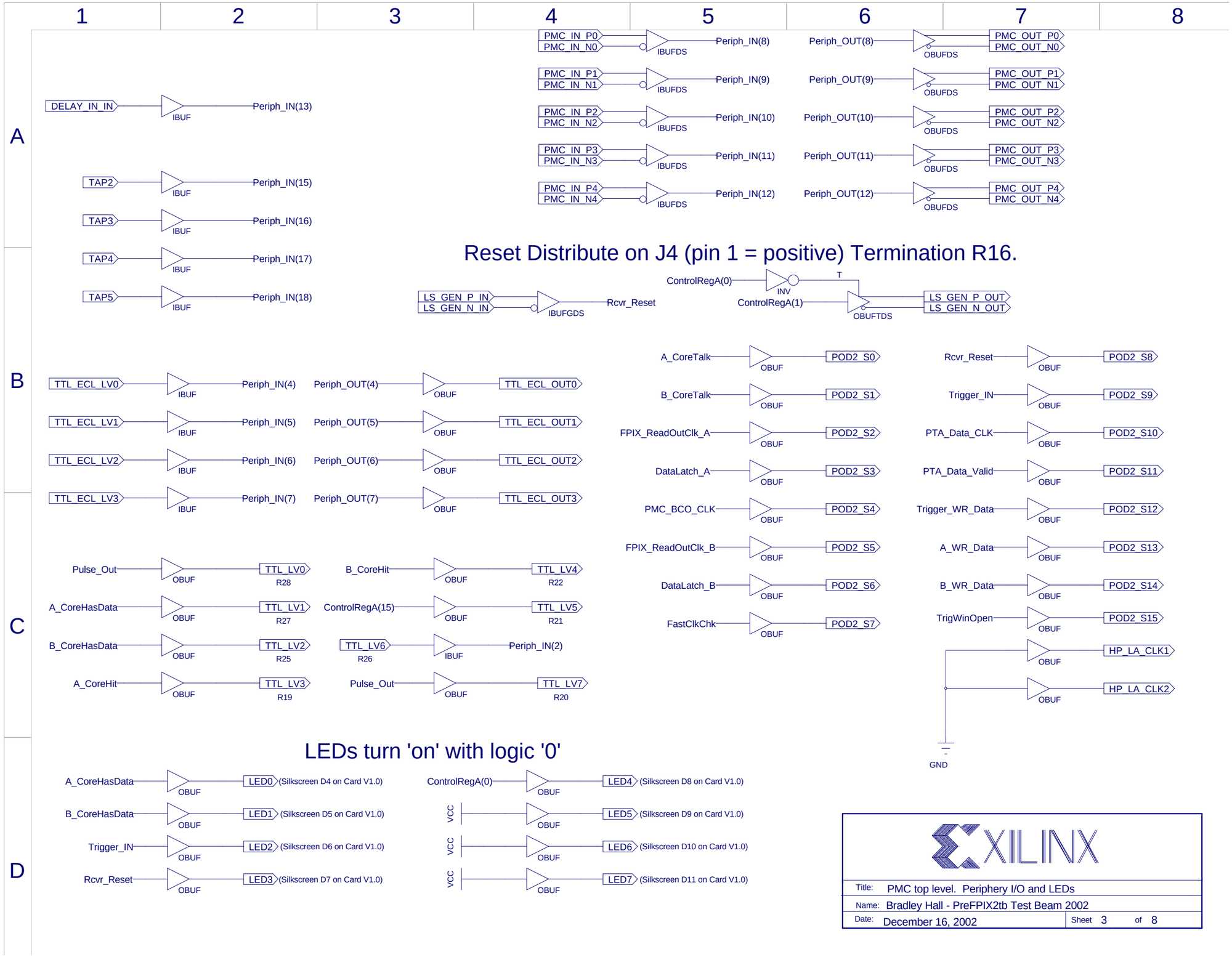
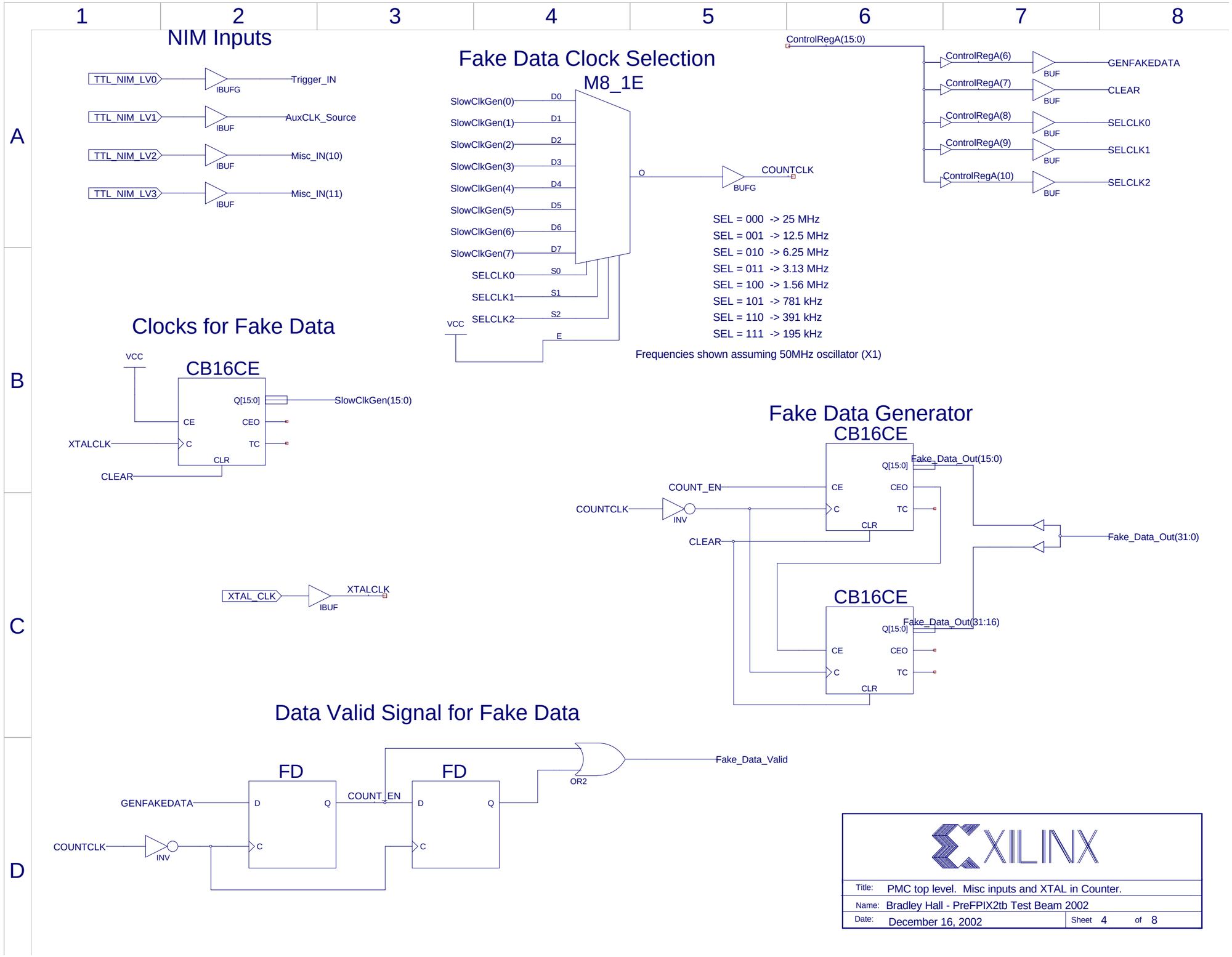
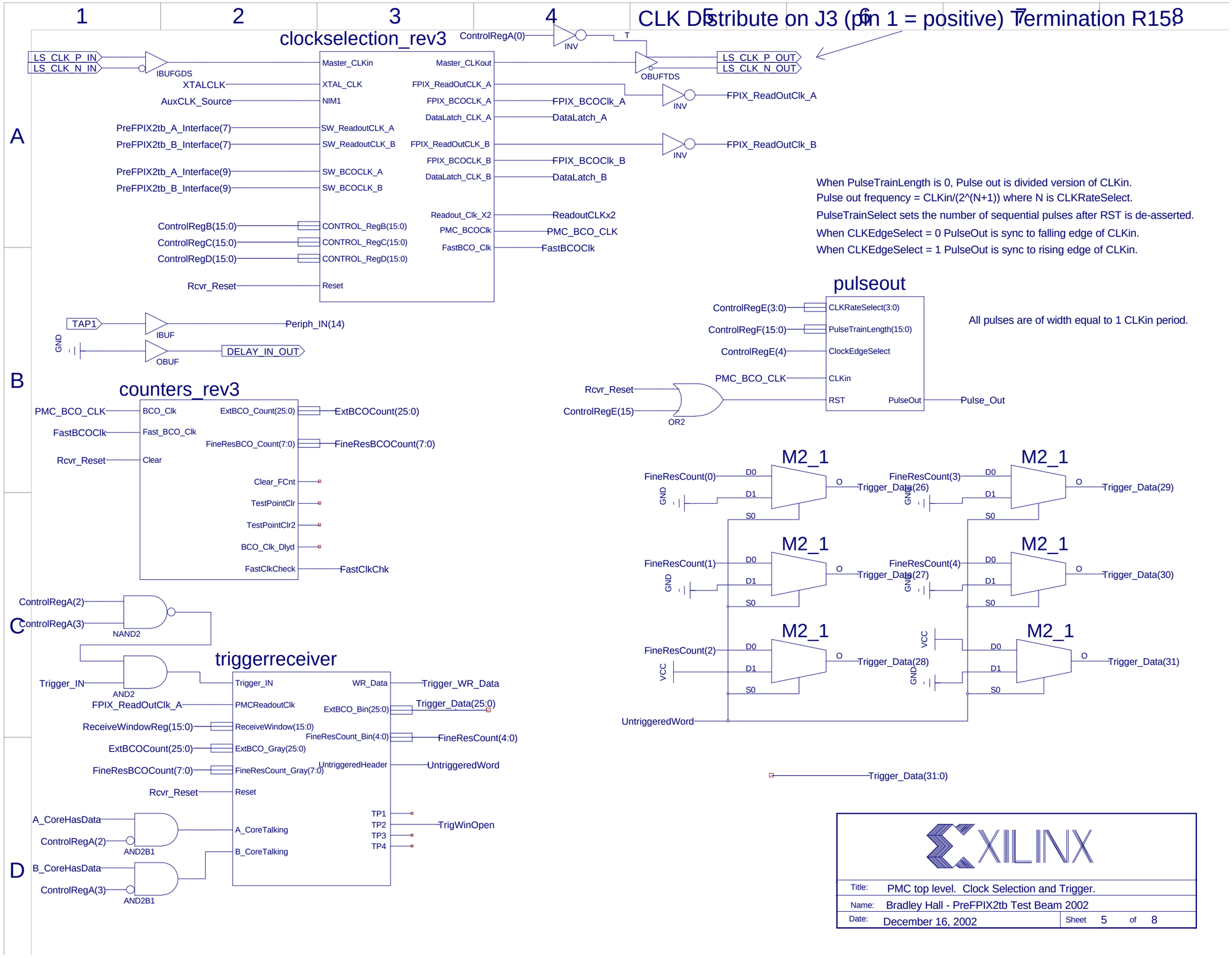

Interface to PTA card
JN1_S0
JN1_S1
JN1_S2
JN1_S3
JN1_S4
JN1_S5
JN1_S6
JN1_S7
JN1_S8
JN1_S9
JN1_S10
JN1_S11
JN1_S12
JN1_S13
JN1_S14
JN1_S15
IBUF
LAD_IN(0)
LAD_IN(1)
LAD_IN(2)
LAD_IN(3)
LAD_IN(4)
LAD_IN(5)
LAD_IN(6)
LAD_IN(7)
LAD_IN(8)
LAD_IN(9)
LAD_IN(10)
LAD_IN(11)
LAD_IN(12)
LAD_IN(13)
LAD_IN(14)
LAD_IN(15)
LAD_OUT(15:0)
LAD_IN(15:0)
OBUF
LAD_OUT(0)
LAD_OUT(1)
LAD_OUT(2)
LAD_OUT(3)
LAD_OUT(4)
LAD_OUT(5)
LAD_OUT(6)
LAD_OUT(7)
LAD_OUT(8)
LAD_OUT(9)
LAD_OUT(10)
LAD_OUT(11)
LAD_OUT(12)
LAD_OUT(13)
LAD_OUT(14)
LAD_OUT(15)
JN1_S16
JN1_S17
JN1_S18
JN1_S19
JN1_S20
JN1_S21
JN1_S22
JN1_S23
JN1_S24
JN1_S25
JN1_S26
JN1_S27
JN1_S28
JN1_S29
JN1_S30
JN1_S31
JN1_S32
JN1_S33
JN1_S34
WR_EN
ALE
PCI_CLK
Ground(15:0)
Ground(0)
Ground(1)
Ground(2)
Ground(3)
Ground(4)
Ground(5)
Ground(6)
Ground(7)
Ground(8)
Ground(9)
Ground(10)
Ground(11)
Ground(12)
Ground(13)
Ground(14)
Ground(15)
GND
pmcregisters
LAD_IN(15:0)
WR_EN
ALE
PCI_CLK
FirmwareType(15:0)
FirmwareRev(15:0)
Ground(15:0)
Misc_IN(15:0)
Periph_IN(31:0)
Periph_IN(15:0)
Periph_IN(31:16)
LAD_OUT(15:0)
Reg0000_in(15:0)
Reg0000(15:0)
Reg0004_in(15:0)
Reg0004(15:0)
Reg0008_in(15:0)
Reg0008(15:0)
Reg000C_in(15:0)
Reg000C(15:0)
Reg0010_in(15:0)
Reg0010(15:0)
Reg0014_in(15:0)
Reg0014(15:0)
Reg00018_in(15:0)
Reg00018(15:0)
Reg0001C_in(15:0)
Reg0001C(15:0)
Reg00020_in(15:0)
Reg00020(15:0)
Reg00024_in(15:0)
Reg00024(15:0)
Reg00028_in(15:0)
Reg00028(15:0)
Reg0002C_in(15:0)
Reg0002C(15:0)
Reg0030_in(15:0)
Reg0030(15:0)
Reg0034_in(15:0)
Reg0034(15:0)
Reg0038_in(15:0)
Reg0038(15:0)
Reg003C_in(15:0)
Reg003C(15:0)
ControlRegA(15:0)
ControlRegB(15:0)
ControlRegC(15:0)
ControlRegD(15:0)
ControlRegE(15:0)
ControlRegF(15:0)
Periph_OUT(15:0)
Periph_OUT(31:16)
Periph_OUT(31:0)
Plane_A_ID(15:0)
Plane_B_ID(15:0)
ReceiveWindowReg(15:0)
VCC
Firmware Type = preFPIX2tb interface
FirmwareType(2)
FirmwareType(15:0)
FirmwareType(15)
FirmwareType(14)
FirmwareType(13)
FirmwareType(12)
FirmwareType(11)
FirmwareType(10)
FirmwareType(9)
FirmwareType(8)
FirmwareType(7)
FirmwareType(6)
FirmwareType(5)
FirmwareType(4)
FirmwareType(3)
FirmwareType(1)
FirmwareType(0)
Firmware Rev = 1.7
FirmwareRev(8)
FirmwareRev(2)
FirmwareRev(1)
FirmwareRev(0)
FirmwareRev(15:0)
FirmwareRev(15)
FirmwareRev(14)
FirmwareRev(13)
FirmwareRev(12)
FirmwareRev(11)
FirmwareRev(10)
FirmwareRev(9)
FirmwareRev(7)
FirmwareRev(6)
FirmwareRev(5)
FirmwareRev(4)
FirmwareRev(3)
XILINX
Title: PMC top level. JN1 I/O and Registers.
Name: Bradley Hall - PreFPIX2tb Test Beam 2002
Date: December 16, 2002
Sheet 1 of 8

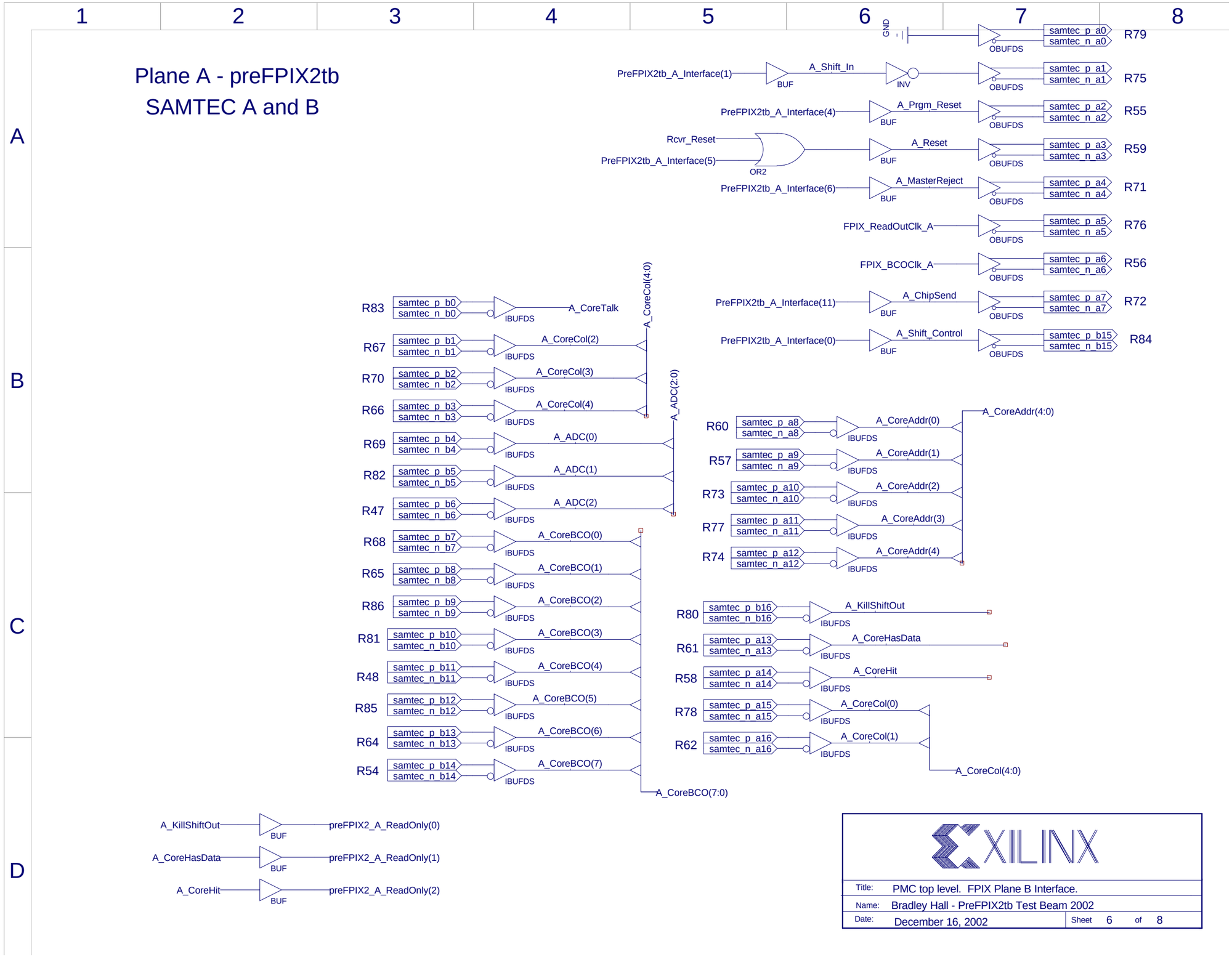

DATA_OUT(0) OBUF JN2_S0
DATA_OUT(1) OBUF JN2_S1
DATA_OUT(2) OBUF JN2_S2
DATA_OUT(3) OBUF JN2_S3
DATA_OUT(4) OBUF JN2_S4
DATA_OUT(5) OBUF JN2_S5
DATA_OUT(6) OBUF JN2_S6
DATA_OUT(7) OBUF JN2_S7
DATA_OUT(8) OBUF JN2_S8
DATA_OUT(9) OBUF JN2_S9
DATA_OUT(10) OBUF JN2_S10
DATA_OUT(11) OBUF JN2_S11
DATA_OUT(12) OBUF JN2_S12
DATA_OUT(13) OBUF JN2_S13
DATA_OUT(14) OBUF JN2_S14
DATA_OUT(15) OBUF JN2_S15
DATA_OUT(16) OBUF JN2_S16
DATA_OUT(17) OBUF JN2_S17
DATA_OUT(18) OBUF JN2_S18
DATA_OUT(19) OBUF JN2_S19
DATA_OUT(20) OBUF JN2_S20
DATA_OUT(21) OBUF JN2_S21
DATA_OUT(22) OBUF JN2_S22
DATA_OUT(23) OBUF JN2_S23
DATA_OUT(24) OBUF JN2_S24
DATA_OUT(25) OBUF JN2_S25
DATA_OUT(26) OBUF JN2_S26
DATA_OUT(27) OBUF JN2_S27
DATA_OUT(28) OBUF JN2_S28
DATA_OUT(29) OBUF JN2_S29
DATA_OUT(30) OBUF JN2_S30
DATA_OUT(31) OBUF JN2_S31
PTA_Data_Valid OBUF JN2_S32
PTA_Data_CLK OBUF ALTERA_CLK4
Had to make copy of mux2to1_16bit that is used in PMCregisters block. Caused currupt register read/writing otherwise.
copymux2to1_16bits
Real_Data_Out(15:0) IN0(15:0)
Fake_Data_Out(15:0) IN1(15:0)
ControlRegA(6) SEL
O(15:0) DATA_OUT(15:0)
copymux2to1_16bits
Real_Data_Out(31:16) IN0(15:0)
Fake_Data_Out(31:16) IN1(15:0)
ControlRegA(6) SEL
O(15:0) DATA_OUT(31:16)
DATA_OUT(31:0)
M2_1
RealData_Valid D0
Fake_Data_Valid D1
ControlRegA(6) S0
O PTA_Data_Valid
M2_1
ReadoutCLKx2 D0
COUNTCLK D1
ControlRegA(6) S0
O PTA_Data_CLK
XILINX
Title: PMC top level. JN2 Outputs.
Name: Bradley Hall - PreFPIX2tb Test Beam 2002
Date: December 16, 2002
Sheet 2 of 8


1 2 3 4 5 6 7 8
A
B
C
D
PMC_IN_P0
PMC_IN_N0
IBUFDS
Periph_IN(8)
Periph_OUT(8)
OBUFDS
PMC_OUT_P0
PMC_OUT_N0
PMC_IN_P1
PMC_IN_N1
Periph_IN(9)
Periph_OUT(9)
PMC_OUT_P1
PMC_OUT_N1
DELAY_IN_IN
IBUF
Periph_IN(13)
PMC_IN_P2
PMC_IN_N2
Periph_IN(10)
Periph_OUT(10)
PMC_OUT_P2
PMC_OUT_N2
PMC_IN_P3
PMC_IN_N3
Periph_IN(11)
Periph_OUT(11)
PMC_OUT_P3
PMC_OUT_N3
TAP2
Periph_IN(15)
PMC_IN_P4
PMC_IN_N4
Periph_IN(12)
Periph_OUT(12)
PMC_OUT_P4
PMC_OUT_N4
TAP3
Periph_IN(16)
TAP4
Periph_IN(17)
Reset Distribute on J4 (pin 1 = positive) Termination R16.
TAP5
Periph_IN(18)
LS_GEN_P_IN
LS_GEN_N_IN
IBUFGDS
Rcvr_Reset
ControlRegA(0)
INV
T
ControlRegA(1)
OBUFTDS
LS_GEN_P_OUT
LS_GEN_N_OUT
A_CoreTalk
POD2_S0
Rcvr_Reset
POD2_S8
TTL_ECL_LV0
Periph_IN(4)
Periph_OUT(4)
TTL_ECL_OUT0
B_CoreTalk
POD2_S1
Trigger_IN
POD2_S9
TTL_ECL_LV1
Periph_IN(5)
Periph_OUT(5)
TTL_ECL_OUT1
FPIX_ReadOutClk_A
POD2_S2
PTA_Data_CLK
POD2_S10
TTL_ECL_LV2
Periph_IN(6)
Periph_OUT(6)
TTL_ECL_OUT2
DataLatch_A
POD2_S3
PTA_Data_Valid
POD2_S11
TTL_ECL_LV3
Periph_IN(7)
Periph_OUT(7)
TTL_ECL_OUT3
PMC_BCO_CLK
POD2_S4
Trigger_WR_Data
POD2_S12
FPIX_ReadOutClk_B
POD2_S5
A_WR_Data
POD2_S13
Pulse_Out
TTL_LV0
R28
B_CoreHit
TTL_LV4
R22
DataLatch_B
POD2_S6
B_WR_Data
POD2_S14
A_CoreHasData
TTL_LV1
R27
ControlRegA(15)
TTL_LV5
R21
FastClkChk
POD2_S7
TrigWinOpen
POD2_S15
B_CoreHasData
TTL_LV2
R25
TTL_LV6
R26
Periph_IN(2)
HP_LA_CLK1
A_CoreHit
TTL_LV3
R19
Pulse_Out
TTL_LV7
R20
HP_LA_CLK2
GND
OBUF
IBUF
LEDs turn 'on' with logic '0'
A_CoreHasData
LED0
(Silkscreen D4 on Card V1.0)
ControlRegA(0)
LED4
(Silkscreen D8 on Card V1.0)
B_CoreHasData
LED1
(Silkscreen D5 on Card V1.0)
VCC
LED5
(Silkscreen D9 on Card V1.0)
Trigger_IN
LED2
(Silkscreen D6 on Card V1.0)
LED6
(Silkscreen D10 on Card V1.0)
Rcvr_Reset
LED3
(Silkscreen D7 on Card V1.0)
LED7
(Silkscreen D11 on Card V1.0)
XILINX
Title: PMC top level. Periphery I/O and LEDs
Name: Bradley Hall - PreFPIX2tb Test Beam 2002
Date: December 16, 2002
Sheet 3 of 8


NIM Inputs
TTL_NIM_LV0
IBUFG
Trigger_IN
TTL_NIM_LV1
IBUF
AuxCLK_Source
TTL_NIM_LV2
IBUF
Misc_IN(10)
TTL_NIM_LV3
IBUF
Misc_IN(11)
Fake Data Clock Selection
M8_1E
SlowClkGen(0)
SlowClkGen(1)
SlowClkGen(2)
SlowClkGen(3)
SlowClkGen(4)
SlowClkGen(5)
SlowClkGen(6)
SlowClkGen(7)
SELCLK0
SELCLK1
SELCLK2
VCC
D0
D1
D2
D3
D4
D5
D6
D7
S0
S1
S2
E
O
BUFG
COUNTCLK
SEL = 000 -> 25 MHz
SEL = 001 -> 12.5 MHz
SEL = 010 -> 6.25 MHz
SEL = 011 -> 3.13 MHz
SEL = 100 -> 1.56 MHz
SEL = 101 -> 781 kHz
SEL = 110 -> 391 kHz
SEL = 111 -> 195 kHz
Frequencies shown assuming 50MHz oscillator (X1)
ControlRegA(15:0)
ControlRegA(6)
ControlRegA(7)
ControlRegA(8)
ControlRegA(9)
ControlRegA(10)
BUF
GENFAKEDATA
CLEAR
SELCLK0
SELCLK1
SELCLK2
Clocks for Fake Data
VCC
CB16CE
Q[15:0]
SlowClkGen(15:0)
CE
CEO
XTALCLK
C
TC
CLR
CLEAR
XTAL_CLK
IBUF
XTALCLK
Fake Data Generator
CB16CE
Fake_Data_Out(15:0)
COUNT_EN
COUNTCLK
INV
CLEAR
Fake_Data_Out(31:0)
CB16CE
Fake_Data_Out(31:16)
Data Valid Signal for Fake Data
FD
FD
GENFAKEDATA
COUNTCLK
INV
D
Q
C
COUNT_EN
OR2
Fake_Data_Valid
XILINX
Title: PMC top level. Misc inputs and XTAL in Counter.
Name: Bradley Hall - PreFPIX2tb Test Beam 2002
Date: December 16, 2002
Sheet 4 of 8

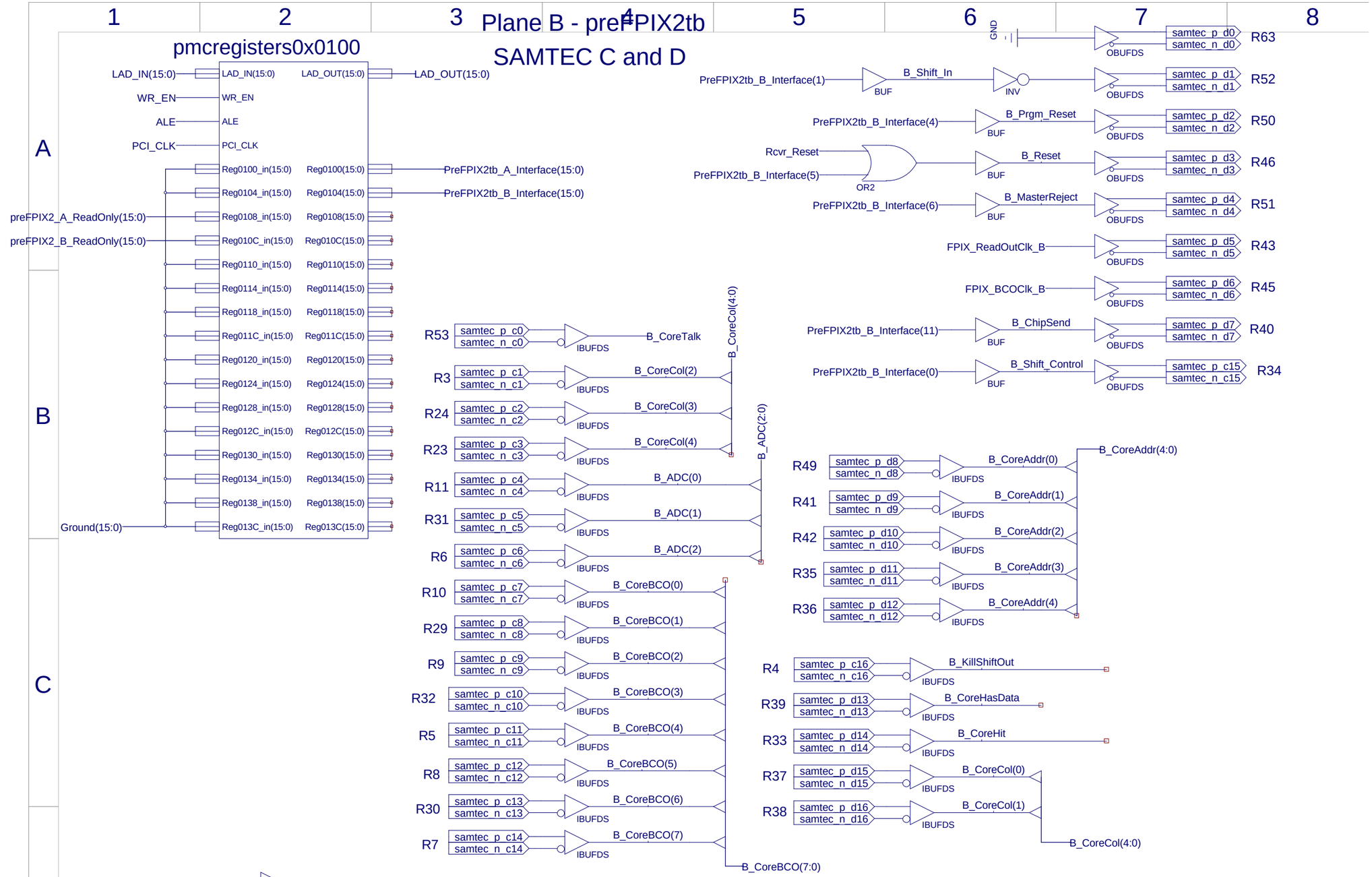

CLK Distribute on J3 (pin 1 = positive) Termination R158
clockselection_rev3
LS_CLK_P_IN
LS_CLK_N_IN
IBUFGDS
XTALCLK
AuxCLK_Source
PreFPIX2tb_A_Interface(7)
PreFPIX2tb_B_Interface(7)
PreFPIX2tb_A_Interface(9)
PreFPIX2tb_B_Interface(9)
ControlRegB(15:0)
ControlRegC(15:0)
ControlRegD(15:0)
Rcvr_Reset
Master_CLKin
XTAL_CLK
NIM1
SW_ReadoutCLK_A
SW_ReadoutCLK_B
SW_BCOCLK_A
SW_BCOCLK_B
CONTROL_RegB(15:0)
CONTROL_RegC(15:0)
CONTROL_RegD(15:0)
Reset
Master_CLKout
FPIX_ReadOutCLK_A
FPIX_BCOCLK_A
DataLatch_CLK_A
FPIX_ReadOutCLK_B
FPIX_BCOCLK_B
DataLatch_CLK_B
Readout_Clk_X2
PMC_BCOClk
FastBCO_Clk
ControlRegA(0)
INV
T
OBUFTDS
LS_CLK_P_OUT
LS_CLK_N_OUT
FPIX_BCOClk_A
DataLatch_A
FPIX_ReadOutClk_A
FPIX_BCOClk_B
DataLatch_B
FPIX_ReadOutClk_B
ReadoutCLKx2
PMC_BCO_CLK
FastBCOClk
TAP1
IBUF
Periph_IN(14)
GND
OBUF
DELAY_IN_OUT
When PulseTrainLength is 0, Pulse out is divided version of CLKin.
Pulse out frequency = CLKin/(2^(N+1)) where N is CLKRateSelect.
PulseTrainSelect sets the number of sequential pulses after RST is de-asserted.
When CLKEdgeSelect = 0 PulseOut is sync to falling edge of CLKin.
When CLKEdgeSelect = 1 PulseOut is sync to rising edge of CLKin.
pulseout
ControlRegE(3:0)
ControlRegF(15:0)
ControlRegE(4)
PMC_BCO_CLK
Rcvr_Reset
ControlRegE(15)
OR2
CLKRateSelect(3:0)
PulseTrainLength(15:0)
ClockEdgeSelect
CLKin
RST
PulseOut
Pulse_Out
All pulses are of width equal to 1 CLKin period.
counters_rev3
PMC_BCO_CLK
FastBCOClk
Rcvr_Reset
BCO_Clk
Fast_BCO_Clk
Clear
ExtBCO_Count(25:0)
FineResBCO_Count(7:0)
Clear_FCnt
TestPointClr
TestPointClr2
BCO_Clk_Dlyd
FastClkCheck
ExtBCOCount(25:0)
FineResBCOCount(7:0)
FastClkChk
M2_1
FineResCount(0)
FineResCount(1)
FineResCount(2)
FineResCount(3)
FineResCount(4)
D0
D1
S0
O
Trigger_Data(26)
Trigger_Data(27)
Trigger_Data(28)
Trigger_Data(29)
Trigger_Data(30)
Trigger_Data(31)
VCC
UntriggeredWord
Trigger_Data(31:0)
ControlRegA(2)
ControlRegA(3)
NAND2
Trigger_IN
AND2
triggerreceiver
FPIX_ReadOutClk_A
ReceiveWindowReg(15:0)
ExtBCOCount(25:0)
FineResBCOCount(7:0)
Rcvr_Reset
Trigger_IN
PMCReadoutClk
ReceiveWindow(15:0)
ExtBCO_Gray(25:0)
FineResCount_Gray(7:0)
Reset
WR_Data
ExtBCO_Bin(25:0)
FineResCount_Bin(4:0)
UntriggeredHeader
TP1
TP2
TP3
TP4
Trigger_WR_Data
Trigger_Data(25:0)
FineResCount(4:0)
UntriggeredWord
TrigWinOpen
A_CoreHasData
ControlRegA(2)
AND2B1
B_CoreHasData
ControlRegA(3)
A_CoreTalking
B_CoreTalking
A
B
C
D
XILINX
Title: PMC top level. Clock Selection and Trigger.
Name: Bradley Hall - PreFPIX2tb Test Beam 2002
Date: December 16, 2002
Sheet 5 of 8

Plane A - preFPIX2tb
SAMTEC A and B

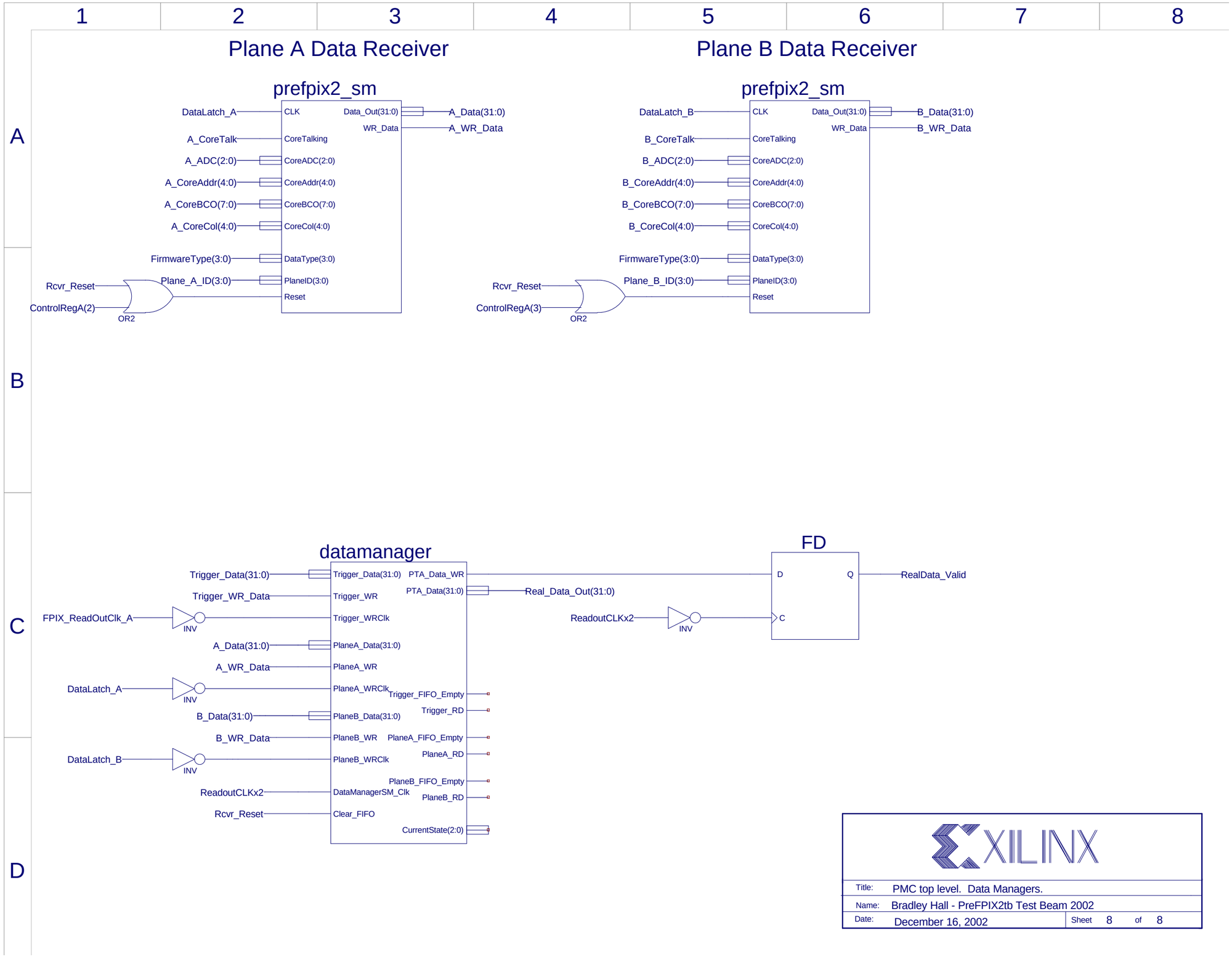


Title:	PMC top level. FPIX Plane B Interface.
Name:	Bradley Hall - PreFPIX2tb Test Beam 2002
Date:	December 16, 2002
Sheet	6 of 8

Plane B - preFPIX2tb SAMTEC C and D



Title:	PMC top level. FPIX Plane B Interface.
Name:	Bradley Hall - PreFPIX2tb Test Beam 2002
Date:	December 16, 2002
Sheet	7 of 8


1
2
3
4
5
6
7
8
A
B
C
D
Plane A Data Receiver
prefpix2_sm
DataLatch_A
A_CoreTalk
A_ADC(2:0)
A_CoreAddr(4:0)
A_CoreBCO(7:0)
A_CoreCol(4:0)
FirmwareType(3:0)
Plane_A_ID(3:0)
Rcvr_Reset
ControlRegA(2)
OR2
CLK
CoreTalking
CoreADC(2:0)
CoreAddr(4:0)
CoreBCO(7:0)
CoreCol(4:0)
DataType(3:0)
PlaneID(3:0)
Reset
Data_Out(31:0)
WR_Data
A_Data(31:0)
A_WR_Data
Plane B Data Receiver
prefpix2_sm
DataLatch_B
B_CoreTalk
B_ADC(2:0)
B_CoreAddr(4:0)
B_CoreBCO(7:0)
B_CoreCol(4:0)
FirmwareType(3:0)
Plane_B_ID(3:0)
Rcvr_Reset
ControlRegA(3)
OR2
CLK
CoreTalking
CoreADC(2:0)
CoreAddr(4:0)
CoreBCO(7:0)
CoreCol(4:0)
DataType(3:0)
PlaneID(3:0)
Reset
Data_Out(31:0)
WR_Data
B_Data(31:0)
B_WR_Data
datamanager
Trigger_Data(31:0)
Trigger_WR_Data
FPIX_ReadOutClk_A
INV
A_Data(31:0)
A_WR_Data
DataLatch_A
INV
B_Data(31:0)
B_WR_Data
DataLatch_B
INV
ReadoutCLKx2
Rcvr_Reset
Trigger_Data(31:0)
Trigger_WR
Trigger_WRClk
PlaneA_Data(31:0)
PlaneA_WR
PlaneA_WRClk
PlaneB_Data(31:0)
PlaneB_WR
PlaneB_WRClk
DataManagerSM_Clk
Clear_FIFO
PTA_Data_WR
PTA_Data(31:0)
Trigger_FIFO_Empty
Trigger_RD
PlaneA_FIFO_Empty
PlaneA_RD
PlaneB_FIFO_Empty
PlaneB_RD
CurrentState(2:0)
Real_Data_Out(31:0)
FD
D
Q
C
RealData_Valid
ReadoutCLKx2
INV
XILINX
Title: PMC top level. Data Managers.
Name: Bradley Hall - PreFPIX2tb Test Beam 2002
Date: December 16, 2002
Sheet 8 of 8