

MI BPM Project
MI BPM TB Controller Status Report January 10th, 2006, 9:30am

Hardware status

MI BPM_TB Controller Prototype:

-) Completed Prototype Layout.
-) Placed order for PCB fabrication (thanks to Bakul BANERJEE).
-) Submitted PCB design for fabrication to CYREXX, CA (Wednesday January 4th).
-) Received PCB from manufacturer (Monday January 9th)
-) Parts ordered and mostly received (thanks to Manfred WENDT).
-) Assembled first board.

Interface with the MI BPM TB:

-) To start interface tests today using:
 - 1) MI BPM_TB Controller Prototype
 - 2) MI BPM TB (digital logic only)
 - 3) VME P1 Backplane

Firmware status:

MI BPM_TB Firmware

-) From Status report January 3rd :
*“First release completed as specification.
Allows for the MI_BPM_TB to be remotely controlled
It requires an external test signal.”*
-) Work in progress on second release which provides for an on board test signal and more diagnostics.

MI BPM_TB Controller Prototype Firmware (Avnet Xilinx card FPGA)

-) From Status report January 3rd :
“Implemented simplified interface with MI_BPM_TB”.
-) Work in progress on new version with more diagnostic and the capability to generate an on-board test signal and more diagnostics.
-) Worked with Bill Haynes to define an initial (simple) interface protocol between the Timing Module and the MI_BPM_TB Controller.

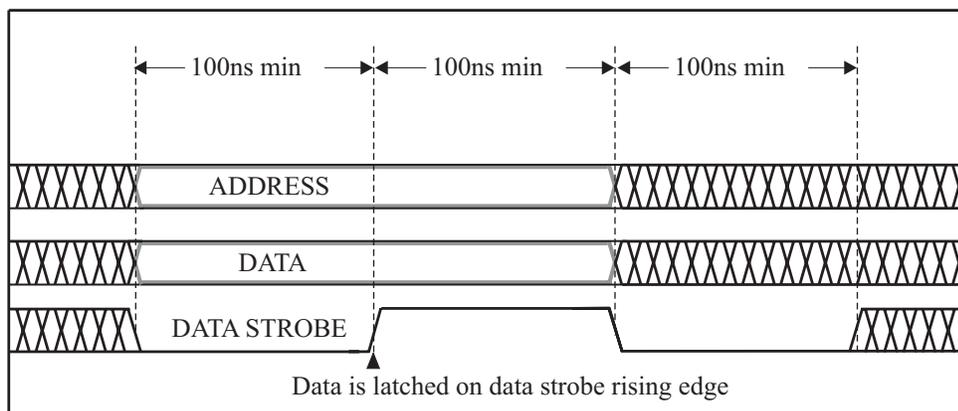
Preliminary Specification Proposal for the
Interface between the Timing Module and the MI BPM TB Controller
January 5th, 2005

Signal	Notes
FECTL[15..0]	Data (mapped to TB)
FECTL[16]	Data Strobe (mapped to TB)
FECTL[18..17]	Address (mapped to TB)
FECTL[21..19]	Reserved (mapped to TB). Driven low.
FECTL[27..22]	Reserved (not Mapped to TB). Driven low.
FECTL[28]	Data Bus Direction (not Mapped to TB).
FECTL[30..29]	Reserved (not Mapped to TB).
FECTL[31]	Test Signal (mapped to TB).

Timing Module Interface signal assignments

Timing Module Interface Address Space Mapping		
Address bus is 2 bit wide. Address bits are: FECTL[18..17]		
Data MSB, FECTL[15..8]	Data LSB, FECTL[7..0]	Address
MI BPM TB control register 0		0x0
MI BPM TB control register 1		0x1
MI BPM TB control register 2		0x2
MI BPM TB control register 3		0x3

Address Space Mapping



Timing Module Interface Protocol

MI BPM_TB Controller Prototype

