MI BPM Project

MI BPM TB Controller Status Report January 3rd, 2006, 9:30am

Hardware status

MI BPM_TB Controller Prototype:
-) Completed Prototype Schematic.
-) Prototype Layout to be completed today.
-) Parts order in progress tanks to Manfred WENDT help.
-) Quote request should be sent out today. We will try to submit board for manufacturing this week.

Interface with the MI BPM TB:
-) Assembled test fixture to allow interface between Avnet Xilinx card and MI_BPM_TB without need for a backplane or controller motherboard.

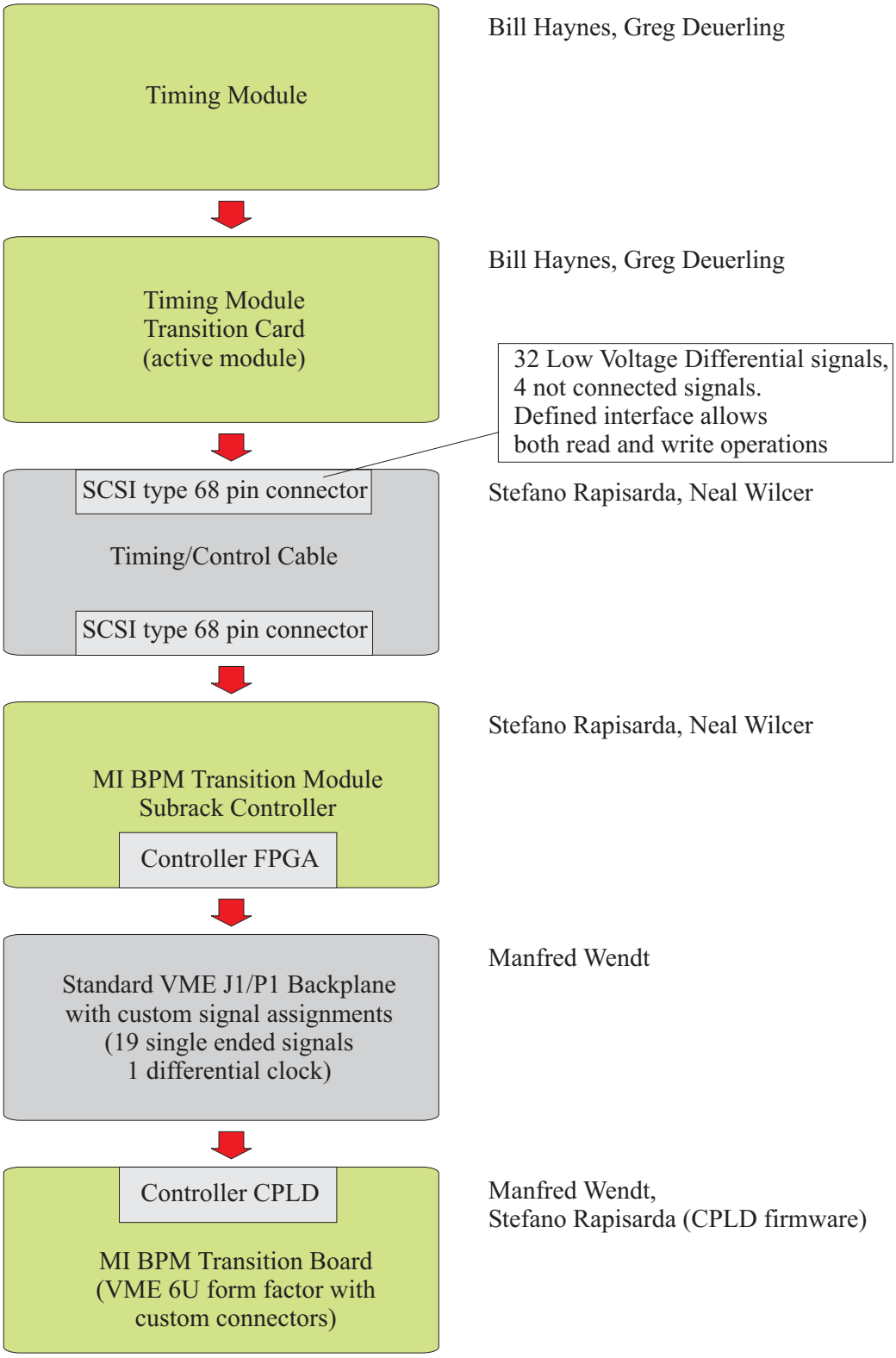
Firmware status:

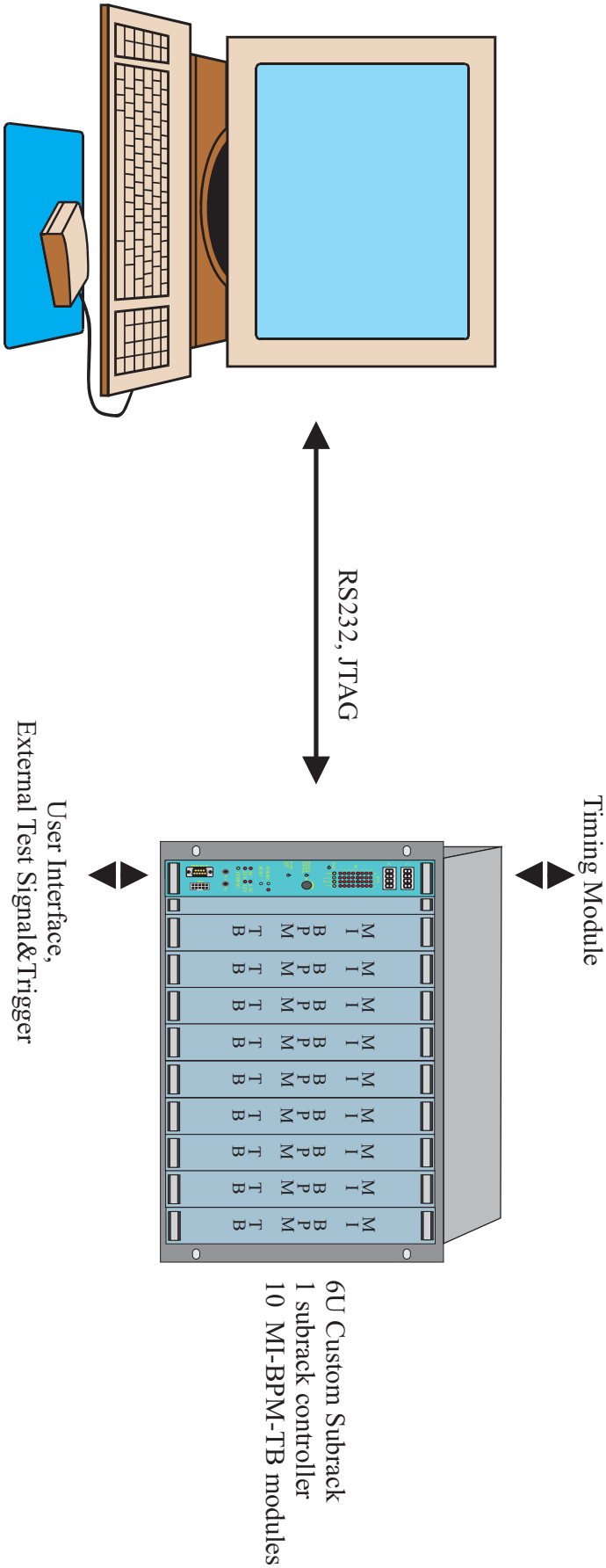
MI BPM_TB Firmware

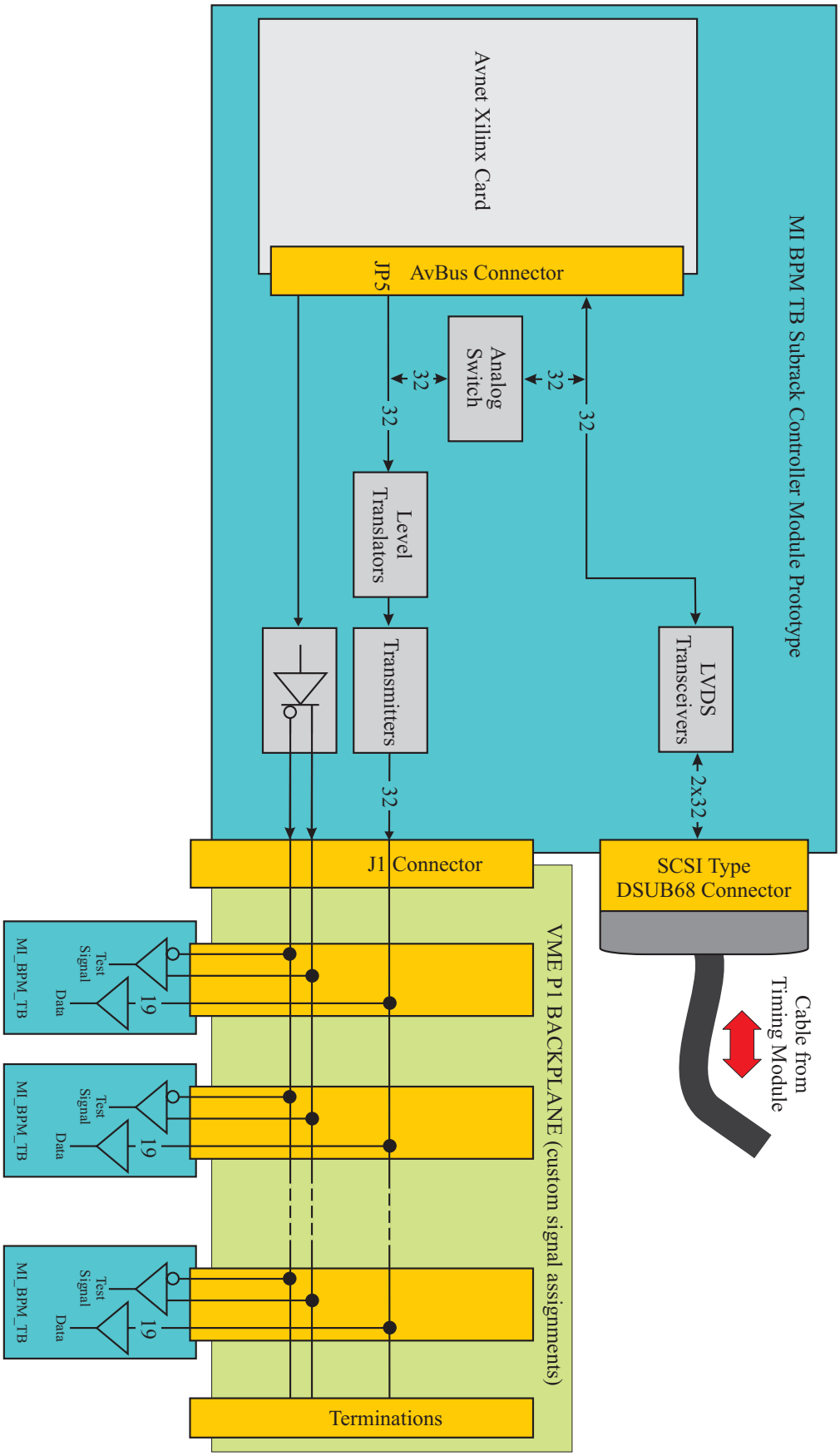
-) Firmware first release completed as specification. Allows for the MI_BPM_TB to be remotely controlled. External test signal needed.

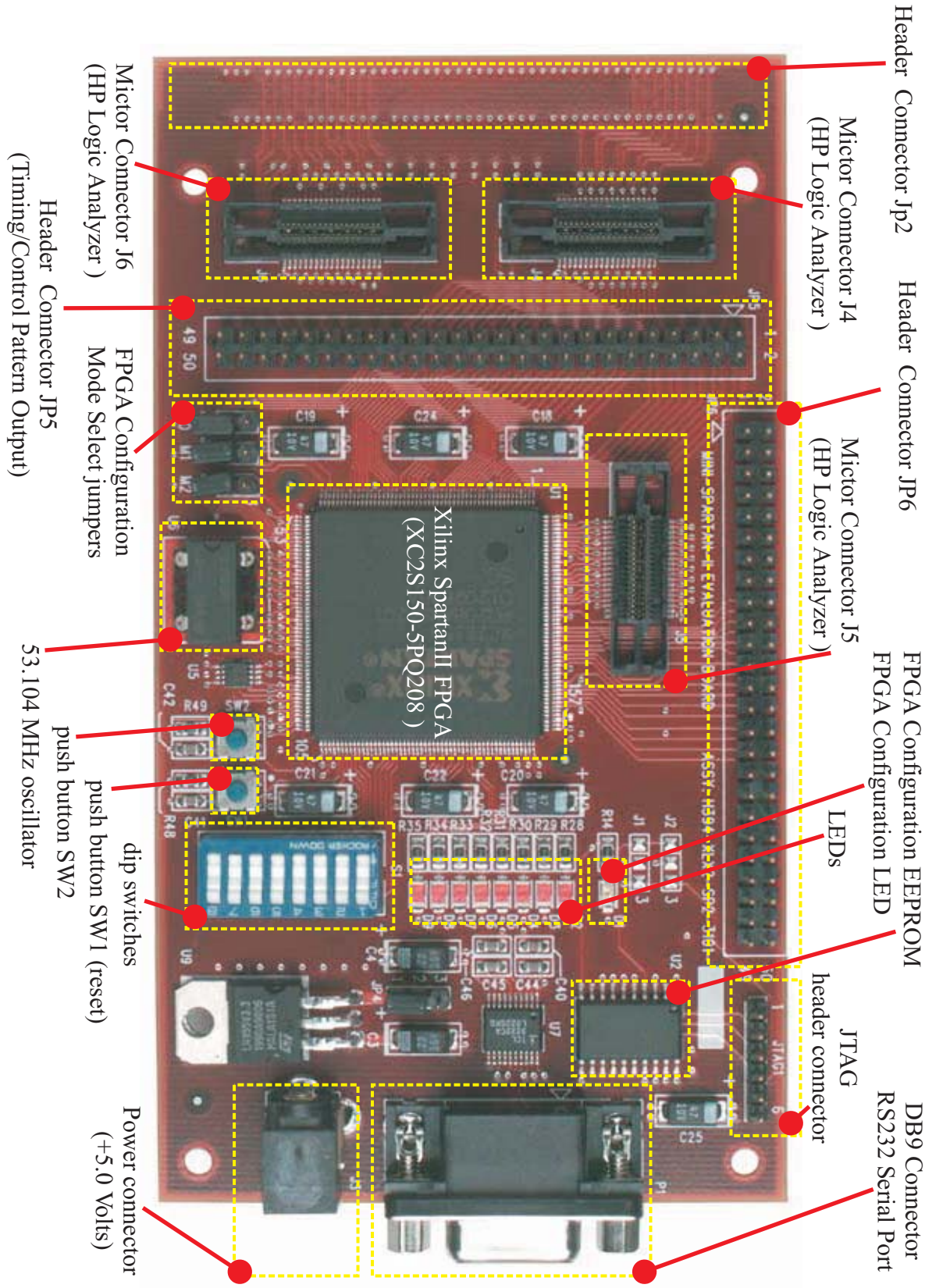
MI BPM_TB Prototype Firmware (Avnet Xilinx card)

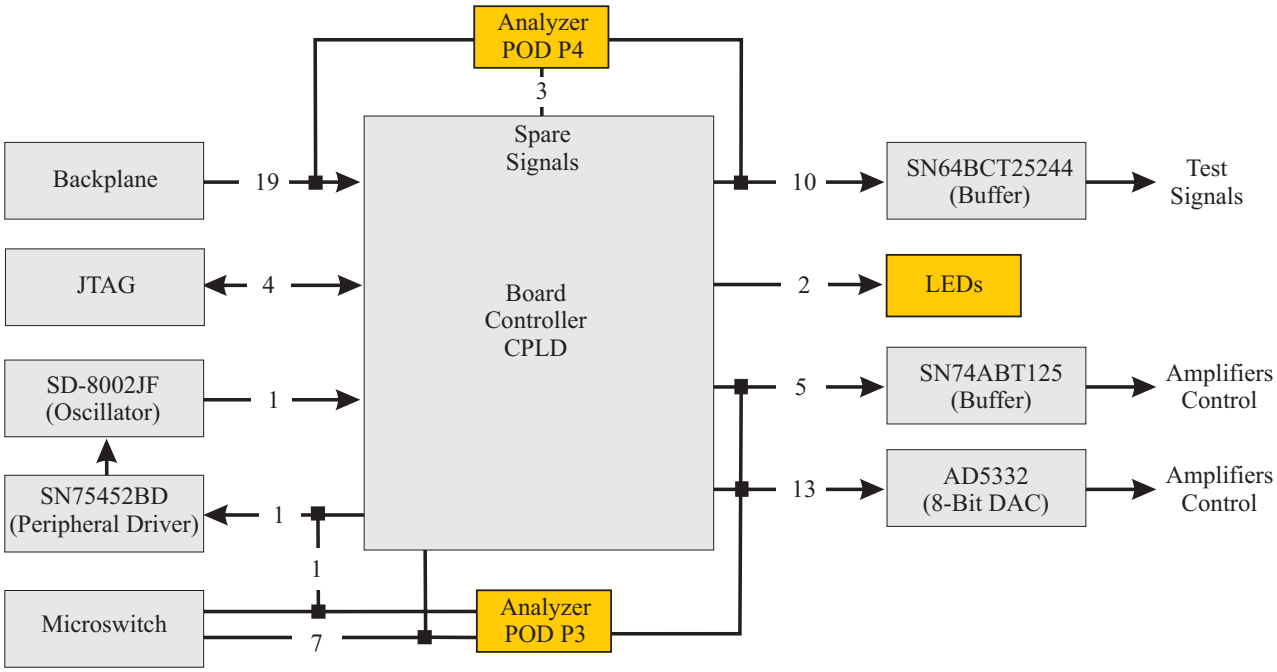
-) Implemented simplified interface with MI_BPM_TB. Tested successfully at FCC.

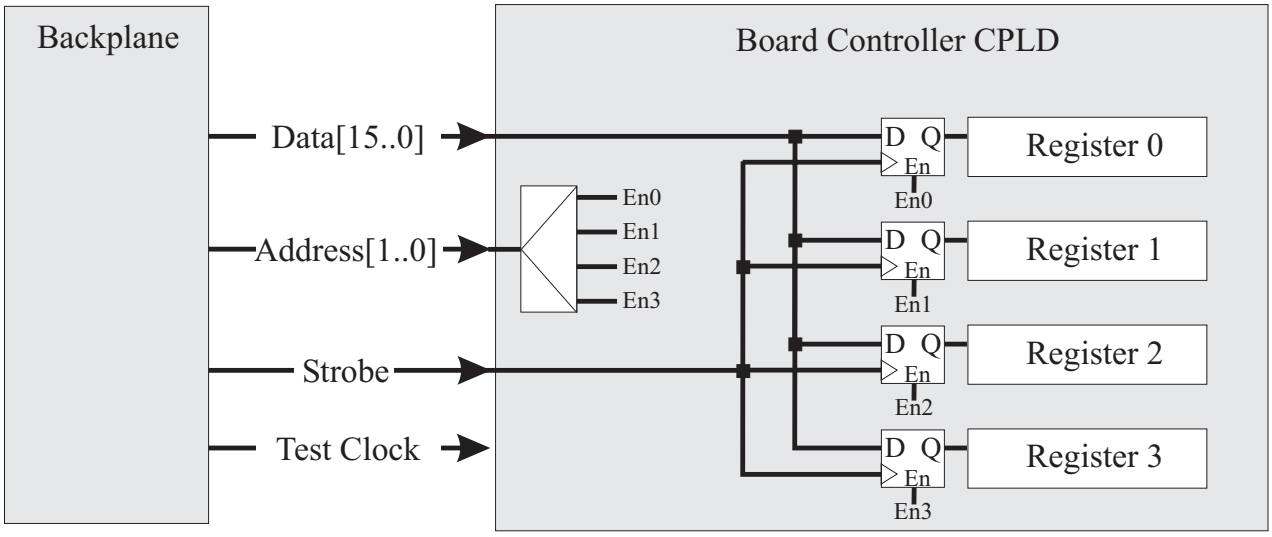

Timing Module
Bill Haynes, Greg Deuerling
Timing Module
Transition Card
(active module)
Bill Haynes, Greg Deuerling
32 Low Voltage Differential signals,
4 not connected signals.
Defined interface allows
both read and write operations
SCSI type 68 pin connector
Timing/Control Cable
SCSI type 68 pin connector
Stefano Rapisarda, Neal Wilcer
MI BPM Transition Module
Subrack Controller
Controller FPGA
Stefano Rapisarda, Neal Wilcer
Standard VME J1/P1 Backplane
with custom signal assignments
(19 single ended signals
1 differential clock)
Manfred Wendt
Controller CPLD
MI BPM Transition Board
(VME 6U form factor with
custom connectors)
Manfred Wendt,
Stefano Rapisarda (CPLD firmware)


Timing Module
RS232, JTAG
User Interface,
External Test Signal&Trigger
6U Custom Subrack
1 subrack controller
10 MI-BPM-TB modules


MI BPM TB Subrack Controller Module Prototype
Avnet Xilinx Card
AvBus Connector
JP5
32
Analog Switch
32
32
Level Translators
Transmitters
32
LVDS Transceivers
2x32
SCSI Type DSUB68 Connector
Cable from Timing Module
J1 Connector
VME P1 BACKPLANE (custom signal assignments)
Terminations
19
Test Signal
Data
MI_BPM_TB
19
Test Signal
Data
MI_BPM_TB
19
Test Signal
Data
MI_BPM_TB


Header Connector Jp2
Mictor Connector J4
(HP Logic Analyzer)
Header Connector JP6
Mictor Connector J5
(HP Logic Analyzer)
FPGA Configuration EEPROM
FPGA Configuration LED
LEDs
JTAG
header connector
DB9 Connector
RS232 Serial Port
Mictor Connector J6
(HP Logic Analyzer)
Header Connector JP5
(Timing/Control Pattern Output)
FPGA Configuration
Mode Select jumpers
53.104 MHz oscillator
push button SW2
push button SW1 (reset)
dip switches
Power connector
(+5.0 Volts)
Xilinx SpartanII FPGA
(XC2S150-5PQ208)


Analyzer POD P4
3
Spare Signals
Backplane
19
JTAG
4
SD-8002JF (Oscillator)
1
SN75452BD (Peripheral Driver)
1
1
Microswitch
7
Board Controller CPLD
Analyzer POD P3
10
SN64BCT25244 (Buffer)
Test Signals
2
LEDs
5
SN74ABT125 (Buffer)
Amplifiers Control
13
AD5332 (8-Bit DAC)
Amplifiers Control


Backplane
Data[15..0]
Address[1..0]
Strobe
Test Clock
Board Controller CPLD
En0
En1
En2
En3
D Q
En
Register 0
Register 1
Register 2
Register 3