Fermi National Accelerator Laboratory

Main Injector Electronics

Beam Position Monitor Transition Board Control Module Prototype

PRELIMINARY

Date: November 1st, 2005
Revision Date: February 19th, 2006

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Document # Beam-doc-2145-v3

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2 Introduction

This document specifies the Fermilab Main Injector Beam Position Monitor Transition-Board Control Module (MI-BPM-TB-CTL) Prototype. The MI-BPM-TB-CTL is part of the electronics of the Main Injector at Fermilab. More information on the experiments performed at Fermilab is available on the laboratory web page:
http://www.fnal.gov/

Documents describing the Main Injector Upgrade project are available in the Fermilab Accelerator Division Document Databases web page:
http://beamdocs.fnal.gov/

Documents describing the MI-BPM-TB-CTL module are available on the web page:
http://www-ese.fnal.gov/MI_BPM_TB_CTL/

The designers welcome suggestions and corrections [Ref.29], which can be addressed directly to the engineer responsible of the project. Contact information is available on the Electronics System Engineering (ESE) web page:
http://www-ese.fnal.gov/

3 Overview

The Main Injector Beam Position Monitor Transition-Board Control Module (MI-BPM-TB-CTL) Prototype is a custom designed module used in the Fermilab Main Injector (MI) system to control the Beam Positioning Monitoring (BPM) Transition Board (TB) subrack.

The MI BPM TB subrack receives timing and control information from the Timing Generator Fanout (TGF) module [Ref.28] and interfaces with the MI-BPM-TB [Ref.28] over a custom backplane.

4 BPM Transition Board and BPM system

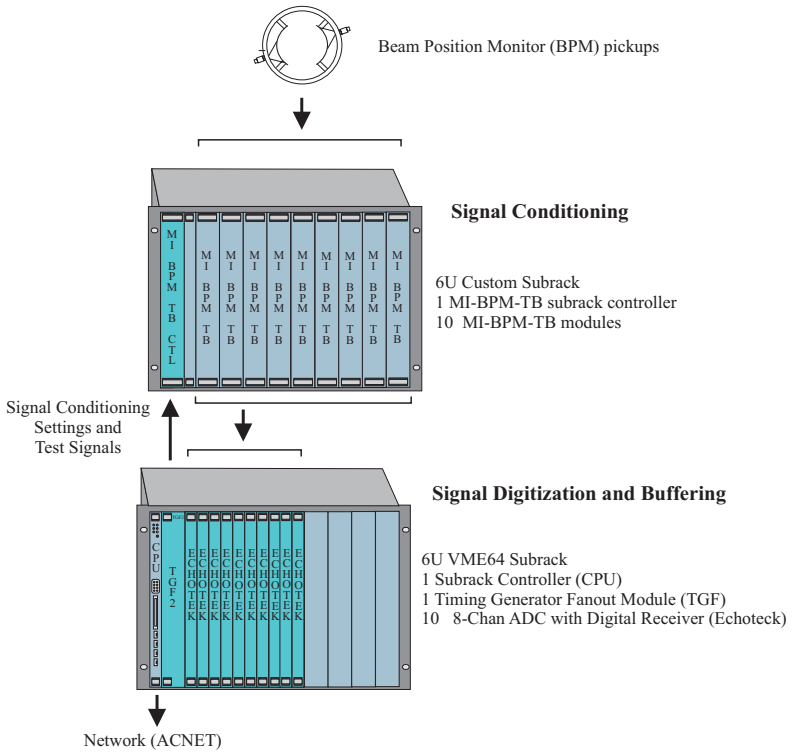

Figure 4.1, BPM Transition Board and BPM System

4.1 How the MI-BPM-TB Control Module fits into the MI BPM System

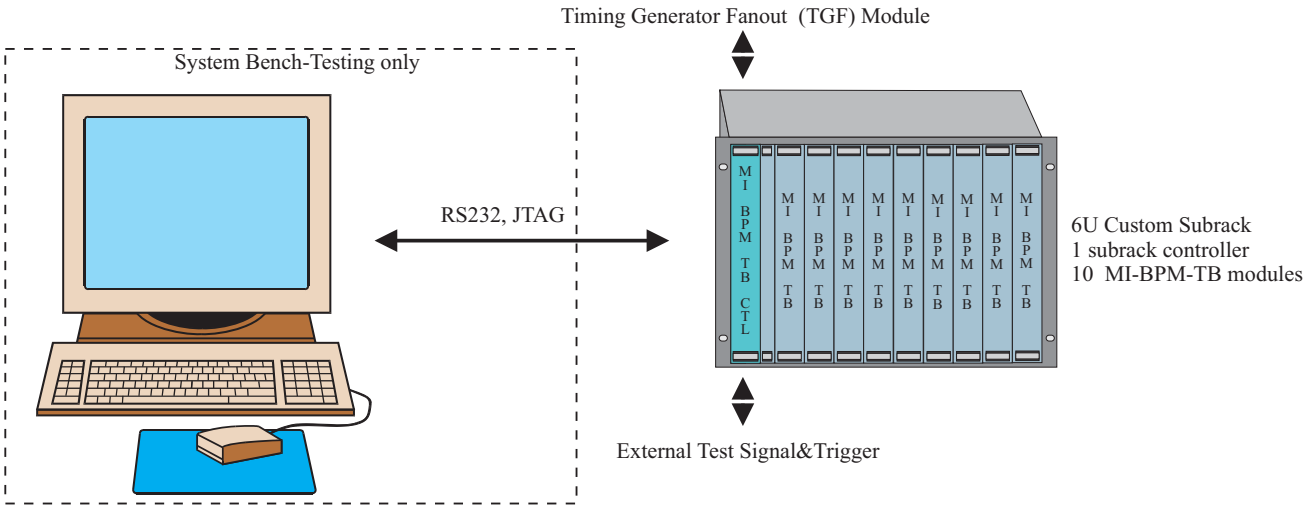

Figure 4.2, MI BPM TB System

4.2 Interfaces

The Control Module(MI-BPM-TB-CTL Prototype) supports the following interfaces:

Backplane Interface

Connects the module to a custom backplane used to communicate with the MI-BPM-TB modules. The backplane used is a standard VME J1/P1 backplane with non-standard signal assignments and power supply voltages.

The communications from the Control Module to the MI-BPM-TB modules are unidirectional. Test signals and commands are broadcasted by the Control Module over the backplane and no capability to address modules individually is provided.

Timing Module Interface

Unidirectional custom bus used to receive commands and timing from the Timing Module and to report subrack status. It is implemented on a SCSI type 68-pin connector located on the top back side of the MI-BPM-TB-CTL Prototype module.

Serial (RS232) interface

A connector provides access to the RS232 interface. The RS232 interface provides an additional access to the module logic for monitoring and debugging. The RS232 interface can be used for the module standalone operation (system bench testing) making unnecessary the need for a connection to the Timing Module.

External Test Signal & Trigger interface

Connectors provide the user with the capability to connect an external test signal source and an external trigger source directly to the MI-BPM-TB-CTL.

Power supply

The module is powered through a backplane connection to the 5.0 Volts subrack power supply. For stand-alone operations a module can be powered through an auxiliary connector. LEDs are used to indicate when the module is powered and what voltages are present. The module has its own over-current/over-voltage protection.

JTAG (IEEE 1149.1) interface

A four pin Test Access Port (TAP) provides access to the module card JTAG chain. The JTAG port is used for module FPGAs/EEPROMs configuration and diagnostic.

Logic Analyzer interface

For debugging/diagnostic purposes, the MI-BPM-TB-CTL has several connectors to fit the high-density adapter cables for Agilent 16550A logic analyzers.

4.3 MI BPM TB Control Module Prototype block diagram

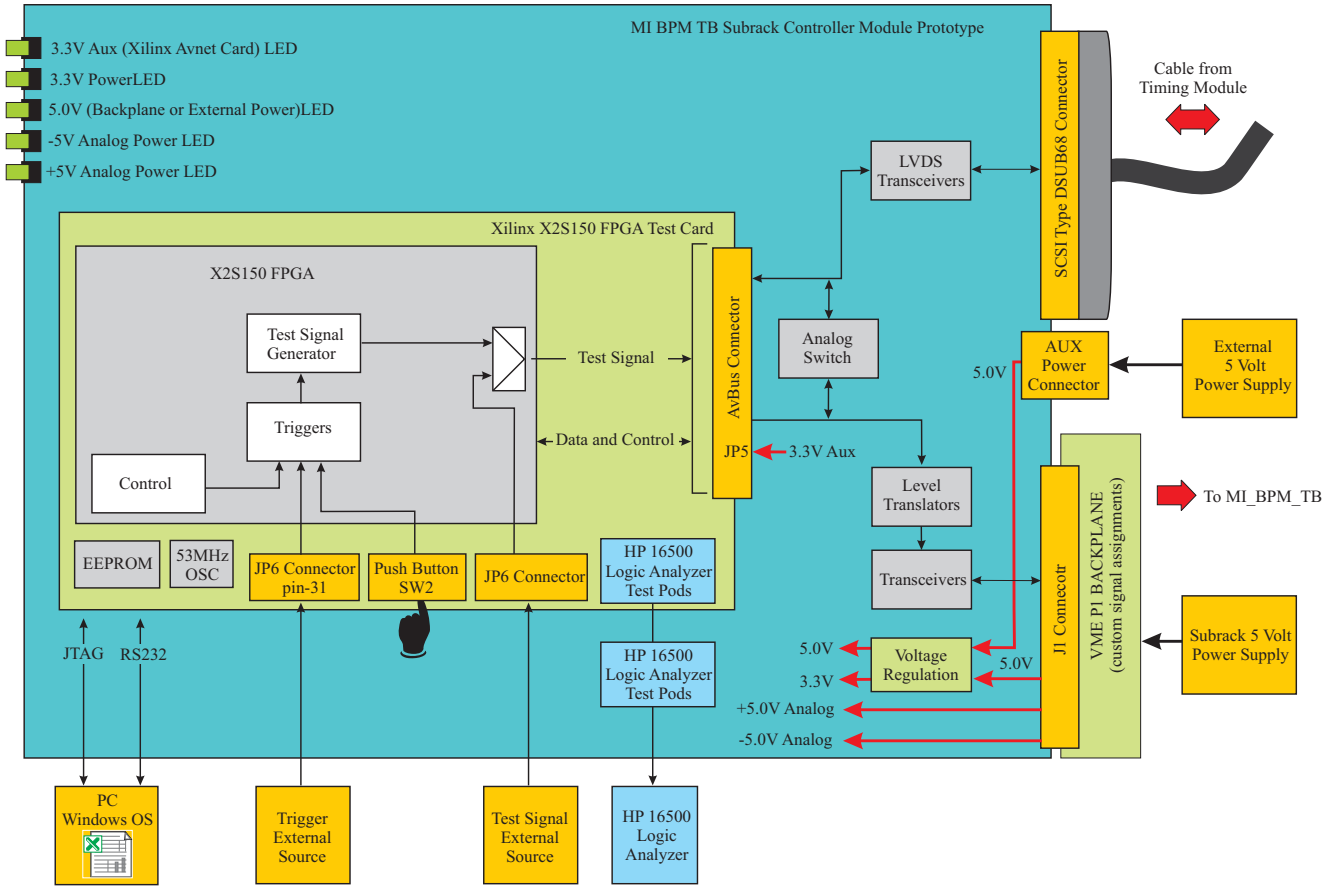

Figure 4.3, MI BPM TB Control Module Prototype block diagram

The MI BPM TB Control Module Prototype has been assembled using a custom designed module hereafter referred as "Control Module Prototype Motherboard" and a commercially available test card (Avnet [Ref.11] Xilinx [Ref.27] Spartan II evaluation card) hereafter referred as "Xilinx Avnet Card".

The Xilinx Avnet Card is used to interface the module with a PC over a serial port (RS232). A Graphical User Interface based on Microsoft Excel is used to communicate with the Control Module Prototype.

The PC is also used to reprogram the Xilinx Avnet Card FPGA's configuration EEPROM with the use of a Xilinx JTAG cable.
The FPGA on the Xilinx Avnet Card provides the memory and the controls used to receive commands from the Timing Module and to generate the commands for the MI_BPM_TBs.

The Xilinx Avnet Card provides the MI-BPM-TB-CTL Prototype for additional diagnostics capabilities but is not needed for interfacing directly the Timing Module with the MI-BPM-TBs (pass-through mode).

If the Avent Xilinx Card is not installed the Control Module Prototype Motherboard design is such that it goes automatically into pass-through mode.

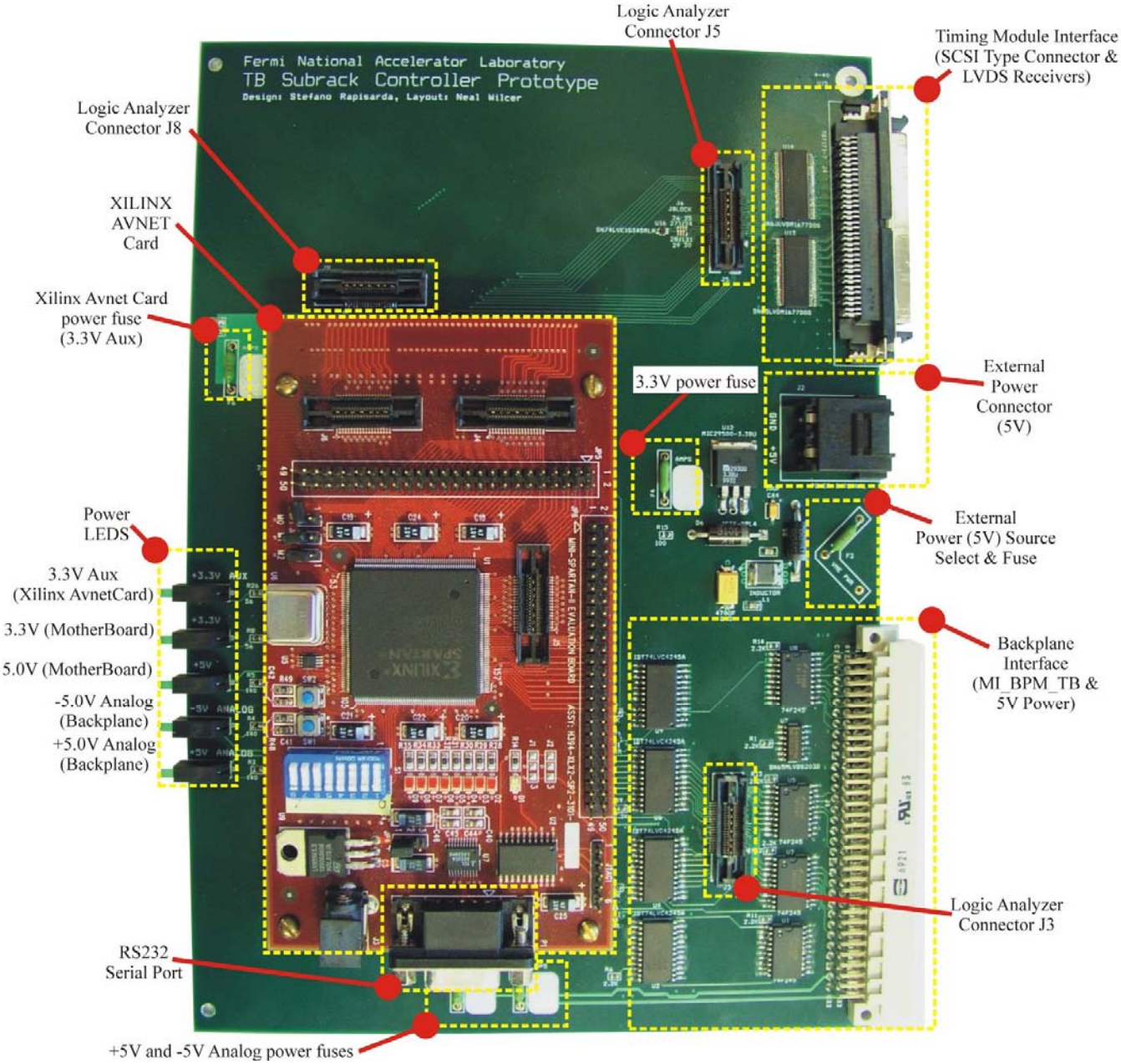

Figure 4.4, MI BPM TB Control Module Prototype (motherboard and Xilinx Avnet card)

5 MI-BPM-TB Control Module Prototype Motherboard

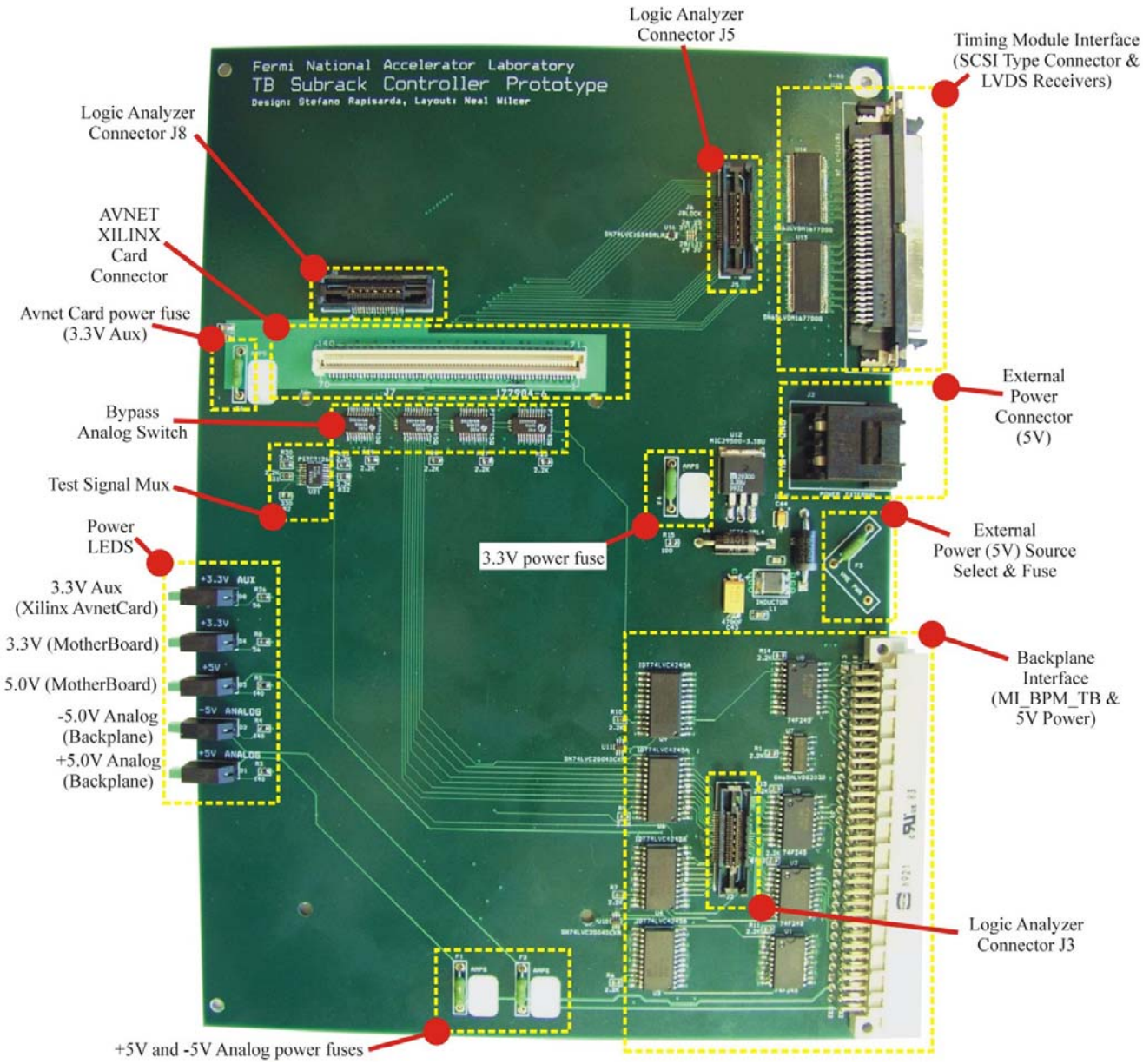

Figure 5.1, Control Module Prototype Motherboard only

5.1 Interface with the Timing Module

Pinout of the Timing Module Interface connector is provided in Appendix B (Page 37).

Signal	Notes
FECTL[0]	Reserved (not mapped to TB)
FECTL[16..1]	Data[15..0] (mapped to TB)
FECTL[17]	Data Strobe (mapped to TB)
FECTL[19..18]	Address[1..0] (mapped to TB). See Table 5.2.
FECTL[21..20]	Reserved[1..0] (mapped to TB). Driven low.
FECTL[27..22]	Reserved[5..0] (not Mapped to TB). Driven low.
FECTL[28]	Data Bus Direction (not Mapped to TB).
FECTL[30..29]	Reserved[1..0] (not Mapped to TB).
FECTL[31]	Test Signal (mapped to TB).

Table 5.1, Timing Module Interface signal assignments

Address bus is 2 bit wide. Address bits are: FECTL[19..18]		
MSB, FECTL[16..9]	LSB, FECTL[8..1]	Address
MI BPM TB control register 0		0x0
MI BPM TB control register 1		0x1
MI BPM TB control register 2		0x2
MI BPM TB control register 3		0x3

Table 5.2, Timing Module Interface Address Space Mapping

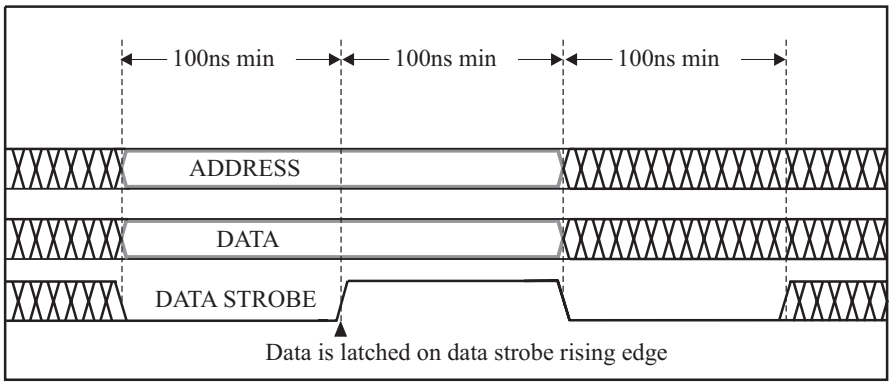

Figure 5.2, Timing Module Interface Protocol

Figure 5.3, Timing Module Interface Cable [Ref.10]

5.2 Interface with the Xilinx Avnet Card

The MI-BPM-TB CTL Prototype Motherboard interfaces with the Xilinx Avnet card over a 140-pin connector (J7, AvBus). AvBus is a custom bus defined by Avnet [Ref.11] and used for interfacing evaluation modules, AvBus Connector pinout is provided in Appendix C (page 43).

The Xilinx Avnet Card is powered (3.3V Aux) through the J7 AvBus connector.

The Xilinx Avnet Card uses the signals on the J7 AvBus connector to control the motherboard digital logic and the dataflow between the Timing Module and the MI BPM TB Modules.

5.3 Backplane Interface

Backplane connector pinout is provided in Appendix B (Page 28).

The backplane interface is implemented using standard VME P1 backplane with custom pin assignments. The interface is implemented using a multidrop scheme.

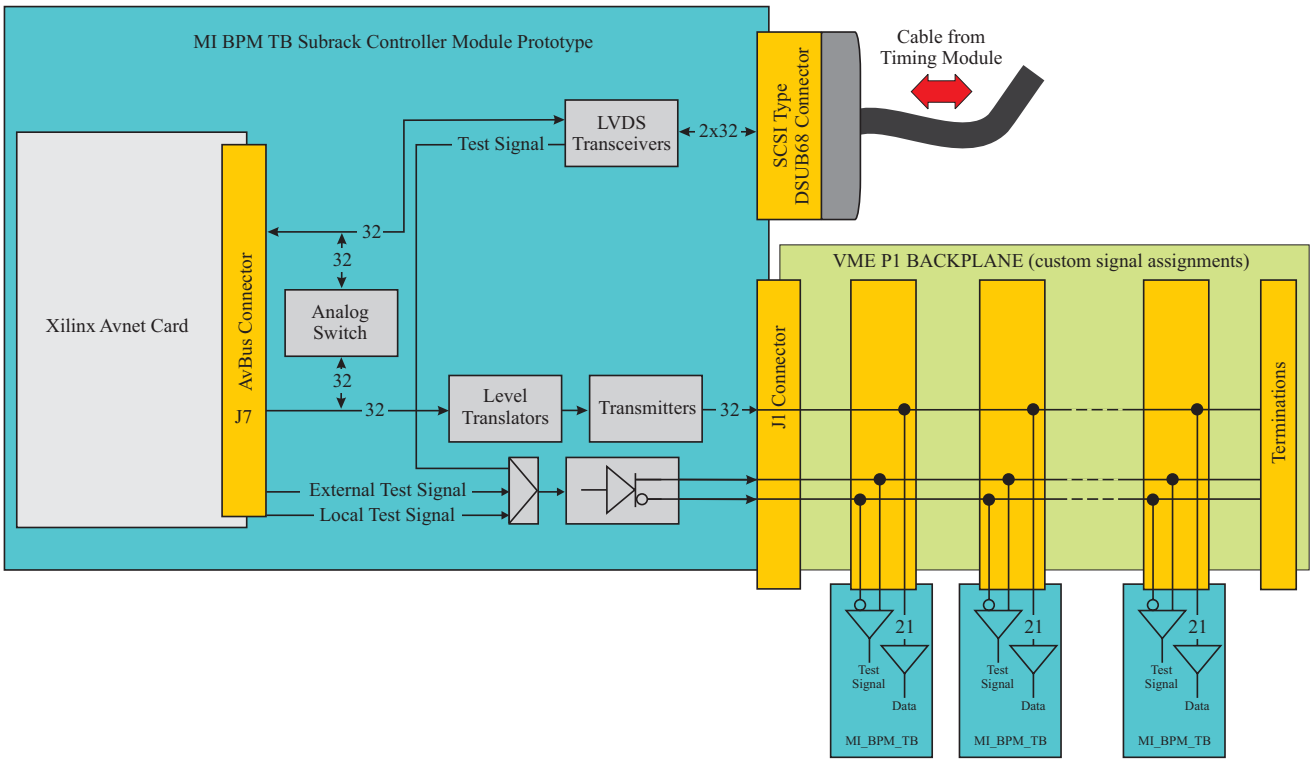

Figure 5.4, Backplane Interface

5.4 Power supply

The MI BPM TB System use a standard VME P1 backplane with custom pin assignments.

The VME standard defines, via the J1/P1 connector, three pins of +5V. The standard VME backplane connector has also 1 pin that supplies +12V, and 1 pin that provide –12V. Each pin is rated for 1.5 amps.

The MI BPM TB CTL Prototype module is powered only by the +5V pins.

The +12V and the -12V pins are used in the MI BPM TB System to provide the +5V and -5V analog power. These two "analog power" pins are used by the MI BPM TB CTL to power two "power status" LEDs on the front panel.

The MI BPM TB CTL Prototype module also has a Molex style power connector to allow for standalone operations with a +5V power supply.

The MI BPM TB CTL Prototype module design DOES NOT ALLOW for operation in a standard VME 6U subrack.

Fuse Identifier	Fuse Value	Notes
F1	0.5 Amp	+5 Volt Analog power
F2	0.5 Amp	-5 Volt Analog power
F3	3 Amp	External Power or Backplane Power. The fuse has two possible positions, allowing the user to select which of the two power source is used.
F4	3 Amp	3.3 Volt Digital Logic.
F6	2 Amp	3.3 Volt Aux. Powers the Xilinx Avnet Card over the J7 AvBus connector.

Table 5.3, MI BPM TB CTL Prototype fuse values

5.5 Logic Analyzer Connectors

For debugging/diagnostic purposes the MI-BPM-TB-CTL Prototype module has six Amp [Ref.8] "Mictor 38" connectors (AMP 2-767004-2) to fit the Agilent (formerly HP) [Ref.5] High Density adapter cables (Agilent E5346A). Each adapter cable fits two test pods of an Agilent 16550A Logic Analyzer allowing monitoring of up to 38 signals. Three Logic Analyzer Connectors are on the Control Module Prototype Motherboard and three are on the Xilinx Avnet Card.

6 Xilinx Avnet Card

The Xilinx Avnet Card used is the one provided in the Avnet [Ref.11] Spartan II Evaluation Kit (Avnet part number: ADS-XLX-SP2-EVL).

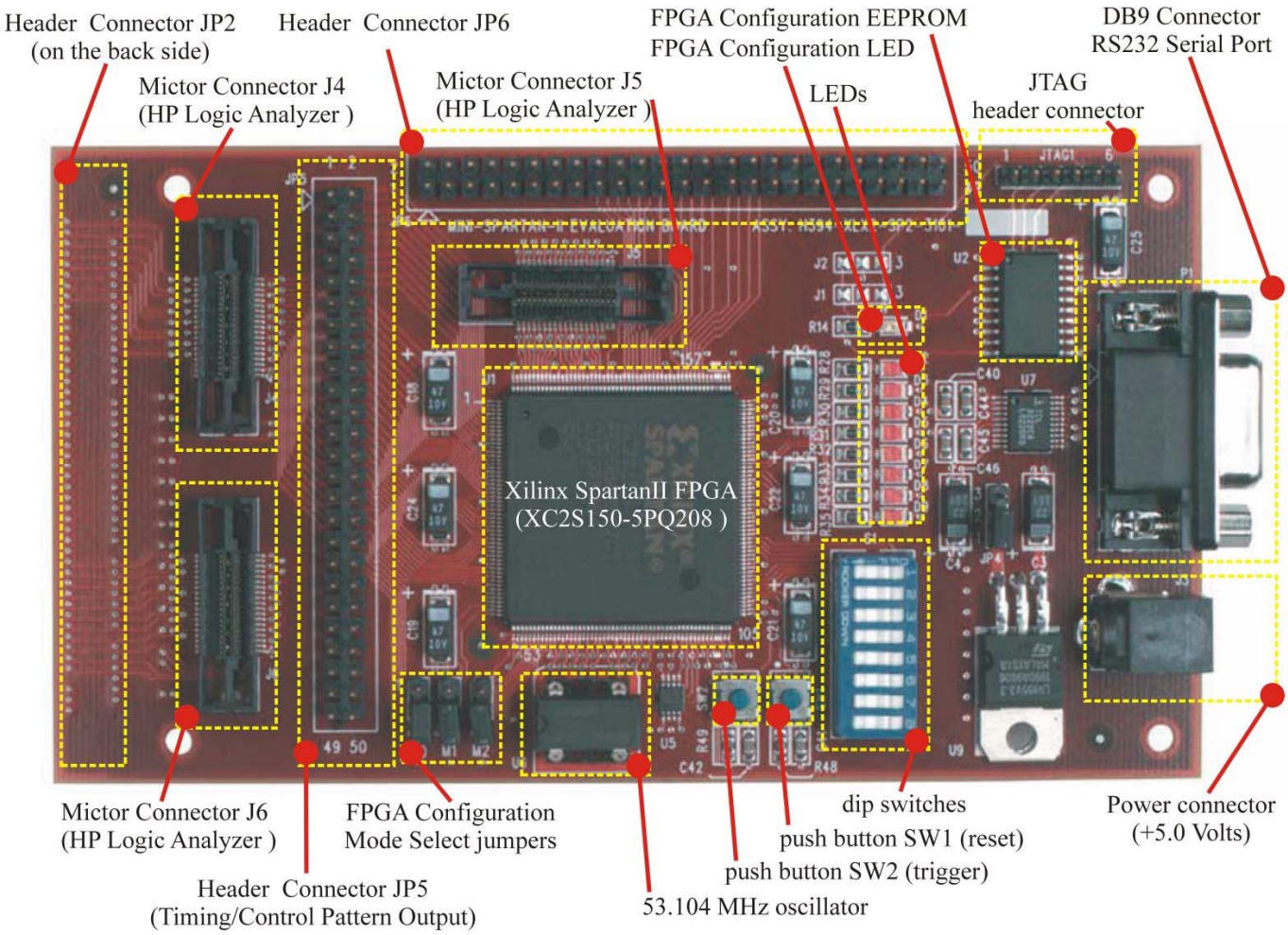

Figure 6.1, Xilinx Avnet Card (Spartan II Evaluation kit).

The Spartan II evaluation kit is supplied with VHDL source code. The code has been rewritten in order to meet the MI-BPM-TB CTL Prototype needs.

6.1 Memory Mapping

The memory space inside the Xilinx FPGA is implemented in locations two bytes wide. Each location is identified by a two-byte address (0x0000 to 0xFFFF). The memory is read/write accessible through the serial port interface specified in Section 6.2 (page 19).

For convenience the memory can be considered as partitioned in blocks, with the block number specified by the most significant 4 bits of the 16-bit address word. Currently only three of the 16 possible blocks are used. Block 0 is used for the board control/status registers. Block 1 and block 2 are assigned respectively to store the data received from the Timing Module (Timing Module data memory buffer) and channel 2 to store the data sent to the MI BPM TB over the backplane (MI BPM TB data memory buffer).

Block address	Row address		
bits 15..12	bits 11..8	bits 7..4	bits 3..0

Figure 6.2, Address format

Both data memory buffers use the rows from 0x000 to 0x3FF to map the 16 bit wide "block RAM" locations (1024 words deep).

Board Block 0x0				Timing Module data memory buffer Block 0x1				MI BPM TB data memory buffer Block 0x2				
MSB		LSB		MSB		LSB		MSB		LSB		Row
15..12	11..8	7..4	3..0	15..12	11..8	7..4	3..0	15..12	11..8	7..4	3..0	
Board Memory block See Table 6.2												0x000
												0x001
												• • •
												0x3FE
												0x3FF
												• • • • • •
												0xFFF

Table 6.1, Xilinx Avnet Card Memory map

Board Block 0x0				
MSB		LSB		Row
15..12	11..8	7..4	3..0	
Board control/status register 0				0x000
Board control/status register 1				0x001
				•
				•
				•
Board control/status register 15				0x00F
Timing Module Data Memory Buffer control/status register 0				0x010
Timing Module Data Memory Buffer control/status register 1				0x011
				•
				•
				•
Timing Module Data Memory Buffer control/status register 15				0x01F
MI BPM TB Data Memory Buffer control/status register 0				0x020
MI BPM TB Data Memory Buffer control/status register 1				0x021
				•
				•
				•
MI BPM TB Data Memory Buffer control/status register 15				0x02F
				•
				•
				•
				•
				•
				0xFFF

Table 6.2, Xilinx Avnet Card - Board Memory Block map

6.1.1 Board Control/Status registers

Register	Address	Notes
Control/Status 0	0x0000	MI BPM TB Modules Mapped Register 0
Control/Status 1	0x0001	MI BPM TB Modules Mapped Register 1
Control/Status 2	0x0002	MI BPM TB Modules Mapped Register 2
Control/Status 3	0x0003	MI BPM TB Modules Mapped Register 3
Control/Status 4	0x0004	
Control/Status 5	0x0005	
Control/Status 6	0x0006	
Control/Status 7	0x0007	
Control/Status 8	0x0008	
Control/Status 9	0x0009	
Control/Status 10	0x000A	
Control/Status 11	0x000B	
Control/Status 12	0x000C	
Control/Status 13	0x000D	
Control/Status 14	0x000E	Module Serial Number and Firmware Revision Code
Control/Status 15	0x000F	Firmware Revision Date

Table 6.3, Board Control/Status registers

6.1.1.1 Board Control/Status register 0, 1, 2, 3 (MI BPM TB Mapped register)

These registers are mapped to the MI BPM TB Modules registers. Each time one of these registers is accessed in writing the content is sent over the backplane and written to the corresponding MI BPM TB register. See Section 7.2 (page 25) for MI BPM TB Modules registers description.

6.1.1.2 Board Control/Status register 14 (Module Serial Number and Firmware Revision Code)

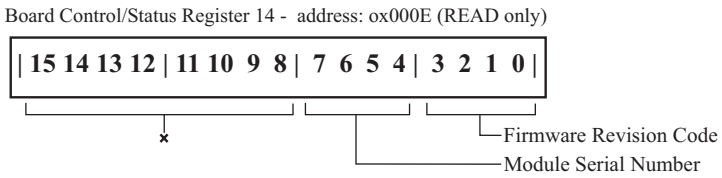

Figure 6.3, Board Control/Status register 14

Bit#	Name (Type)	Interpretation
15..8	--	Not Used
7..4	Module Serial Number	
3..0	Firmware Revision Code	

Table 6.4, Board Control/Status register 14.

6.1.1.3 Board Control/Status register 15 (Firmware Revision Date)

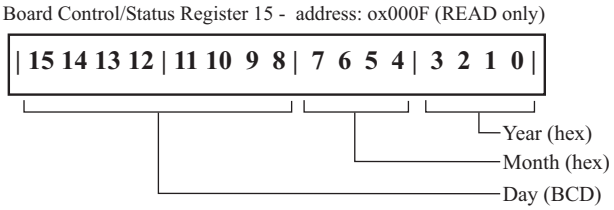

Figure 6.4, Board Control/Status register 15

Bit#	Name (Type)	Interpretation
15..8	Day	Day of the month, BCD coded.
7..4	Month	Month, hex coded.
3..0	Year	Year last digit, hex coded.

Table 6.5, Board Control/Status register 15

6.2 Serial Port Interface

A Universal Asynchronous Receiver/Transmitter (UART) is implemented in the Xilinx Avnet Card FPGA. The Xilinx Avnet Card uses an Analog Devices ADM3222 as RS-232 transceiver. The UART allows interfacing the card with a computer having a serial port. The module behaves like a Data Communication Equipment (DCE) with adjustable settings.

The default settings are: BAUD rate 115200, 1 start bit, 2 stop bits, no parity and no handshake. The serial interface is used for diagnostic purposes.

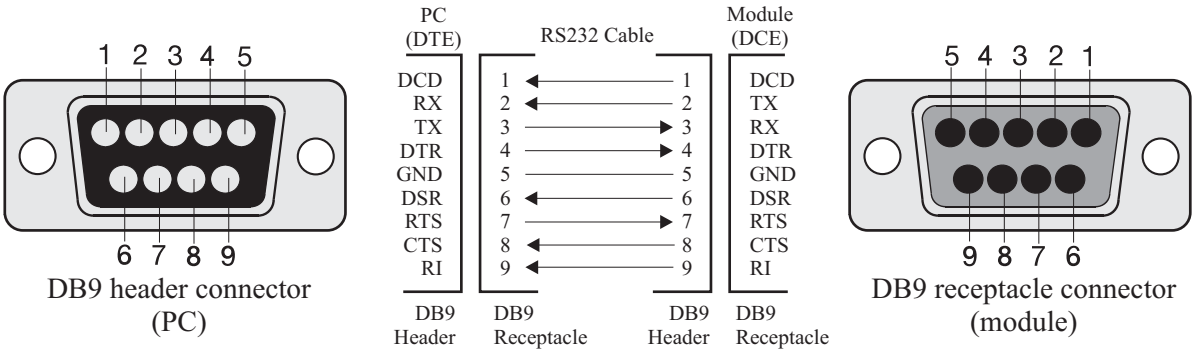

Figure 6.5, RS232 Interface

6.3 Logic Analyzer Connectors

For debugging/diagnostic purposes the Xilinx Avnet Card has three Amp [Ref.8] "Mictor 38" connectors (AMP 2-767004-2) to fit the Agilent (formerly HP) [Ref.5] High Density adapter cables (Agilent E5346A). Each adapter cable fits two test pods of an Agilent 16550A Logic Analyzer allowing monitoring up to 38 signals. Three tables in Appendix C (page 43) list the signals connected to the Xilinx Avnet Card's logic analyzer connector.

6.4 Header Connectors

The Xilinx Avnet Card has two 25x2 Header connectors.

Two tables in Appendix C (page 43) provide the pinouts of the Xilinx Avnet Card's header connectors.

6.5 AVBUS 140-pin Connector

The Xilinx Avnet Card has one 140 pin connector. The connector implements the AVBUS custom bus defined by Avnet as interface to their development systems. The connector is a AMP [Ref.8] 0.8mm Free Height Receptacle (AMP part number 5-179010-6) and is compatible with AMP 0.8mm Free Height plugs connectors (AMP part numbers: 177984-6, 179029-6, 179030-6, 179031-6).

Two tables in Appendix C (page 43) provide the pinout of the AvBus connector.

6.6 JTAG Interface

See a description of JTAG in Section 10 (Page 50, Glossary). One four pin Test Access Port (TAP) is provided on the Xilinx Avnet Card, it accesses the Xilinx FPGA and its configuration EEPROM [Ref.27].

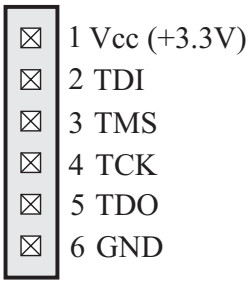

Figure 6.6, Xilinx Avnet Card - JTAG Connectors pinout

JTAG Chain#1, connector CON3		
Device #	Device Type	Notes
1	XC18V01SO20C	In-System-Programmable Configuration PROM.
2	XC2S150-5PQ208C	Spartan II FPGA

Table 6.6, Xilinx Avnet Card - JTAG Chain Devices

6.7 Board switches/buttons mapping

The dip-switches on the test board allow the selection of which signals are used to drive the set of 8 LEDs. The two buttons are used one for reset and the other as trigger.

Name used in the firmware	PCB Name	Standard Setting	Notes
SWITCH[3..0]	S1 switch[4..1]		Used to select the signals driving the LEDs 0000 LED scan 0001 Temperature 0010 RS232 Receiver (received data) 0011 RS232 Transmitter (data driving the transmitter input) 0100 Command Error Word lower byte 0101 Command Error Word upper byte 0110 Board Control/Status Register 0 lower byte 0111 Board Control/Status Register 0 upper byte 1000 1001 1010 1011 1100 1101 1110 1111
SWITCH[4]	S1 switch[5]	OFF	Internal Test Signal Select ON: 53 MHz, OFF 2.5 MHz.
SWITCH[5]	S1 switch[6]		
SWITCH[7..6]	S1 switch[8..7]	ON, ON	Test Signal Source Select 00 GND 01 FPGA Internal 10 External 11 Timing Module
SWITCH[8]	SW1 push button	N.A.	Reset button
SWITCH[9]	SW2 push button	N.A.	External Trigger.

Table 6.7, Board switches/buttons mapping.

7 Appendix A - MI BPM Transition Board

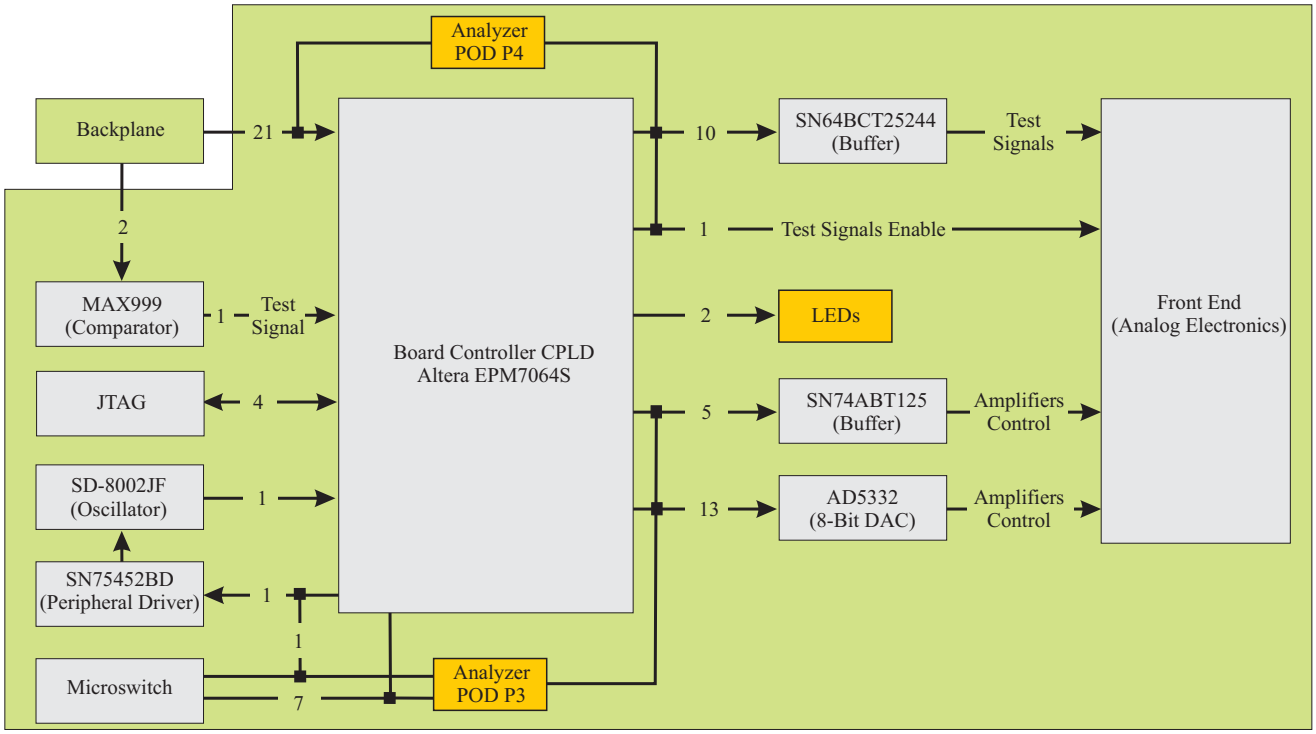

Figure 7.1, MI BPM TB digital section block diagram

7.1 Front End Interface on the MI BPM TB

Amplification Stages

CPLD Signal	Notes
ENB_53	Used to enable the 53MHz amplifiers gain stage. Driven by the Altera CPLD. Controls the power down (/PD) signal on the AD8129/30 in the 53MHz gain stage. High: 53MHz stage ON, Low: 53MHz stage OFF.
ENB_25	Used to enable the 2.5MHz amplifiers gain stage. Driven by the Altera CPLD. Controls the power down (/PD) signal on the AD8130 in the 2.5MHz gain stage. High: 2.5MHz stage ON, Low: 2.5MHz stage OFF.
HILO_53	Select the gain of the 53MHz VGA post-amp. Driven by the Altera CPLD. Controls the power down (/PD) signal on the AD8332 in the 53MHz gain stages. High: high gain, Low: low gain.
HILO_25	Select the gain of the 2.5MHz VGA post-amp. Driven by the Altera CPLD. Controls the power down (/PD) signal on the AD8332 in the 2.5MHz gain stages. High: high gain, Low: low gain.
nCTL_OE	Controls the output enable of the buffer (SN74ABT125) for the signals ENB_53, ENB_25, HILO_53, HILO_25. Driven by the Altera CPLD. High: outputs disabled (high impedance), Low: outputs enabled.
GAIN_53	Analog signal 0 to 1 Volt. Is driven by the AD5332 DAC. Controls the gain of the 53MHz VGA.
GAIN_25	Analog signal 0 to 1 Volt. Is driven by the AD5332 DAC. Controls the gain of the 2.5MHz VGA
TESTA[4..1]	Channels of group A test signals. Driven by the Altera CPLD.
TESTB[4..1]	Channels of group B test signals. Driven by the Altera CPLD.
nTESTA_OE	Channels of group A test signals Output Enable control. Driven by the Altera CPLD. High: outputs disabled (high impedance), Low: outputs enabled.
nTESTB_OE	Channels of group B test signals Output Enable control. Driven by the Altera CPLD. High: outputs disabled (high impedance), Low: outputs enabled.
TEST_ENB	Output Enable of Test Signal Driver (front-end). High: outputs enabled, Low: outputs disabled.

Digital to Analog Converter

The Digital to Analog Converter chip (U68, AD5332) generates the GAIN_53 and GAIN_25 signals. The following table list the signals used to control the DAC.

CPLD Signal	Notes
DAC_DB[7..0]	DB[7..0]. 8-bit data word used to set VGA gain setting. The VGA stage (53MHz or 2.5MHz) is selected by A0. Driven by the Altera CPLD.
DAC_nCS	/CS . Chip select (active low). Driven by the Altera CPLD.
DAC_nWR	/WR. Write (active low). Driven by the Altera CPLD.
DAC_A0	A0. Address DAC A (GAIN25) or B (GAIN53). Driven by the Altera CPLD.
DAC_nCLR	/CLR. Clear (active low). Driven by the Altera CPLD.
DAC_nLDAC	/LDAC (active low). Driven by the Altera CPLD.
VrefA, VrefB	Reference voltage. Is set to 1Volt by an ADR510.
/PD	Power down (active low). Forced high wit direct connection to 5V.

Oscillator Control

The on-board oscillator can be turned off by the CPLD signal OSC_Control.

7.2 Backplane Interface on the MI BPM TB

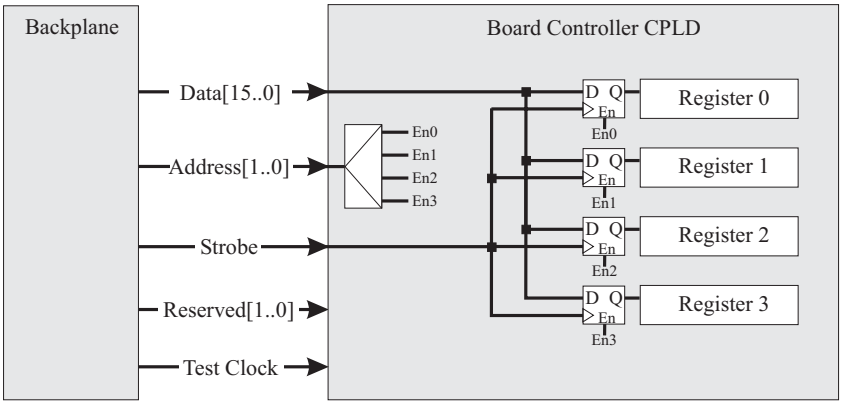

Figure 7.2, Backplane Interface Block Diagram

7.2.1 MI BPM TB Module Control Register 0

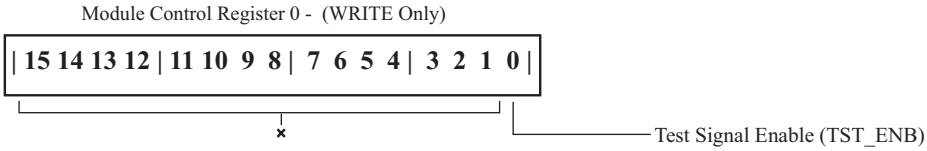

Figure 7.3, Module Control Register 0.

Signal	Notes
TST_ENB	**TST_ENB.** Test Signal Enable

Table 7.1, Module Control Register 0.

7.2.2 MI BPM TB Module Control Register 1

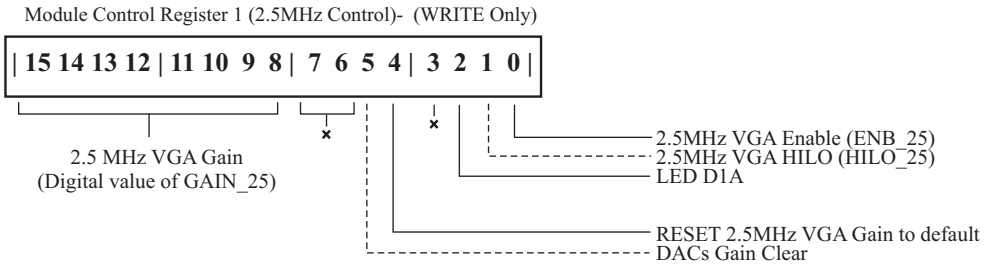

Figure 7.4, Module Control Register 1, 2.5 MHz VGA Control

Signal	Notes
2.5 MHz VGA Gain [7..0]	Digital value to generate **GAIN_25**. 8-bit data word used to set 2.5MHz VGA gain. The reference voltage used by the DAC is 1Volt. Default at power-up: 0 Volt = 00 hexadecimal = 0 decimal. Default after a "2.5 MHz VGA Gain Reset": 0.7 Volt = B3 hexadecimal = 179 decimal.
2.5 MHz VGA HILO	**HILO_25**. Selects gain of the 2.5MHz VGA post-amp. High: high gain, Low: low gain. Default: low gain.
2.5 MHz VGA EN	**ENB_25.** Enable the 2.5 MHz amplifier gain stages (controls the /PD power down signal of the AD8130s). High: enabled (ON), Low: disabled (OFF). Default: enabled.
2.5 MHz VGA Gain Reset	2.5 MHz VGA Gain to the default value: 0.7 Volt = B3 hexadecimal = 179 decimal.
DACs Gain Clear	Clears the gain value of both DACs. Controls the signal /CLR to the DAC (AD5332). High: CLEAR, Low: normal operations. Default: normal operations. After a CLEAR is issued the DACs will stay in CLEAR mode until this bit is set back to low.
LED D1A	Controls LED D1A (CALOnLED). High: ON, Low: OFF. Default: ON.

Table 7.2, Module Control Register 1, 2.5 MHz VGA Control

7.2.3 MI BPM TB Module Control Register 2

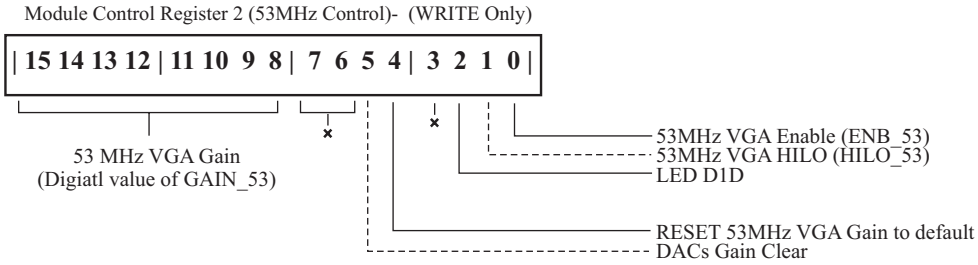

Figure 7.5, Module Control Register 2, 53 MHz VGA Control

Signal	Notes
53 MHz VGA Gain [7..0]	Digital value to generate **GAIN_53**. 8-bit data word used to set 53 MHz VGA gain. The reference voltage used by the DAC is 1Volt. Default at power-up: 0 Volt = 00 hexadecimal = 0 decimal. Default after a "53 MHz VGA Gain Reset": 0.3 Volt = 4D hexadecimal = 77 decimal.
53 MHz VGA HILO	**HILO_53.** Selects gain of the 53 MHz VGA post-amp. High: high gain, Low: low gain. Default: low gain.
53 MHz VGA EN	**ENB_53.** Enable the 53 MHz amplifier gain stages (controls the /PD power down signal of the AD8130s). High: enabled (ON), Low: disabled (OFF). Default: enabled.
53 MHz VGA Gain Reset	53 MHz VGA Gain to the default value: 0.3 Volt = 4D hexadecimal = 77 decimal.
DACs Gain Clear	Clears the gain value of both DACs. Controls the signal /CLR to the DAC (AD5332). High: CLEAR, Low: normal operations. Default: normal operations. After a CLEAR is issued the DACs will stay in CLEAR mode until this bit is set back to low.
LED D1D	Controls LED D1D. High: ON, Low: OFF. Default: ON.

Table 7.3, Module Control Register 2, 53 MHz VGA Control

7.2.4 MI BPM TB Module Control Register 3

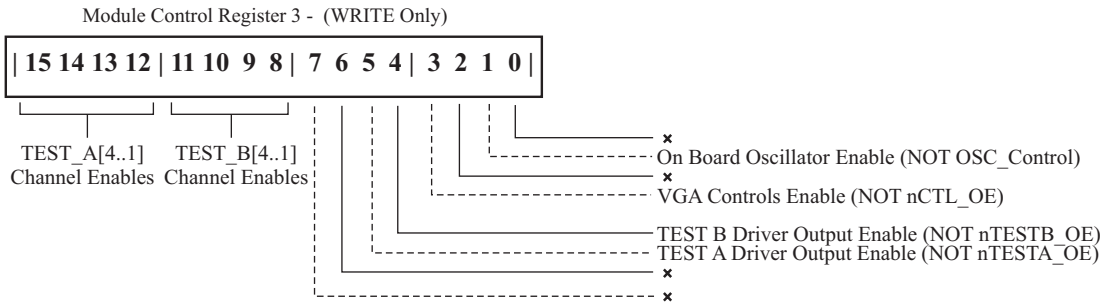

Figure 7.6, Module Control Register 3

Signal	Notes
VGA Controls EN	**nCTL_OE**. Controls the Output Enable of the buffer (U65, SN74ABT125) driving the control VGA signals. High: enabled, Low: disabled. Default: enabled.
TESTA_EN [4..1]	NOT **nTESTA_OE**. Enables test signal for channels A (A1, A2, A3, A4). High: enabled, Low: disabled. Default: enabled.
TESTB_EN [4..1]	NOT **nTESTB_OE**. Enables test signals for channels B (B1, B2, B3, B4). High: enabled, Low: disabled. Default: enabled.
TEST_A[4..1] Driver Output Enable	**TEST_A[4..1].** Channels of group A test signals Output Enable control. High: enabled, Low: disabled. Default: enabled.
TEST_B[4..1] Driver Output Enable	**TEST_B[4..1]**. Channels of group B test signals Output Enable control. High: enabled, Low: disabled. Default: enabled.
On Board Oscillator Enable	NOT **OSC_Control.** Enable the on-board 53MHz oscillator. High: enabled, Low: disabled. Default: disabled.

Table 7.4, Module Control Register 3

7.3 Backplane Interface - connectors pinout

The following table describes the pin assignment for connectors J1/P1 on a standard VME backplane interface. A second table describes the signals used by the MI-BPM-TB backplane connector. The MI-BPM-TB uses the J1/P1 backplane in a non-standard way. Beside using a custom signal assignments and voltages the J1/P1 backplane is positioned on the lower part of the subrack (were the J2/P2 backplane connector is in a standard VME subrack).

The signals highlighted in green are those used by the MI-BPM-TB and are connected to the module logic (Module Controller CPLD).

Pin#	Row A	Row B	Row C
1	D00 (Data Bus)	BBSY* (Bus Busy)	D08 (Data Bus)
2	D01 (Data Bus)	BCLR* (Bus Clear)	D09 (Data Bus)
3	D02 (Data Bus)	ACFAIL* (AC Power Fail)	D10 (Data Bus)
4	D03 (Data Bus)	BG0IN* (Bus Grant daisy-chain)	D11 (Data Bus)
5	D04 (Data Bus)	BG0OUT* (Bus Grant daisy-chain)	D12 (Data Bus)
6	D05 (Data Bus)	BG1IN* (Bus Grant daisy-chain)	D13 (Data Bus)
7	D06 (Data Bus)	BG1OUT* (Bus Grant daisy-chain)	D14 (Data Bus)
8	D07 (Data Bus)	BG2IN* (Bus Grant daisy-chain)	D15 (Data Bus)
9	GND (Ground)	BG2OUT* (Bus Grant daisy-chain)	GND (Ground)
10	SYSCLK	BG3IN* (Bus Grant daisy-chain)	SYSFAIL* (System Fail)
11	GND (Ground)	BG3OUT* (Bus Grant daisy-chain)	BERR* (Bus Error)
12	DS1* (Data Strobe)	BR0* (Bus Request)	SYSRESET* (System Reset)
13	DS0* (Data Strobe)	BR1* (Bus Request)	LWORD* (Long Word)
14	WRITE* (Read/Write)	BR2* (Bus Request)	AM5 (Address Modifier)
15	GND (Ground)	BR3* (Bus Request)	A23 (Address Bus)
16	DTACK* (Data Transfer Acknowledge)	AM0 (Address Modifier)	A22 (Address Bus)
17	GND (Ground)	AM1 (Address Modifier)	A21 (Address Bus)
18	AS* (Address Strobe)	AM2 (Address Modifier)	A20 (Address Bus)
19	GND (Ground)	AM3 (Address Modifier)	A19 (Address Bus)
20	IACK* (Interrupt Acknowledge)	GND (Ground)	A18 (Address Bus)
21	IACKIN* (Interrupt Acknowledge daisy-chain)	SERA (Serial Bus)	A17 (Address Bus)
22	IACKOUT* (Interrupt Acknowledge daisy-chain)	SERB (Serial Bus)	A16 (Address Bus)
23	AM4 (Address Modifier)	GND (Ground)	A15 (Address Bus)
24	A07 (Address Bus)	IRQ7* (Interrupt request)	A14 (Address Bus)
25	A06 (Address Bus)	IRQ6* (Interrupt request)	A13 (Address Bus)
26	A05 (Address Bus)	IRQ5* (Interrupt request)	A12 (Address Bus)
27	A04 (Address Bus)	IRQ4* (Interrupt request)	A11 (Address Bus)
28	A03 (Address Bus)	IRQ3* (Interrupt request)	A10 (Address Bus)
29	A02 (Address Bus)	IRQ2* (Interrupt request)	A09 (Address Bus)
30	A01 (Address Bus)	IRQ1* (Interrupt request)	A08 (Address Bus)
31	Power: -12V	Power: +5VSTDBY	Power: +12V
32	Power: +5V	Power: +5V	Power: +5V

Table 7.5. VME J1/P1 Pin Assignments

Pin#	Row A	Row B	Row C
1	Not Connected	Not Connected	Not Connected
2	Not Connected	Not Connected	Not Connected
3	Not Connected	Not Connected	Not Connected
4	Not Connected	Not Connected	Not Connected
5	Not Connected	Not Connected	Not Connected
6	Not Connected	Not Connected	Not Connected
7	Not Connected	Not Connected	Not Connected
8	Not Connected	Not Connected	Not Connected
9	GND (Ground)	Not Connected	GND (Ground)
10	Not Connected	Not Connected	Not Connected
11	GND (Ground)	Not Connected	Not Connected
12	pTest_Clock	Not Connected	Not Connected
13	nTest_Clock	Not Connected	Not Connected
14	Not Connected	Not Connected	Not Connected
15	GND (Ground)	Not Connected	Not Connected
16	Not Connected	Not Connected	Not Connected
17	GND (Ground)	Not Connected	BackplaneReserved01 (CPLD pin 46) (*)
18	Not Connected	Not Connected	BackplaneReserved00 (CPLD pin45) (*)
19	GND (Ground)	Not Connected	BackplaneAddress01 (CPLD pin 98)
20	Not Connected	GND (Ground)	BackplaneAddress00 (CPLD pin 97)
21	Not Connected	Not Connected	BackplaneStrobe (CPLD pin 96)
22	Not Connected	Not Connected	BackplaneData15 (CPLD pin 94)
23	Not Connected	GND (Ground)	BackplaneData14 (CPLD pin 93)
24	BackplaneData06 (CPLD pin 92)	Not Connected	BackplaneData13 (CPLD pin 85)
25	BackplaneData05 (CPLD pin 84)	Not Connected	BackplaneData12 (CPLD pin 83)
26	BackplaneData04 (CPLD pin 81)	Not Connected	BackplaneData11 (CPLD pin 80)
27	BackplaneData03 (CPLD pin 79)	Not Connected	BackplaneData10 (CPLD pin 76)
28	Backplane Data02 (CPLD pin 75)	Not Connected	BackplaneData09 (CPLD pin 71)
29	BackplaneData01 (CPLD pin 69)	Not Connected	BackplaneData08 (CPLD pin 68)
30	BackplaneData00 (CPLD pin 67)	Not Connected	BackplaneData07 (CPLD pin 48)
31	Power: -5V Analog	Not Connected	Power: +5V Analog
32	Power: +5V Digital	Power: +5V Digital	Power: +5V Digital

Table 7.6, MI-BPM-TB J1/P1 Pin Assignments

(*) Note: requires modification to MI BPM TB revision A modules. Design change has been applied to revision B modules.

7.4 MI-BPM-TB Logic Analyzer Connectors Pinout

The following tables list the signals connected to the MI-BPM-TB's logic analyzer connectors.

Notes	Schematic name	Pin #	Pin name	Pin name	Pin #	Schematic name	Notes
N.C.	N.C.	1	+5VDC	SCL	2	N.C.	N.C.
Ground	GND	3	GND	SDA	4	N.C.	N.C.
N.C.	N.C.	5	CLK1	CLK2	6	N.C.	N.C.
U68-20 (DB7)	(CPLD pin 16)	7	P1.15	P2.15	8	(CPLD pin 99)	SW1G
U68-17 (DB4)	(CPLD pin 20)	9	P1.14	P2.14	10	(CPLD pin 100)	U65-12 (4A)
U68-15 (DB2)	(CPLD pin 23)	11	P1.13	P2.13	12	(CPLD pin 6)	OSC Control U66-6&7, SW1H
SW1D	(CPLD pin 44)	13	P1.12	P2.12	14	(CPLD pin 8)	SW1F
SW1C	(CPLD pin 42)	15	P1.11	P2.11	16	(CPLD pin 9)	U65-9 (3A)
SW1B	(CPLD pin 41)	17	P1.10	P2.10	18	(CPLD pin 10)	U65-5 (2A)
SW1A	(CPLD pin 40)	19	P1.09	P2.09	20	(CPLD pin 12)	SW1E
LED D1D	(CPLD pin 37)	21	P1.08	P2.08	22	(CPLD pin 13)	U65-2 (1A)
N.C.	N.C.	23	P1.07	P2.07	24	(CPLD pin 14)	U65-1 (1/OE), -4 (2/OE), -10 (3/OE), -13 (4/OE)
N.C.	N.C.	25	P1.06	P2.06	26	(CPLD pin 36)	LED D1A (Cal ON)
N.C.	N.C.	27	P1.05	P2.05	28	(CPLD pin 30)	U68-10 (/LDAC)
N.C.	N.C.	29	P1.04	P2.04	30	(CPLD pin 29)	U68-13 (DB0)
U68-9 (/CLR)	(CPLD pin 31)	31	P1.03	P2.03	32	(CPLD pin 25)	U68-14 (DB1)
U68-8 (A0)	(CPLD pin 32)	33	P1.02	P2.02	34	(CPLD pin 21)	U68-16 (DB3)
U68-7 (/WR)	(CPLD pin 33)	35	P1.01	P2.01	36	(CPLD pin 19)	U68-18 (DB5)
U68-6 (/CS)	(CPLD pin 35)	37	P1.00	P2.00	38	(CPLD pin 17)	U68-19 (DB6)

Table 7.7, HP Logic Analyzer connector P3

Notes	Schematic name	Pin #	Pin name	Pin name	Pin #	Schematic name	Notes
N.C.	N.C.	1	+5VDC	SCL	2	N.C.	N.C.
Ground	GND	3	GND	SDA	4	N.C.	N.C.
N.C.	N.C.	5	CLK1	CLK2	6	N.C.	N.C.
Backplane connector P2-A26	(CPLD pin 81)	7	P1.15	P2.15	8	(CPLD pin 48)	Backplane connector P2-C30
Backplane connector P2-C25	(CPLD pin 83)	9	P1.14	P2.14	10	(CPLD pin 67)	Backplane connector P2-A30
Backplane connector P2-A25	(CPLD pin 84)	11	P1.13	P2.13	12	(CPLD pin 68)	Backplane connector P2-C29
Backplane connector P2-C24	(CPLD pin 85)	13	P1.12	P2.12	14	(CPLD pin 69)	Backplane connector P2-A29
Backplane connector P2-A24	(CPLD pin 92)	15	P1.11	P2.11	16	(CPLD pin 71)	Backplane connector P2-C28
Backplane connector P2-C23	(CPLD pin 93)	17	P1.10	P2.10	18	(CPLD pin 75)	Backplane connector P2-A28
Backplane connector P2-C22	(CPLD pin 94)	19	P1.09	P2.09	20	(CPLD pin 76)	Backplane connector P2-C27
Backplane connector P2-C21	(CPLD pin 96)	21	P1.08	P2.08	22	(CPLD pin 79)	Backplane connector P2-A27
Backplane connector P2-C20	(CPLD pin 97)	23	P1.07	P2.07	24	(CPLD pin 80)	Backplane connector P2-C26
Backplane connector P2-C19	(CPLD pin 98)	25	P1.06	P2.06	26	(CPLD pin 45)	Backplane connector P2-C18 (*)
U69-13 (/2OE)	(CPLD pin 52)	27	P1.05	P2.05	28	(CPLD pin 60)	U69-19 (1A4)
U69-14 (2A4)	(CPLD pin 54)	29	P1.04	P2.04	30	(CPLD pin 61)	U69-20 (1A3)
U69-15 (2A3)	(CPLD pin 56)	31	P1.03	P2.03	32	(CPLD pin 63)	U69-22 (1A2)
U69-17 (2A2)	(CPLD pin 57)	33	P1.02	P2.02	34	(CPLD pin 64)	U69-23 (1A1)
U69-18 (2A1)	(CPLD pin 58)	35	P1.01	P2.01	36	(CPLD pin 65)	U69-24 (/1OE)
TEST_ENB (*)	(CPLD pin 47)	37	P1.00	P2.00	38	(CPLD pin 46)	Backplane connector P2-C17 (*)

Table 7.8, HP Logic Analyzer connector P4

(*) Note: requires modification to MI BPM TB revision A modules.

7.5 MI-BPM-TB Module Controller CPLD Pinout

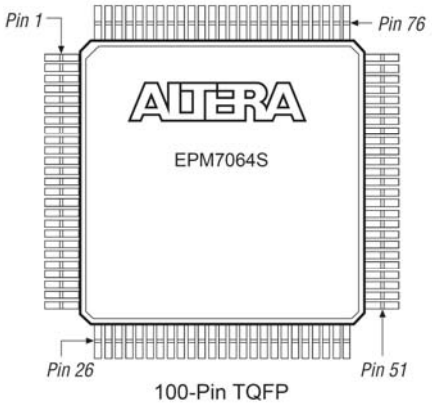

Figure 7.7, MI-BPM-TB Module Controller CPLD package

Color Legend	
	Not Connected
	Standard (User I/O)
	Power
	Ground
	JTAG

Pin #	Pin Function	Notes
1	No Connect (N.C.)	Dedicated pin.
2	No Connect (N.C.)	Dedicated pin.
3	VCCIO (3.3V or 5.0V)	Dedicated pin.
4	TDI/User I/O (LAB A)	Dedicated pin.
5	No Connect (N.C.)	Dedicated pin.
6	User I/O (LAB A)	Output. To U66-6&7 [OSC Control]
7	No Connect (N.C.)	Dedicated pin.
8	User I/O (LAB A)	SW1F. Analyzer Pod P3-14.
9	User I/O (LAB A)	U65-9 (3A). Analyzer Pod P3-16.
10	User I/O (LAB A)	U65-5 (2A). Analyzer Pod P3-18.
11	Ground	Dedicated pin.
12	User I/O (LAB A)	SW1E. Analyzer Pod P3-20.
13	User I/O (LAB A)	U65-2 (1A). Analyzer Pod P3-22.
14	User I/O (LAB A)	U65-1 (1/OE), U65-4 (2/OE), U65-10 (3/OE), U65-13 (4/OE). Analyzer Pod P3-24.
15	TMS/User I/O (LAB B)	Dedicated pin.
16	User I/O (LAB B)	U68-20 (DB7). Analyzer Pod P3-7.
17	User I/O (LAB B)	U68-19 (DB6). Analyzer Pod P3-38.
18	VCCIO (3.3V or 5.0V)	Dedicated pin.
19	User I/O (LAB B)	U68-18 (DB5). Analyzer Pod P3-36.
20	User I/O (LAB B)	U68-17 (DB4). Analyzer Pod P3-9.
21	User I/O (LAB B)	U68-16 (DB3). Analyzer Pod P3-34.
22	No Connect (N.C.)	Dedicated pin.
23	User I/O (LAB B)	U68-15 (DB2). Analyzer Pod P3-11.
24	No Connect (N.C.)	Dedicated pin.

25	User I/O (LAB B)	U68-14 (DB1). Analyzer Pod P3-32.
26	Ground	Dedicated pin.
27	No Connect (N.C.)	Dedicated pin.
28	No Connect (N.C.)	Dedicated pin.
29	User I/O (LAB B)	U68-13 (DB0). Analyzer Pod P3-30.
30	User I/O (LAB B)	U68-10 (/LDAC). Analyzer Pod P3-28.
31	User I/O (LAB B)	U68-9 (/CLR). Analyzer Pod P3-31.
32	User I/O (LAB B)	U68-8 (A0). Analyzer Pod P3-33.
33	User I/O (LAB B)	U68-7 (/WR). Analyzer Pod P3-35.
34	VCCIO (3.3V or 5.0V)	Dedicated pin.
35	User I/O (LAB B)	U68-6 (/CS). Analyzer Pod P3-37.
36	User I/O (LAB B)	LED D1A (Cal ON). Analyzer Pod P3-26.
37	User I/O (LAB B)	LED D1D. Analyzer Pod P3-21.
38	Ground	Dedicated pin.
39	VCC INT (5.0V only)	Dedicated pin.
40	User I/O (LAB C)	SW1A. Analyzer Pod P3-19.
41	User I/O (LAB C)	SW1B. Analyzer Pod P3-17.
42	User I/O (LAB C)	SW1C. Analyzer Pod P3-15.
43	Ground	Dedicated pin.
44	User I/O (LAB C)	SW1D Analyzer Pod P3-13.
45	User I/O (LAB C)	Backplane connector P2-C18. Analyzer Pod P4-26.
46	User I/O (LAB C)	Backplane connector P2-C17. Analyzer Pod P4-38.
47	User I/O (LAB C)	TEST_ENB. Analyzer Pod P4-37.
48	User I/O (LAB C)	Backplane connector P2-C30. Analyzer Pod P4-8.
49	No Connect (N.C.)	Dedicated pin.
50	No Connect (N.C.)	Dedicated pin.
51	VCCIO (3.3V or 5.0V)	Dedicated pin.
52	User I/O (LAB C)	U69-13 (/2OE). Analyzer Pod P4-27.
53	No Connect (N.C.)	Dedicated pin.
54	User I/O (LAB C)	U69-14 (2A4). Analyzer Pod P4-29.
55	No Connect (N.C.)	Dedicated pin.
56	User I/O (LAB C)	U69-15 (2A3). Analyzer Pod P4-31.
57	User I/O (LAB C)	U69-17 (2A2). Analyzer Pod P4-33.
58	User I/O (LAB C)	U69-18 (2A1). Analyzer Pod P4-35.
59	Ground	Dedicated pin.
60	User I/O (LAB C)	U69-19 (1A4) . Analyzer Pod P4-28.
61	User I/O (LAB C)	U69-20 (1A3). Analyzer Pod P4-30.
62	TCK/User I/O (LAB C)	Dedicated pin.
63	User I/O (LAB D)	U69-22 (1A2). Analyzer Pod P4-32.
64	User I/O (LAB D)	U69-23 (1A1). Analyzer Pod P4-34.
65	User I/O (LAB D)	U69-24 (/1OE). Analyzer Pod P4-36.
66	VCCIO (3.3V or 5.0V)	Dedicated pin.
67	User I/O (LAB D)	Backplane connector P2-A30. Analyzer Pod P4-10.
68	User I/O (LAB D)	Backplane connector P2-C29. Analyzer Pod P4-12.
69	User I/O (LAB D)	Backplane connector P2-A29. Analyzer Pod P4-14.
70	No Connect (N.C.)	Dedicated pin.
71	User I/O (LAB D)	Backplane connector P2-C28. Analyzer Pod P4-16.
72	No Connect (N.C.)	Dedicated pin.
73	TDO/User I/O (LAB D)	Dedicated pin.

74	Ground	Dedicated pin.
75	User I/O (LAB D)	Backplane connector P2-A28. Analyzer Pod P4-18.
76	User I/O (LAB D)	Backplane connector P2-C27. Analyzer Pod P4-20.
77	No Connect (N.C.)	Dedicated pin.
78	No Connect (N.C.)	Dedicated pin.
79	User I/O (LAB D)	Backplane connector P2-A27. Analyzer Pod P4-22.
80	User I/O (LAB D)	Backplane connector P2-C26. Analyzer Pod P4-24.
81	User I/O (LAB D)	Backplane connector P2-A26. Analyzer Pod P4-7.
82	VCCIO (3.3V or 5.0V)	Dedicated pin.
83	User I/O (LAB D)	Backplane connector P2-C25. Analyzer Pod P4-9.
84	User I/O (LAB D)	Backplane connector P2-A25. Analyzer Pod P4-11.
85	User I/O (LAB D)	Backplane connector P2-C24. Analyzer Pod P4-13.
86	Ground	Dedicated pin.
87	INPUT/GCLK1	Dedicated pin. Y1-3. Signal CLK_IN_53.
88	INPUT/OE1	Dedicated pin.
89	INPUT/GCLRn	Dedicated pin.
90	INPUT/OE2/GCLK2	Dedicated pin.
91	VCC INT (5.0V only)	Dedicated pin.
92	User I/O (LAB A)	Backplane connector P2-A24. Analyzer Pod P4-15.
93	User I/O (LAB A)	Backplane connector P2-C23. Analyzer Pod P4-17.
94	User I/O (LAB A)	Backplane connector P2-C22. Analyzer Pod P4-19.
95	Ground	Dedicated pin.
96	User I/O (LAB A)	Backplane connector P2-C21. Analyzer Pod P4-21.
97	User I/O (LAB A)	Backplane connector P2-C20. Analyzer Pod P4-23.
98	User I/O (LAB A)	Backplane connector P2-C19. Analyzer Pod P4-25.
99	User I/O (LAB A)	SW1G. Analyzer Pod P3-8.
100	User I/O (LAB A)	U65-12 (4A) . Analyzer Pod P3-10.

Table 7.9, MI-BPM-TB Module Controller CPLD pinout

7.6 MI-BPM-TB JTAG Interface

See a description of JTAG in Section 10 (Page 50, Glossary). One four pin Test Access Port (TAP) is provided on the MI-BPM-TB module, it accesses the Module Controller CPLD.

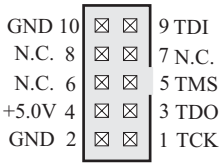

Figure 7.8, JTAG Interface

JTAG Chain		
Device #	Device Type	Notes
1	EPM7064ST100	Module Controller CPLD

Table 7.10, JTAG Chain Devices

8 Appendix B – MI BPM TB Control Module Motherboard Connectors Pinout

8.1 MI-BPM-TB Control Module Motherboard Timing Module interface connector

Notes	Schematic name	Pin #			Pin #	Schematic name	Notes
DATA0 (+)	FECTL_P_0	1			35	FECTL_N_0	DATA0 (-)
DATA1 (+)	FECTL_P_1	2			36	FECTL_N_1	DATA1 (-)
DATA2 (+)	FECTL_P_2	3			37	FECTL_N_2	DATA2 (-)
DATA3 (+)	FECTL_P_3	4			38	FECTL_N_3	DATA3 (-)
DATA4 (+)	FECTL_P_4	5			39	FECTL_N_4	DATA4 (-)
DATA5 (+)	FECTL_P_5	6			40	FECTL_N_5	DATA5 (-)
DATA6 (+)	FECTL_P_6	7			41	FECTL_N_6	DATA6 (-)
DATA7 (+)	FECTL_P_7	8			42	FECTL_N_7	DATA7 (-)
DATA8 (+)	FECTL_P_8	9			43	FECTL_N_8	DATA8 (-)
DATA9 (+)	FECTL_P_9	10			44	FECTL_N_9	DATA9 (-)
DATA10 (+)	FECTL_P_10	11			45	FECTL_N_10	DATA10 (-)
DATA11 (+)	FECTL_P_11	12			46	FECTL_N_11	DATA11 (-)
DATA12 (+)	FECTL_P_12	13			47	FECTL_N_12	DATA12 (-)
DATA13 (+)	FECTL_P_13	14			48	FECTL_N_13	DATA13 (-)
DATA14 (+)	FECTL_P_14	15			49	FECTL_N_14	DATA14 (-)
DATA15 (+)	FECTL_P_15	16			50	FECTL_N_15	DATA15 (-)
DATA16 (+)	FECTL_P_16	17			51	FECTL_N_16	DATA16 (-)
DATA17 (+)	FECTL_P_17	18			52	FECTL_N_17	DATA17 (-)
DATA18 (+)	FECTL_P_18	19			53	FECTL_N_18	DATA18 (-)
DATA19 (+)	FECTL_P_19	20			54	FECTL_N_19	DATA19 (-)
DATA20 (+)	FECTL_P_20	21			55	FECTL_N_20	DATA20 (-)
DATA21 (+)	FECTL_P_21	22			56	FECTL_N_21	DATA21 (-)
DATA22 (+)	FECTL_P_22	23			57	FECTL_N_22	DATA22 (-)
DATA23 (+)	FECTL_P_23	24			58	FECTL_N_23	DATA23 (-)
DATA24 (+)	FECTL_P_24	25			59	FECTL_N_24	DATA24 (-)
DATA25 (+)	FECTL_P_25	26			60	FECTL_N_25	DATA25 (-)
DATA26 (+)	FECTL_P_26	27			61	FECTL_N_26	DATA26 (-)
DATA27 (+)	FECTL_P_27	28			52	FECTL_N_27	DATA27 (-)
DATA28 (+)	FECTL_P_28	29			63	FECTL_N_28	DATA28 (-)
DATA29 (+)	FECTL_P_29	30			64	FECTL_N_29	DATA29 (-)
DATA30 (+)	FECTL_P_30	31			65	FECTL_N_30	DATA30 (-)
DATA31 (+)	FECTL_P_31	32			66	FECTL_N_31	DATA31 (-)
	GND (*)	33			67	GND (*)	
	GND (*)	34			67	GND (*)	
	Shield GND (*)	S1			S2	Shield GND (*)	

Table 8.1, Timing Module interface connector pinout

(*) Note: requires hardware modification.

8.2 MI-BPM-TB Control Module Motherboard Logic Analyzer Connectors

The following tables list the signals connected to the MI-BPM-TB CTL module's logic analyzer connectors.

Notes	Control Module schematic name (Avnet Card name)	Pin #	Pin name	Pin name	Pin #	Control Module schematic name (Avnet Card name)	Notes
N.C.	N.C.	1	+5VDC	SCL	2	N.C.	N.C.
Ground	GND	3	GND	SDA	4	N.C.	N.C.
N.C.	N.C.	5	CLK1	CLK2	6	N.C.	N.C.
Bypass Switch Control PI3C3245 U20-pin19	/BS_BE3 (CNTL15)	7	P1.15	P2.15	8	N.C.	N.C.
Bypass Switch Control PI3C3245 U19-pin19	/BS_BE2 (CNTL12)	9	P1.14	P2.14	10	N.C.	N.C.
Bypass Switch Control PI3C3245 U18-pin19	/BS_BE1 (CNTL11)	11	P1.13	P2.13	12	N.C.	N.C.
Bypass Switch Control PI3C3245 U17-pin19	/BS_BE0 (CNTL8)	13	P1.12	P2.12	14	N.C.	N.C.
Backplane Interface PI3C3126 U21-pin15	BE3 (CNTL7)	15	P1.11	P2.11	16	N.C.	N.C.
Backplane Interface PI3C3126 U21-pin12	BE2 (CNTL4)	17	P1.10	P2.10	18	N.C.	N.C.
Backplane Interface PI3C3126 U21-pin5	BE1 (CNTL3)	19	P1.09	P2.09	20	CLK_OUT (CLK_OUT)	N.C.
Backplane Interface PI3C3126 U21-pin2	BE0 (CNTL0)	21	P1.08	P2.08	22	JTAG_TMS (JTAG_TMS)	N.C.
Backplane Interface 74F245 U8-pin1, SN74LVC2G04 U11-pin3	BPLN_DIR3 (CNTL14)	23	P1.07	P2.07	24	JTAG_TDI (JTAG_TDI)	N.C.
Backplane Interface 74F245 U5-pin1, SN74LVC2G04 U11-pin1	BPLN_DIR2 (CNTL13)	25	P1.06	P2.06	26	JTAG_TRS (JTAG_TRS)	N.C.
Backplane Interface 74F245 U3-pin1, SN74LVC2G04 U10-pin3	BPLN_DIR1 (CNTL10)	27	P1.05	P2.05	28	JTAG_TCK (JTAG_TCK)	N.C.
Backplane Interface 74F245 U1-pin1, SN74LVC2G04 U10-pin1	BPLN_DIR0 (CNTL9)	29	P1.04	P2.04	30	JTAG_TDO (JTAG_TDO)	N.C.
Backplane Interface 74F245 U8-pin19, IDT74LVC4245A U9-pin22	/BPLN_EN3 (CNTL6)	31	P1.03	P2.03	32	XCVR_DIR3 (CNTL20)	Timing Card Interface SN65LVDM1677DGG U13-pin23/28
Backplane Interface 74F245 U5-pin19, IDT74LVC4245A U6-pin22	/BPLN_EN2 (CNTL5)	33	P1.02	P2.02	34	XCVR_DIR2 (CNTL19)	Timing Card Interface SN65LVDM1677DGG U13-pin5/10
Backplane Interface 74F245 U3-pin19, IDT74LVC4245A U4-pin22	/BPLN_EN1 (CNTL2)	35	P1.01	P2.01	36	XCVR_DIR1 (CNTL16)	Timing Card Interface SN65LVDM1677DGG U14-pin23/28
Backplane Interface 74F245 U1-pin19, IDT74LVC4245A U2-pin22	/BPLN_EN0 (CNTL1)	37	P1.00	P2.00	38	XCVR_DIR0 (CNTL18)	Timing Card Interface SN65LVDM1677DGG U14-pin5/10

Table 8.2, MI-BPM-TB-CTL - Logic Analyzer connector J8 - Control Signals

Notes	Schematic name	Pin #	Pin name	Pin name	Pin #	Schematic name	Notes
N.C.	N.C.	1	+5VDC	SCL	2	N.C.	N.C.
Ground	GND	3	GND	SDA	4	N.C.	N.C.
N.C.	N.C.	5	CLK1	CLK2	6	N.C.	N.C.
LVDS Cable RX/TX (FECTL_15)	DATA15	7	P1.15	P2.15	8	DATA31	LVDS Cable RX/TX (FECTL_31)
LVDS Cable RX/TX (FECTL_14)	DATA14	9	P1.14	P2.14	10	DATA30	LVDS Cable RX/TX (FECTL_30)
LVDS Cable RX/TX (FECTL_13)	DATA13	11	P1.13	P2.13	12	DATA29	LVDS Cable RX/TX (FECTL_29)
LVDS Cable RX/TX (FECTL_12)	DATA12	13	P1.12	P2.12	14	DATA28	LVDS Cable RX/TX (FECTL_28)
LVDS Cable RX/TX (FECTL_11)	DATA11	15	P1.11	P2.11	16	DATA27	LVDS Cable RX/TX (FECTL_27)
LVDS Cable RX/TX (FECTL_10)	DATA10	17	P1.10	P2.10	18	DATA26	LVDS Cable RX/TX (FECTL_26)
LVDS Cable RX/TX (FECTL_9)	DATA9	19	P1.09	P2.09	20	DATA25	LVDS Cable RX/TX (FECTL_25)
LVDS Cable RX/TX (FECTL_8)	DATA8	21	P1.08	P2.08	22	DATA24	LVDS Cable RX/TX (FECTL_24)
LVDS Cable RX/TX (FECTL_7)	DATA7	23	P1.07	P2.07	24	DATA23	LVDS Cable RX/TX (FECTL_23)
LVDS Cable RX/TX (FECTL_6)	DATA6	25	P1.06	P2.06	26	DATA22	LVDS Cable RX/TX (FECTL_22)
LVDS Cable RX/TX (FECTL_5)	DATA5	27	P1.05	P2.05	28	DATA21	LVDS Cable RX/TX (FECTL_21)
LVDS Cable RX/TX (FECTL_4)	DATA4	29	P1.04	P2.04	30	DATA20	LVDS Cable RX/TX (FECTL_20)
LVDS Cable RX/TX (FECTL_3)	DATA3	31	P1.03	P2.03	32	DATA19	LVDS Cable RX/TX (FECTL_19)
LVDS Cable RX/TX (FECTL_2)	DATA2	33	P1.02	P2.02	34	DATA18	LVDS Cable RX/TX (FECTL_18)
LVDS Cable RX/TX (FECTL_1)	DATA1	35	P1.01	P2.01	36	DATA17	LVDS Cable RX/TX (FECTL_17)
LVDS Cable RX/TX (FECTL_0)	DATA0	37	P1.00	P2.00	38	DATA16	LVDS Cable RX/TX (FECTL_16)

Table 8.3, MI-BPM-TB-CTL - Logic Analyzer connector J5 - Timing Module Interface

Notes	Schematic name	Pin #	Pin name	Pin name	Pin #	Schematic name	Notes
N.C.	N.C.	1	+5VDC	SCL	2	N.C.	N.C.
Ground	GND	3	GND	SDA	4	N.C.	N.C.
Input of Backplane Test Clock Transmitter	TEST_CLK	5	CLK1	CLK2	6	RTEST_CLK	Output of Backplane Test Clock Receiver
Input of Backplane TX/RX (VME-A15)	BUF_A15	7	P1.15	P2.15	8	BUF_A31	Input of Backplane TX/RX (VME-D07)
Input of Backplane TX/RX (VME-A14)	BUF_A14	9	P1.14	P2.14	10	BUF_A30	Input of Backplane TX/RX (VME-D06)
Input of Backplane TX/RX (VME-A13)	BUF_A13	11	P1.13	P2.13	12	BUF_A29	Input of Backplane TX/RX (VME-D05)
Input of Backplane TX/RX (VME-A12)	BUF_A12	13	P1.12	P2.12	14	BUF_A28	Input of Backplane TX/RX (VME-D04)
Input of Backplane TX/RX (VME-A11)	BUF_A11	15	P1.11	P2.11	16	BUF_A27	Input of Backplane TX/RX (VME-D03)
Input of Backplane TX/RX (VME-A10)	BUF_A10	17	P1.10	P2.10	18	BUF_A26	Input of Backplane TX/RX (VME-D02)
Input of Backplane TX/RX (VME-A09)	BUF_A09	19	P1.09	P2.09	20	BUF_A25	Input of Backplane TX/RX (VME-D01)
Input of Backplane TX/RX (VME-A08)	BUF_A08	21	P1.08	P2.08	22	BUF_A24	Input of Backplane TX/RX (VME-D00)
Input of Backplane TX/RX (VME-A07)	BUF_A07	23	P1.07	P2.07	24	BUF_A23	Input of Backplane TX/RX (VME-A23)
Input of Backplane TX/RX (VME-A06)	BUF_A06	25	P1.06	P2.06	26	BUF_A22	Input of Backplane TX/RX (VME-A22)
Input of Backplane TX/RX (VME-A05)	BUF_A05	27	P1.05	P2.05	28	BUF_A21	Input of Backplane TX/RX (VME-A21)
Input of Backplane TX/RX (VME-A04)	BUF_A04	29	P1.04	P2.04	30	BUF_A20	Input of Backplane TX/RX (VME-A20)
Input of Backplane TX/RX (VME-A03)	BUF_A03	31	P1.03	P2.03	32	BUF_A19	Input of Backplane TX/RX (VME-A19)
Input of Backplane TX/RX (VME-A02)	BUF_A02	33	P1.02	P2.02	34	BUF_A18	Input of Backplane TX/RX (VME-A18)
Input of Backplane TX/RX (VME-A01)	BUF_A01	35	P1.01	P2.01	36	BUF_A17	Input of Backplane TX/RX (VME-A17)
Input of Backplane TX/RX (N.C.)	BUF_A00	37	P1.00	P2.00	38	BUF_A16	Input of Backplane TX/RX (VME-A16)

Table 8.4, MI-BPM-TB-CTL - Logic Analyzer connector J3 - Backplane Interface

8.3 Backplane Interface - connectors pinout

The following table describes the signals used by the MI-BPM-TB CTL on connector J1. The signals highlighted in blue are those used by the MI-BPM-TB CTL but are not used by the MI-BPM-TB (stand-by signals).

The signals highlighted in green are those used by the MI-BPM-TB.

A table describing the pin assignment for connectors J1 on a standard VME backplane interface is available in Appendix A (Section 0, page 28).

Pin#	Row A	Row B	Row C
1	A24 (Backplane Standby VME-D00)	Not Connected	Not Connected
2	A25 (Backplane Standby VME-D01)	Not Connected	Not Connected
3	A26 (Backplane Standby VME-D02)	Not Connected	Not Connected
4	A27 (Backplane Standby VME-D03)	Not Connected	Not Connected
5	A28 (Backplane Standby VME-D04)	Not Connected	Not Connected
6	A29 (Backplane Standby VME-D05)	Not Connected	Not Connected
7	A30 (Backplane Standby VME-D06)	Not Connected	Not Connected
8	A31 (Backplane Standby VME-D07)	Not Connected	Not Connected
9	GND (Ground)	Not Connected	GND (Ground)
10	Not Connected	Not Connected	Not Connected
11	GND (Ground)	Not Connected	Not Connected
12	pTest_Clock	Not Connected	Not Connected
13	nTest_Clock	Not Connected	Not Connected
14	Not Connected	Not Connected	Not Connected
15	GND (Ground)	Not Connected	A23 (Backplane Standby VME-A23)
16	Not Connected	Not Connected	A22 (Backplane Standby VME-A22)
17	GND (Ground)	Not Connected	A21 (BackplaneReserved01, VME-A21)
18	Not Connected	Not Connected	A20 (BackplaneReserved00, VME-A20)
19	GND (Ground)	Not Connected	A19 (BackplaneAddress01, VME-A19)
20	Not Connected	GND (Ground)	A18 (BackplaneAddress00, VME-A18)
21	Not Connected	Not Connected	A17 (BackplaneStrobe, VME-A17)
22	Not Connected	Not Connected	A16 (BackplaneData15, VME-A16)
23	Not Connected	GND (Ground)	A15 (BackplaneData14, VME-A15)
24	A07 (BackplaneData06, VME-A07)	Not Connected	A14 (BackplaneData13, VME-A14)
25	A06 (BackplaneData05, VME-A06)	Not Connected	A13 (BackplaneData12, VME-A13)
26	A05 (BackplaneData04, VME-A05)	Not Connected	A12 (BackplaneData11, VME-A12)
27	A04 (BackplaneData03, VME-A04)	Not Connected	A11 (BackplaneData10, VME-A11)
28	A03 (Backplane Data02, VME-A03)	Not Connected	A10 (BackplaneData09, VME-A10)
29	A02 (BackplaneData01, VME-A02)	Not Connected	A09 (BackplaneData08, VME-A09)
30	A01 (BackplaneData00, VME-A01)	Not Connected	A08 (BackplaneData07, VME-A08)
31	Power: -5V Analog (monitoring only)	Not Connected	Power: +5V Analog (monitoring only)
32	Power: +5V Digital	Power: +5V Digital	Power: +5V Digital

Table 8.5, MI-BPM-TB CTL J1/P1 Pin Assignments

9 Appendix C – Xilinx Avnet Card Connectors Pinout

9.1 Xilinx Avnet Card Logic Analyzer connectors

The following three tables list the signals connected to the Xilinx Avnet Card's logic analyzer connector.

Notes	Xilinx Avnet Card Schematic name [FPGA Pin#]	Pin #	Pin name	Pin name	Pin #	Xilinx Avnet Card Schematic name [FPGA Pin#]	Notes
	N.C.	1	+5VDC	SCL	2	N.C.	
	N.C.	3	GND	SDA	4	N.C.	
Backplane Interface PI3C3126 U21-pin11 (EXT_TST_CLK)	CLK_OUT [P182]	5	CLK1	CLK2	6	OSC [P80]	
Backplane Interface (A31, VME-D07)	ADDRESS31 [P45]	7	P1.15	P2.15	8	ADDRESS15 [P22]	Backplane Interface (A15, VME-A15)
Backplane Interface (A30, VME-D06)	ADDRESS30 [P44]	9	P1.14	P2.14	10	ADDRESS14 [P21]	Backplane Interface (A14, VME-A14)
Backplane Interface (A29, VME-D05)	ADDRESS29 [P43]	11	P1.13	P2.13	12	ADDRESS13 [P13]	Backplane Interface (A13, VME-A13)
Backplane Interface (A28, VME-D04)	ADDRESS28 [P42]	13	P1.12	P2.12	14	ADDRESS12 [P18]	Backplane Interface (A12, VME-A12)
Backplane Interface (A27, VME-D03)	ADDRESS27 [P41]	15	P1.11	P2.11	16	ADDRESS11 [P17]	Backplane Interface (A11, VME-A11)
Backplane Interface (A26, VME-D02)	ADDRESS26 [P37]	17	P1.10	P2.10	18	ADDRESS10 [P16]	Backplane Interface (A10, VME-A10)
Backplane Interface (A25, VME-D01)	ADDRESS25 [P36]	19	P1.09	P2.09	20	ADDRESS9 [P15]	Backplane Interface (A09, VME-A09)
Backplane Interface (A24, VME-D00)	ADDRESS24 [P35]	21	P1.08	P2.08	22	ADDRESS8 [P14]	Backplane Interface (A08, VME-A08)
Backplane Interface (A23, VME-A23)	ADDRESS23 [P34]	23	P1.07	P2.07	24	ADDRESS7 [P10]	Backplane Interface (A07, VME-A07)
Backplane Interface (A22, VME-A22)	ADDRESS22 [P33]	25	P1.06	P2.06	26	ADDRESS6 [P9]	Backplane Interface (A06, VME-A06)
Backplane Interface (A21, VME-A21)	ADDRESS21 [P31]	27	P1.05	P2.05	28	ADDRESS5 [P8]	Backplane Interface (A05, VME-A05)
Backplane Interface (A20, VME-A20)	ADDRESS20 [P30]	29	P1.04	P2.04	30	ADDRESS4 [P7]	Backplane Interface (A04, VME-A04)
Backplane Interface (A19, VME-A19)	ADDRESS19 [P29]	31	P1.03	P2.03	32	ADDRESS3 [P6]	Backplane Interface (A03, VME-A03)
Backplane Interface (A18, VME-A18)	ADDRESS18 [P27]	33	P1.02	P2.02	34	ADDRESS2 [P5]	Backplane Interface (A02, VME-A02)
Backplane Interface (A17, VME-A17)	ADDRESS17 [P24]	35	P1.01	P2.01	36	ADDRESS1 [P4]	Backplane Interface (A01, VME-A01)
Backplane Interface (A16, VME-A16)	ADDRESS16 [P23]	37	P1.00	P2.00	38	ADDRESS0 [P3]	Backplane Interface (N.C.)

Table 9.1, Xilinx Avnet Card - Logic Analyzer connector J4 (suggested analyzer pods: 1 and 2)

Notes	Xilinx Avnet Card Schematic name [FPGA Pin#]	Pin #	Pin name	Pin name	Pin #	Xilinx Avnet Card Schematic name [FPGA Pin#]	Notes
	N.C.	1	+5VDC	SCL	2	N.C.	
	N.C.	3	GND	SDA	4	N.C.	
	GCK3 [P185]	5	CLK1	CLK2	6	GCLK1 [P77]	
Timing Card Interface (FECTL31)	DATA31 [P162]	7	P1.15	P2.15	8	DATA15 [P187]	Timing Card Interface (FECTL15)
Timing Card Interface (FECTL30)	DATA30 [P163]	9	P1.14	P2.14	10	DATA14 [P188]	Timing Card Interface (FECTL14)
Timing Card Interface (FECTL29)	DATA29 [P164]	11	P1.13	P2.13	12	DATA13 [P189]	Timing Card Interface (FECTL13)
Timing Card Interface (FECTL28)	DATA28 [P165]	13	P1.12	P2.12	14	DATA12 [P191]	Timing Card Interface (FECTL12)
Timing Card Interface (FECTL27)	DATA27 [P166]	15	P1.11	P2.11	16	DATA11 [P192]	Timing Card Interface (FECTL11)
Timing Card Interface (FECTL26)	DATA26 [P167]	17	P1.10	P2.10	18	DATA10 [P193]	Timing Card Interface (FECTL10)
Timing Card Interface (FECTL25)	DATA25 [P168]	19	P1.09	P2.09	20	DATA9 [P194]	Timing Card Interface (FECTL9)
Timing Card Interface (FECTL24)	DATA24 [P172]	21	P1.08	P2.08	22	DATA8 [P195]	Timing Card Interface (FECTL8)
Timing Card Interface (FECTL23)	DATA23 [P173]	23	P1.07	P2.07	24	DATA7 [P199]	Timing Card Interface (FECTL7)
Timing Card Interface (FECTL22)	DATA22 [P174]	25	P1.06	P2.06	26	DATA6 [P200]	Timing Card Interface (FECTL6)
Timing Card Interface (FECTL21)	DATA21 [P175]	27	P1.05	P2.05	28	DATA5 [P201]	Timing Card Interface (FECTL5)
Timing Card Interface (FECTL20)	DATA20 [P176]	29	P1.04	P2.04	30	DATA4 [P202]	Timing Card Interface (FECTL4)
Timing Card Interface (FECTL19)	DATA19 [P178]	31	P1.03	P2.03	32	DATA3 [P203]	Timing Card Interface (FECTL3)
Timing Card Interface (FECTL18)	DATA18 [P179]	33	P1.02	P2.02	34	DATA2 [P204]	Timing Card Interface (FECTL2)
Timing Card Interface (FECTL17)	DATA17 [P180]	35	P1.01	P2.01	36	DATA1 [P205]	Timing Card Interface (FECTL1)
Timing Card Interface (FECTL16)	DATA16 [P181]	37	P1.00	P2.00	38	DATA0 [P206]	Timing Card Interface (FECTL0)

Table 9.2, Xilinx Avnet Card - Logic Analyzer connector J5 (suggested analyzer pods: 3 and 4)

Notes	Xilinx Avnet Card Schematic name [FPGA Pin#]	Pin #	Pin name	Pin name	Pin #	Xilinx Avnet Card Schematic name [FPGA Pin#]	Notes
	N.C.	1	+5VDC	SCL	2	N.C.	
	N.C	3	GND	SDA	4	N.C.	
Backplane Interface PI3C3126 U21-pin11 (EXT_TST_CLK)	CLK_OUT [P182]	5	CLK1	CLK2	6	CLK_IN [P147]	Backplane Interface PI3C3126 U21-pin6 (FPGA_TST_CLK)
	DOUT [P154]	7	P1.15	P2.15	8	CNTL15 [P81]	Bypass Switch Control PI3C3245 U20-pin19 (/BS_BE3)
	SWITCH9 [P109]	9	P1.14	P2.14	10	CNTL14 [P75]	Backplane Interface 74F245 U8-pin1, SN74LVC2G04 U11-pin3 (BPLN_DIR3)
	SWITCH8 [P110]	11	P1.13	P2.13	12	CNTL13 [P74]	Backplane Interface 74F245 U5-pin1, SN74LVC2G04 U11-pin1 (BPLN_DIR2)
	TEMP_SDO [P94]	13	P1.12	P2.12	14	CNTL12 [P73]	Bypass Switch Control PI3C3245 U19-pin19 (/BS_BE2)
	TEMP_SDI [P95]	15	P1.11	P2.11	16	CNTL11 [P71]	Bypass Switch Control PI3C3245 U18-pin19 (/BS_BE1)
	TEMP_CE [P96]	17	P1.10	P2.10	18	CNTL10 [P70]	Backplane Interface 74F245 U3-pin1, SN74LVC2G04 U10-pin3 (BPLN_DIR1)
	TEMP_SCLK [P97]	19	P1.09	P2.09	20	CNTL9 [P69]	Backplane Interface 74F245 U1-pin1, SN74LVC2G04 U10-pin1 (BPLN_DIR0)
	RS232SD_N [P149]	21	P1.08	P2.08	22	CNTL8 [P68]	Bypass Switch Control PI3C3245 U17-pin19 (/BS_BE0)
	RS232EN_N [P150]	23	P1.07	P2.07	24	CNTL7 [P67]	Backplane Interface PI3C3126 U21-pin15 (BE3)
	RS232TX [P151]	25	P1.06	P2.06	26	CNTL6 [P63]	Backplane Interface 74F245 U8-pin19, IDT74LVC4245A U9-pin22 (/BPLN_EN3)
	RS232RX [P152]	27	P1.05	P2.05	28	CNTL5 [P62]	Backplane Interface 74F245 U5-pin19, IDT74LVC4245A U6-pin22 (/BPLN_EN2)
Timing Card Interface SN65LVDM1677DGG U13-pin23/28 (XCVR_DIR3)	CNTL20 [P87]	29	P1.04	P2.04	30	CNTL4 [P61]	Backplane Interface PI3C3126 U21-pin12 (BE2)
Timing Card Interface SN65LVDM1677DGG U13-pin5/10 (XCVR_DIR2)	CNTL19 [P86]	31	P1.03	P2.03	32	CNTL3 [P60]	Backplane Interface PI3C3126 U21-pin5 (BE1)
Timing Card Interface SN65LVDM1677DGG U14-pin5/10 (XCVR_DIR0)	CNTL18 [P84]	33	P1.02	P2.02	34	CNTL2 [P59]	Backplane Interface 74F245 U3-pin19, IDT74LVC4245A U4-pin22 (/BPLN_EN1)
Backplane Interface SN65MLVDS203D U7-pin2 (RTEST_CLK)	CNTL17 [P83]	35	P1.01	P2.01	36	CNTL1 [P58]	Backplane Interface 74F245 U1-pin19, IDT74LVC4245A U2-pin22 (/BPLN_EN0)
Timing Card Interface SN65LVDM1677DGG U14-pin23/28 (XCVR_DIR1)	CNTL16 [P82]	37	P1.00	P2.00	38	CNTL0 [P57]	Backplane Interface PI3C3126 U21-pin2 (BE0)

Table 9.3, Xilinx Avnet Card - Logic Analyzer connector J6 (suggested analyzer pods: 5 and 6)

9.2 Xilinx Avnet Card Header connectors

The following two tables provide the pinouts of the Xilinx Avnet Card's header connectors.

Notes	Xilinx AvnetCard Schematic name [FPGA Pin#]	Pin #		Pin #	Xilinx Avnet Card Schematic name [FPGA Pin#]	Notes
Backplane Interface (N.C.)	ADDRESS0 [P3]	1		2	ADDRESS1 [P4]	Backplane Interface (A01, VME-A01)
Backplane Interface (A02, VME-A02)	ADDRESS2 [P5]	3		4	ADDRESS3 [P6]	Backplane Interface (A03, VME-A03)
Backplane Interface (A04, VME-A04)	ADDRESS4 [P7]	5		6	ADDRESS5 [P8]	Backplane Interface (A05, VME-A05)
Backplane Interface (A06, VME-A06)	ADDRESS6 [P9]	7		8	ADDRESS7 [P10]	Backplane Interface (A07, VME-A07)
Backplane Interface (A08, VME-A08)	ADDRESS8 [P14]	9		10	ADDRESS9 [P15]	Backplane Interface (A09, VME-A09)
Backplane Interface (A10 VME-A10)	ADDRESS10 [P16]	11		12	ADDRESS11 [P17]	Backplane Interface (A11, VME-A11)
Backplane Interface (A12, VME-A12)	ADDRESS12 [P18]	13		14	ADDRESS13 [P13]	Backplane Interface (A13, VME-A13)
Backplane Interface (A14, VME-A14)	ADDRESS14 [P21]	15		16	ADDRESS15 [P22]	Backplane Interface (A15, VME-A15)
Backplane Interface (A16, VME-A16)	ADDRESS16 [P23]	17		18	ADDRESS17 [P24]	Backplane Interface (A17, VME-A17)
Backplane Interface (A18, VME-A18)	ADDRESS18 [P27]	19		20	ADDRESS19 [P29]	Backplane Interface (A19, VME-A19)
Backplane Interface (A20, VME-A20)	ADDRESS20 [P30]	21		22	ADDRESS21 [P31]	Backplane Interface (A21, VME-A21)
Backplane Interface (A22, VME-A22)	ADDRESS22 [P33]	23		24	ADDRESS23 [P34]	Backplane Interface (A23, VME-A23)
Backplane Interface (A24, VME-A24)	ADDRESS24 [P35]	25		26	ADDRESS25 [P36]	Backplane Interface (A25, VME-A25)
Backplane Interface (A26, VME-A26)	ADDRESS26 [P37]	27		28	ADDRESS27 [P41]	Backplane Interface (A27, VME-A27)
Backplane Interface (A28, VME-A28)	ADDRESS28 [P42]	29		30	ADDRESS29 [P43]	Backplane Interface (A29, VME-A29)
Backplane Interface (A30, VME-A30)	ADDRESS30 [P44]	31		32	ADDRESS31 [P45]	Backplane Interface (A31, VME-A31)
Backplane Interface PI3C3126 U21-pin2 (BE0)	CNTL0 [P57]	33		34	CNTL1 [P58]	Backplane Interface 74F245 U1-pin19, IDT74LVC4245A U2-pin22 (/BPLN_EN0)
Backplane Interface 74F245 U3-pin19, IDT74LVC4245A U4-pin22 (/BPLN_EN1)	CNTL2 [P59]	35		36	CNTL3 [P60]	Backplane Interface PI3C3126 U21-pin5 (BE1)
Backplane Interface PI3C3126 U21-pin12 (BE2)	CNTL4 [P61]	37		38	CNTL5 [P62]	Backplane Interface 74F245 U5-pin19, IDT74LVC4245A U6-pin22 (/BPLN_EN2)
Backplane Interface 74F245 U8-pin19, IDT74LVC4245A U9-pin22 (/BPLN_EN3)	CNTL6 [P63]	39		40	CNTL7 [P67]	Backplane Interface PI3C3126 U21-pin15 (BE3)
Bypass Switch Control PI3C3245 U17-pin19 (/BS_BE0)	CNTL8 [P68]	41		42	CNTL9 [P69]	Backplane Interface 74F245 U1-pin1, SN74LVC2G04 U10-pin1 (BPLN_DIR0)
Backplane Interface 74F245 U3-pin1, SN74LVC2G04 U10-pin3 (BPLN_DIR1)	CNTL10 [P70]	43		44	PWDN# [P55]	
	OSC[P80] (*)	45		46	STATUS [P56]	
	DOUT[P154]	47		48	GND	
	GND	49		50	GND	

Table 9.4, Xilinx Avnet Card - Header connector JP5

Notes	Xilinx Avnet Card Schematic name [FPGA Pin#]	Pin #		Pin #	Xilinx Avnet Card Schematic name [FPGA Pin#]	Notes
Timing Card Interface (FECTL0)	DATA0 [P206]	1		2	DATA1 [P205]	Timing Card Interface (FECTL1)
Timing Card Interface (FECTL2)	DATA2 [P204]	3		4	DATA3 [P203]	Timing Card Interface (FECTL3)
Timing Card Interface (FECTL4)	DATA4 [P202]	5		6	DATA5 [P201]	Timing Card Interface (FECTL5)
Timing Card Interface (FECTL6)	DATA6 [P200]	7		8	DATA7 [P199]	Timing Card Interface (FECTL7)
Timing Card Interface (FECTL8)	DATA8 [P195]	9		10	DATA9 [P194]	Timing Card Interface (FECTL9)
Timing Card Interface (FECTL10)	DATA10 [P193]	11		12	DATA11 [P192]	Timing Card Interface (FECTL11)
Timing Card Interface (FECTL12)	DATA12 [P191]	13		14	DATA13 [P189]	Timing Card Interface (FECTL13)
Timing Card Interface (FECTL14)	DATA14 [P188]	15		16	DATA15 [P187]	Timing Card Interface (FECTL15)
Timing Card Interface (FECTL16)	DATA16 [P181]	17		18	DATA17 [P180]	Timing Card Interface (FECTL17)
Timing Card Interface (FECTL18)	DATA18 [P179]	19		20	DATA19 [P178]	Timing Card Interface (FECTL19)
Timing Card Interface (FECTL20)	DATA20 [P176]	21		22	DATA21 [P175]	Timing Card Interface (FECTL21)
Timing Card Interface (FECTL22)	DATA22 [P174]	23		24	DATA23 [P173]	Timing Card Interface (FECTL23)
Timing Card Interface (FECTL24)	DATA24 [P172]	25		26	DATA25 [P168]	Timing Card Interface (FECTL25)
Timing Card Interface (FECTL26)	DATA26 [P167]	27		28	DATA27 [P166]	Timing Card Interface (FECTL27)
Timing Card Interface (FECTL28)	DATA28[P165]	29		30	DATA29 [P164]	Timing Card Interface (FECTL29)
Timing Card Interface (FECTL30)	DATA30 [P163]	31		32	DATA31 [P162]	Timing Card Interface (FECTL31)
Bypass Switch Control PI3C3245 U18-pin19 (/BS_BE1)	CNTL11 [P71]	33		34	CNTL12 [P73]	Bypass Switch Control PI3C3245 U19-pin19 (/BS_BE2)
Backplane Interface 74F245 U5-pin1, SN74LVC2G04 U11-pin1 (BPLN_DIR2)	CNTL13 [P74]	35		36	CNTL14 [P75]	Backplane Interface 74F245 U8-pin1, SN74LVC2G04 U11-pin3 (BPLN_DIR3)
Bypass Switch Control PI3C3245 U20-pin19 (/BS_BE3)	CNTL15 [P81]	37		38	CNTL16 [P82]	Timing Card Interface SN65LVDM1677DGG U14-pin23/28 (XCVR_DIR1)
Backplane Interface SN65MLVDS203D U7-pin2 (RTEST_CLK)	CNTL17 [P83]	39		40	CNTL18 [P84]	Timing Card Interface SN65LVDM1677DGG U14-pin5/10 (XCVR_DIR0)
Timing Card Interface SN65LVDM1677DGG U13-pin5/10 (XCVR_DIR2)	CNTL19 [P86]	41		42	CNTL20 [P87]	Timing Card Interface SN65LVDM1677DGG U13-pin23/28 (XCVR_DIR3)
	GCK1 [P77]	43		44	CLK_IN [P147] (*)	Backplane Interface PI3C3126 U21-pin6 (FPGA_TST_CLK)
	GCK3 [P185]	45		46	CLK_OUT [P182] (*)	Backplane Interface PI3C3126 U21-pin11 (EXT_TST_CLK)
Backplane Interface PI3C3126 U21-pin11 (EXT_TST_CLK)	CLK_OUT_FB [P182] (*)	47		48	GND	
	GND	49		50	GND	

Table 9.5, Xilinx Avnet Card - Header connector JP6

9.3 Xilinx Avnet Card AvBus Header connector

The following two tables provide the pinout of the AvBus connector.

Color Legend	
	Standard (User I/O)
	Power
	Ground
	Not Connected

Notes	Xilinx Avnet Card Schematic name [FPGA Pin#]	Pin #		Pin #	Xilinx Avnet Card Schematic name [FPGA Pin#]	Notes
NC	NC (Res. 5.0V)	1		71	ADDRESS0 [P3]	Backplane Interface (N.C.)
Backplane Interface (A01, VME-A01)	ADDRESS1 [P4]	2		72	GND	
Backplane Interface (A02, VME-A02)	ADDRESS2 [P5]	3		73	ADDRESS3 [P6]	Backplane Interface (A03, VME-A03)
	GND	4		74	ADDRESS4 [P7]	Backplane Interface (A04, VME-A04)
Backplane Interface (A05, VME-A05)	ADDRESS5 [P8]	5		75	GND	
Backplane Interface (A06, VME-A06)	ADDRESS6 [P9]	6		76	ADDRESS7 [P10]	Backplane Interface (A07, VME-A07)
	GND	7		77	ADDRESS8 [P14]	Backplane Interface (A08, VME-A08)
Backplane Interface (A09, VME-A09)	ADDRESS9 [P15]	8		78	3.3V	3.3 Volt Power (3.3V_AUX)
Backplane Interface (A10, VME-A10)	ADDRESS10 [P16]	9		79	ADDRESS11 [P17]	Backplane Interface (A11, VME-A11)
	GND	10		80	ADDRESS12 [P18]	Backplane Interface (A12, VME-A12)
Backplane Interface (A13, VME-A13)	ADDRESS13 [P13]	11		81	GND	
Backplane Interface (A14, VME-A14)	ADDRESS14 [P21]	12		82	ADDRESS15 [P22]	Backplane Interface (A15, VME-A15)
NC	NC (Res. 5.0V)	13		83	ADDRESS16 [P23]	Backplane Interface (A16, VME-A16)
Backplane Interface (A17, VME-A17)	ADDRESS17 [P24]	14		84	GND	
Backplane Interface (A18, VME-A18)	ADDRESS18 [P27]	15		85	ADDRESS19 [P29]	Backplane Interface (A19, VME-A19)
	GND	16		86	ADDRESS20 [P30]	Backplane Interface (A20, VME-A20)
Backplane Interface (A21, VME-A21)	ADDRESS21 [P31]	17		87	GND	
Backplane Interface (A22, VME-A22)	ADDRESS22 [P33]	18		88	ADDRESS23 [P34]	Backplane Interface (A23, VME-A23)
	GND	19		89	ADDRESS24 [P35]	Backplane Interface (A24, VME-D0)
Backplane Interface (A25, VME-D1)	ADDRESS25 [P36]	20		90	3.3V	3.3 Volt Power (3.3V_AUX)
Backplane Interface (A26, VME-D2)	ADDRESS26 [P37]	21		91	ADDRESS27 [P41]	Backplane Interface (A27, VME-D3)
	GND	22		92	ADDRESS28 [P42]	Backplane Interface (A28, VME-D4)
Backplane Interface (A29, VME-D5)	ADDRESS29 [P43]	23		93	GND	
Backplane Interface (A30, VME-D6)	ADDRESS30 [P44]	24		94	ADDRESS31 [P45]	Backplane Interface (A31, VME-D7)
NC	NC (Res. 5.0V)	25		95	DATA0 [P206]	Timing Card Interface (FECTL0)
Timing Card Interface (FECTL1)	DATA1 [P205]	26		96	GND	
Timing Card Interface (FECTL2)	DATA2 [P204]	27		97	DATA3 [P203]	Timing Card Interface (FECTL3)
	GND	28		98	DATA4 [P202]	Timing Card Interface (FECTL4)
Timing Card Interface (FECTL5)	DATA5 [P201]	29		99	GND	
Timing Card Interface (FECTL6)	DATA6 [P200]	30		100	DATA7 [P199]	Timing Card Interface (FECTL7)
	GND	31		101	DATA8 [P195]	Timing Card Interface (FECTL8)
Timing Card Interface (FECTL9)	DATA9 [P194]	32		102	3.3V	3.3 Volt Power (3.3V_AUX)
Timing Card Interface (FECTL10)	DATA10 [P193]	33		103	DATA11 [P192]	Timing Card Interface (FECTL11)
	GND	34		104	DATA12 [P191]	Timing Card Interface (FECTL12)
Timing Card Interface (FECTL13)	DATA13 [P189]	35		105	GND	
Timing Card Interface (FECTL14)	DATA14 [P188]	36		106	DATA15 [P187]	Timing Card Interface (FECTL15)
NC	NC (Res. 5.0V)	37		107	DATA16 [P181]	Timing Card Interface (FECTL16)

Table 9.6, Xilinx Avnet Card - Header connector P2-A (AvBus)

Notes	Xilinx Avnet Card Schematic name [FPGA Pin#]	Pin #		Pin #	Xilinx Avnet Card Schematic name [FPGA Pin#]	Notes
Timing Card Interface (FECTL17)	DATA17 [P180]	38		108	GND	
Timing Card Interface (FECTL18)	DATA18 [P179]	39		109	DATA19 [P178]	Timing Card Interface (FECTL19)
	GND	40		110	DATA20 [P176]	Timing Card Interface (FECTL20)
Timing Card Interface (FECTL21)	DATA21 [P175]	41		111	GND	
Timing Card Interface (FECTL22)	DATA22 [P174]	42		112	DATA23 [P173]	Timing Card Interface (FECTL23)
	GND	43		113	DATA24 [P172]	Timing Card Interface (FECTL24)
Timing Card Interface (FECTL25)	DATA25 [P168]	44		114	3.3V	3.3 Volt Power (3.3V_AUX)
Timing Card Interface (FECTL26)	DATA26 [P167]	45		115	DATA27 [P166]	Timing Card Interface (FECTL27)
	GND	46		116	DATA28 [P165]	Timing Card Interface (FECTL28)
Timing Card Interface (FECTL29)	DATA29 [P164]	47		117	GND	
Timing Card Interface (FECTL30)	DATA30 [P163]	48		118	DATA31 [P162]	Timing Card Interface (FECTL31)
NC	NC (Res. 5.0V)	49		119	CNTL0 [P57]	Backplane Interface PI3C3126 U21-pin2 (BE0)
Backplane Interface 74F245 U1-pin19, IDT74LVC4245A U2-pin22 (/BPLN_EN0)	CNTL1 [P58]	50		120	GND	
Backplane Interface 74F245 U3-pin19, IDT74LVC4245A U4-pin22 (/BPLN_EN1)	CNTL2 [P59]	51		121	CNTL3 [P60]	Backplane Interface PI3C3126 U21-pin5 (BE1)
	GND	52		122	CNTL4 [P61]	Backplane Interface PI3C3126 U21-pin12 (BE2)
Backplane Interface 74F245 U5-pin19, IDT74LVC4245A U6-pin22 (/BPLN_EN2)	CNTL5 [P62]	53		123	GND	
Backplane Interface 74F245 U8-pin19, IDT74LVC4245A U9-pin22 (/BPLN_EN3)	CNTL6 [P63]	54		124	CNTL7 [P67]	Backplane Interface PI3C3126 U21-pin15 (BE3)
	GND	55		125	CNTL8 [P68]	Bypass Switch Control PI3C3245 U17-pin19 (/BS_BE0)
Backplane Interface 74F245 U1-pin1, SN74LVC2G04 U10-pin1 (BPLN_DIR0)	CNTL9 [P69]	56		126	3.3V	3.3 Volt Power (3.3V_AUX)
Backplane Interface 74F245 U3-pin1, SN74LVC2G04 U10-pin3 (BPLN_DIR1)	CNTL10 [P70]	57		127	CNTL11 [P71]	Bypass Switch Control PI3C3245 U18-pin19 (/BS_BE1)
	GND	58		128	CNTL12 [P73]	Bypass Switch Control PI3C3245 U19-pin19 (/BS_BE2)
Backplane Interface 74F245 U5-pin1, SN74LVC2G04 U11-pin1 (BPLN_DIR2)	CNTL13 [P74]	59		129	GND	
Backplane Interface 74F245 U8-pin1, SN74LVC2G04 U11-pin3 (BPLN_DIR3)	CNTL14 [P75]	60		130	CNTL15 [P81]	Bypass Switch Control PI3C3245 U20-pin19 (/BS_BE3)
NC	NC (Res. 5.0V)	61		131	CNTL16 [P82]	Timing Card Interface SN65LVDM1677DGG U14-pin23/28 (XCVR_DIR1)
Backplane Interface SN65MLVDS203D U7-pin2 (RTEST_CLK)	CNTL17 [P83]	62		132	GND	
Timing Card Interface SN65LVDM1677DGG U14-pin5/10 (XCVR_DIR0)	CNTL18 [P84]	63		133	CNTL19 [P86]	Timing Card Interface SN65LVDM1677DGG U13-pin5/10 (XCVR_DIR2)
	GND	64		134	CNTL20 [P87]	Timing Card Interface SN65LVDM1677DGG U13-pin23/28 (XCVR_DIR3)
Backplane Interface PI3C3126 U21-pin6 (FPGA_TST_CLK)	CLK_IN [P147] (*)	65		135	GND	
Backplane Interface PI3C3126 U21-pin11 (EXT_TST_CLK)	CLK_OUT_FB [P182] (*)	66		136	CLK_OUT [P182] (*)	PAD
	GND	67		137	JTAG_TMS [P100]	PAD
PAD	JTAG_TDO [P99]	68		138	3.3V	3.3 Volt Power (3.3V_AUX)
PAD	JTAG_TCK [P98]	69		139	JTAG_TDI [P101]	PAD
	GND	70		140	JTAG_TRS [P102]	PAD

Table 9.7, Xilinx Avnet Card - Header connector P2-B (AvBus)

10 Glossary

ACNET: Custom network protocol developed at Fermilab.

ANSI: American National Standards Institute. More information is available on the Internet: http://www.ansi.org/

AvBus: Custom Bus defined by Avnet [Ref.11] to be used as interface on evaluation modules.

BIST: Built-In Self Test, the method of designing circuits with additional logic that can be used to test correct operation of the primary (functional) logic.

BPM: Beam Position Monitor.

BSDL: Boundary Scan Description Language. IEEE 1149.1-1993b defines a language that describes IEEE 1149.1 architecture for an integrated circuit. This language is known as the Boundary Scan Description Language (BSDL). Updated BSDL files for the Altera devices used on the MI-BPM-TM Module can be found at:

ECHOTEK: Term used to refer to the Eight Channel Analog to Digital Converter with Digital Receiver Echoteck module [Ref.14] used in the MI BPM Project.

EDIF: Electronic Data Interchange Format. Industry-standard for specifying a logic design in text (ASCII) form.

EIA: Electronics Industries Alliance.
http://www.eia.org/

EIA-232: see RS-232.

FPGA: Field Programmable Gate Array. An integrated circuit that contains configurable (programmable) logic blocks and configurable (programmable) interconnect between these blocks.

IEEE: Institute of Electrical and Electronics Engineers, Inc. More information is available on the Internet:
http://www.ieee.org/

Jitter: The JEDEC Standard No. 65 (EIA/JESD65) defines jitter as the magnitude of the time deviation of a controlled edge from its nominal position.

JTAG: Joint Test Action Group. Older name for IEEE 1149.1 boundary scan, a method to test printed circuit boards and also integrated circuits. See also BSDL.

Design complexity, difficulty of loaded board testing, and the limited pin access of surface mount technology led industry leaders to seek accord on a standard to support the solution of these problems.

The standard defines a hardware architecture and the mechanisms for its use.

The standard itself defines instructions that can be used to perform functional and interconnect tests as well as built-in self-test procedures. Vendor-specific extensions to the standard have been developed to allow execution of maintenance and diagnostic applications as well as programming algorithms for re-configurable parts.

The top level schematic of the test logic defined by IEEE Std 1149.1 includes three key blocks:

The *TAP Controller*

This responds to the control sequences supplied through the test access port (TAP) and generates the clock and control signals required for correct operation of the other circuit blocks.

The *Instruction Register*

This shift register-based circuit is serially loaded with the instruction that selects an operation to be performed.

The *Data Registers*

These are a bank of shift register based circuits. The stimuli required by an operation are serially loaded into the data registers selected by the current instruction. Following execution of the operation, results can be shifted out for examination.

The *JTAG Test Access Port* (TAP) contains four pins that drive the circuit blocks and control the operations specified. The TAP facilitates the serial loading and unloading of instructions and data. The four pins of the TAP are: TMS (Test Mode Select), TCK (Test Clock), TDI (Test Data In) and TDO (Test Data Out). The function of each TAP pin is as follows:

TCK - this pin is the JTAG test clock. It sequences the TAP controller as well as all of the JTAG registers.

TMS - this pin is the mode input signal to the TAP Controller. The TAP controller is a FSM that provides the control logic for JTAG. The state of TMS at the rising edge of TCK determines the sequence of states for the TAP controller. TMS has an internal pull-up resistor on it to provide a logic 1 to the system if the pin is not driven.

TDI -this pin is the serial data input to all JTAG instruction and data registers. The state of the TAP controller as well as the particular instruction held in the instruction register determines which register is fed by TDI for a specific operation. TDI has an internal pull-up resistor on it to provide a logic 1 to the system if the pin is not driven. TDI is sampled into the JTAG registers on the rising edge of TCK.

TDO - this pin is the serial data output for all JTAG instruction and data registers. The state of the TAP controller as well as the particular instruction held in the instruction register determines which register feeds TDO for a specific operation. Only one register (instruction or data) is allowed to be the active connection between TDI and TDO for any given operation. TDO changes state on the falling edge of TCK and is only active during the shifting of data through the device. This pin is three-stated at all other times.

LVDS (TIA/EIA-644): Low Voltage Differential Signaling. Is a signaling method used for high-speed, low-power transmission of binary data over copper [Ref.26]. A revised version of the standard was published in 2001 as ANSI/TIA/EIA-644-A-2001 (Low Voltage Differential Signaling (LVDS) Interface Circuits. The revised version includes requirements for LVDS devices being used in multidrop configuration.

LVDM: A family of components introduced by Texas Instruments in 1998. It complies with the LVDS (TIA/EIA-644) standard with the exception of doubling the output current.

LVTTL: Low Voltage TTL. Is one of the several switching standards used in digital electronics.

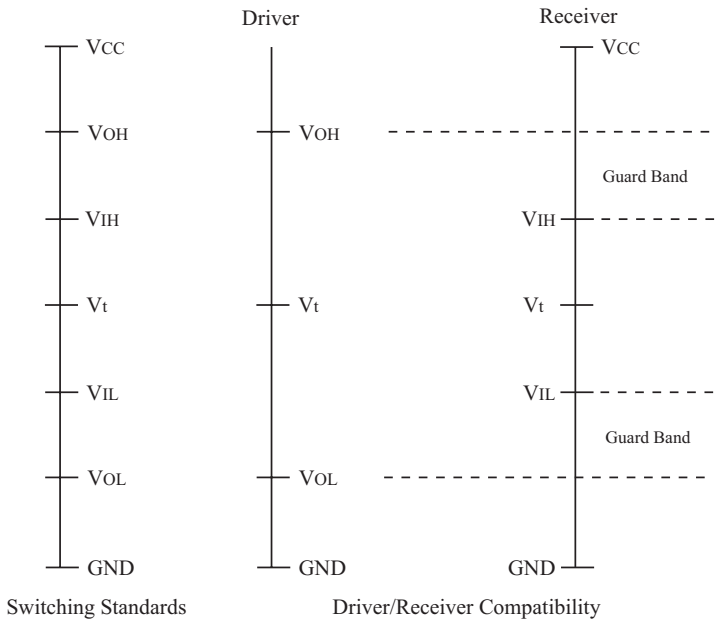

Figure 10.1, Switching standards.

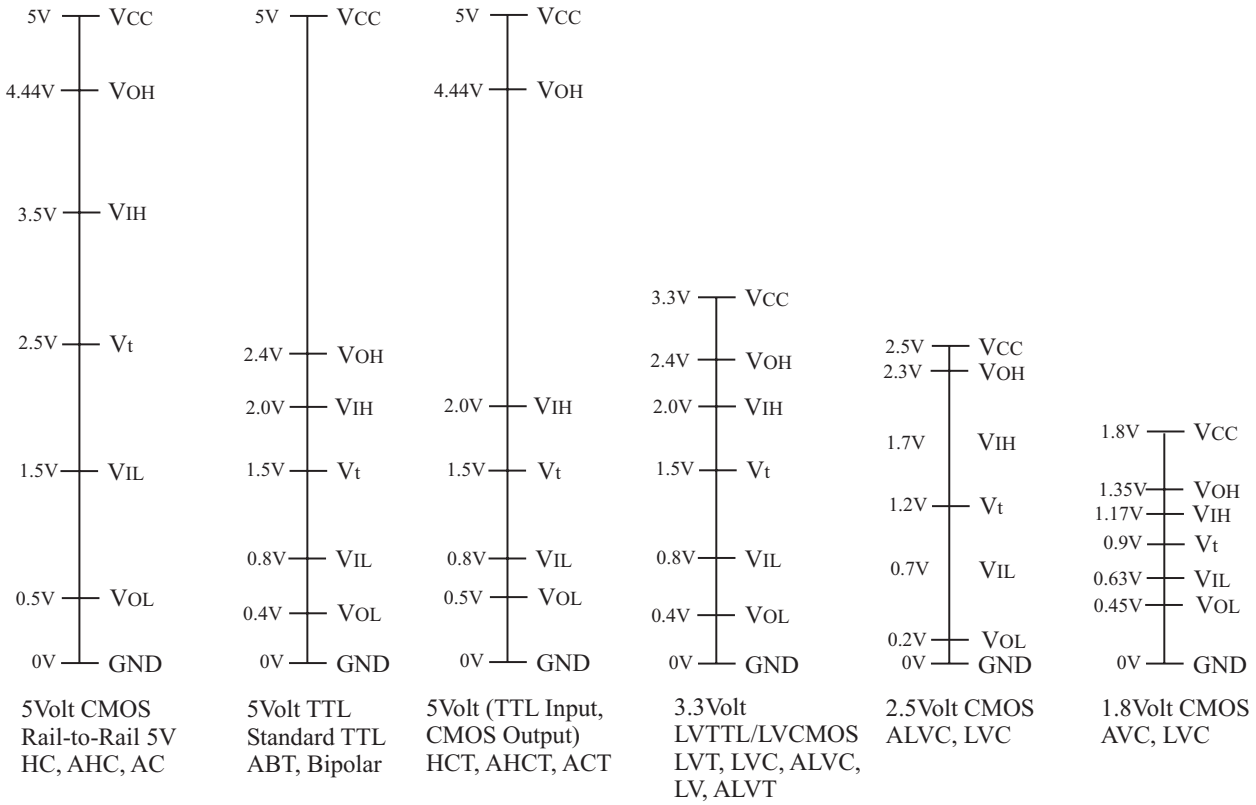

Figure 10.2, Comparison of switching standards.

MI: Fermilab Main Injector.

MI-BPM-TB: Main Injector Beam Position Monitor Transition Board.

MI-BPM-TB-CTL: Main Injector Beam Position Monitor Transition Board Subrack Controller.

M-LVDS (TIA/EIA-899): Multipoint-Low-Voltage Differential Signaling (M-LVDS) Interface Circuits for Multipoint Data Interchange (ANSI/TIA/EIA-899-2002). Is a high speed balanced interface standard [Ref.26]. See also LVDS and LVDM.

Multidrop: A common interconnection configuration. In a multidrop system a single driver is used and multiple receivers are connected to the main transmission line. Where line termination is necessary, a single termination is located at the far end of the line from the transmitter. A multidrop connection provides unidirectional transmission. [Ref.26].

Multipoint: An interconnection architecture where many transmitters and many receivers can be interconnected on a single transmission line. In such architecture there are contention issues that need not to be addressed poin a point-to-point or multidrop system. [Ref.26].

RS-232: The "Recommended Standard" RS-232 bus standard is one of the most popular serial communication bus designs. It is widely used as an intersystem serial communication link. The RS-232 is a serial data, point to point design, with a signal line dedicated for communications in each direction (full-duplex).

SCSI: Small Computer Systems Interface.

Skew: The JEDEC Standard No. 65 (EIA/JESD65) defines skew as The magnitude of the time difference between two events that ideally would occur simultaneously.

TFG: Timing Fanout Generator module.

VHDL: "V" stands for Very High Speed Integrated Circuit and "HDL" stands for Hardware Description Language.

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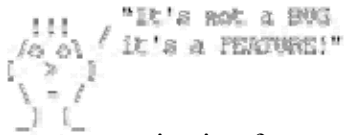

[30] Private communication from undisclosed source.

[31] Private communication from John Smith.