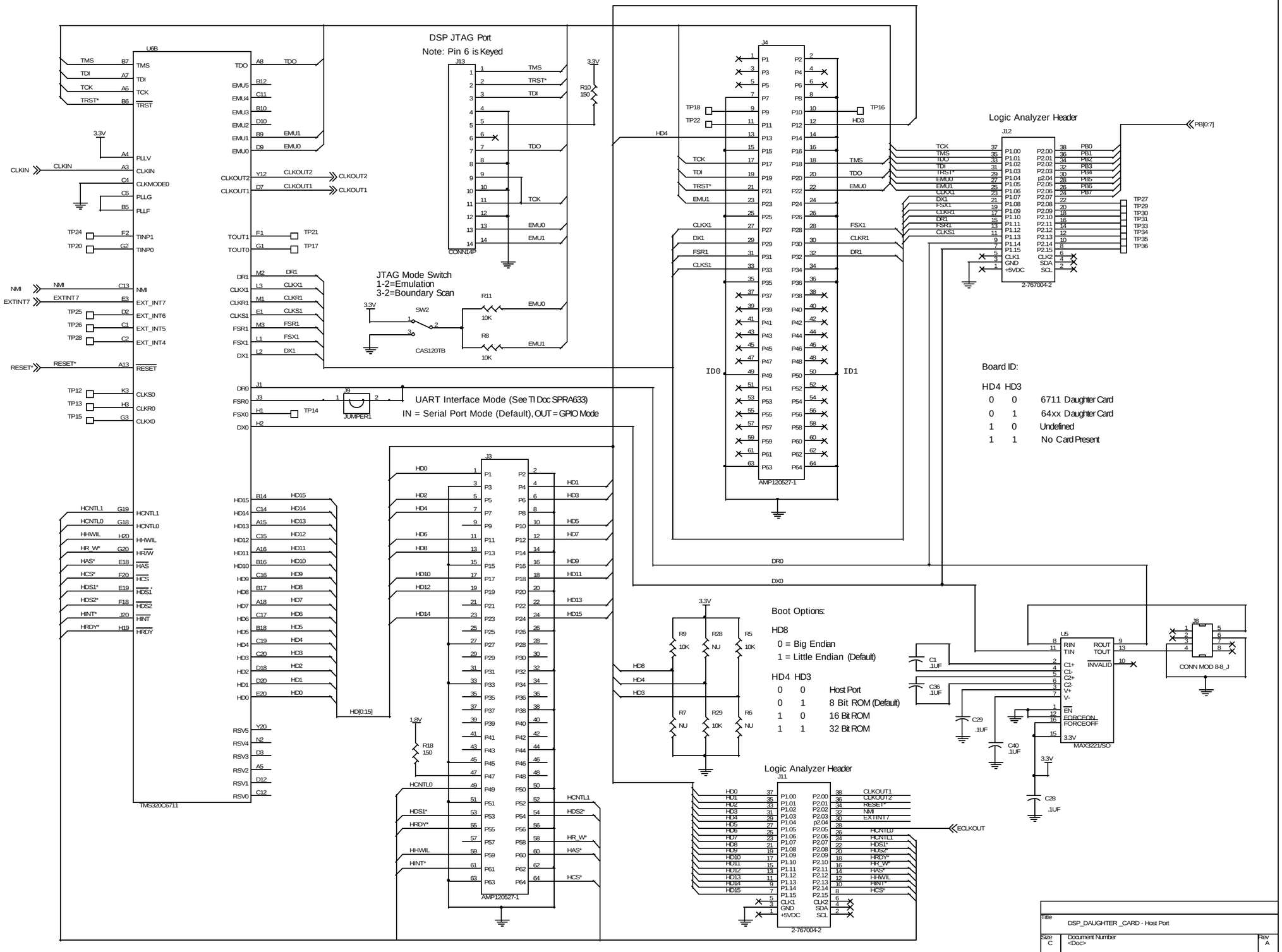
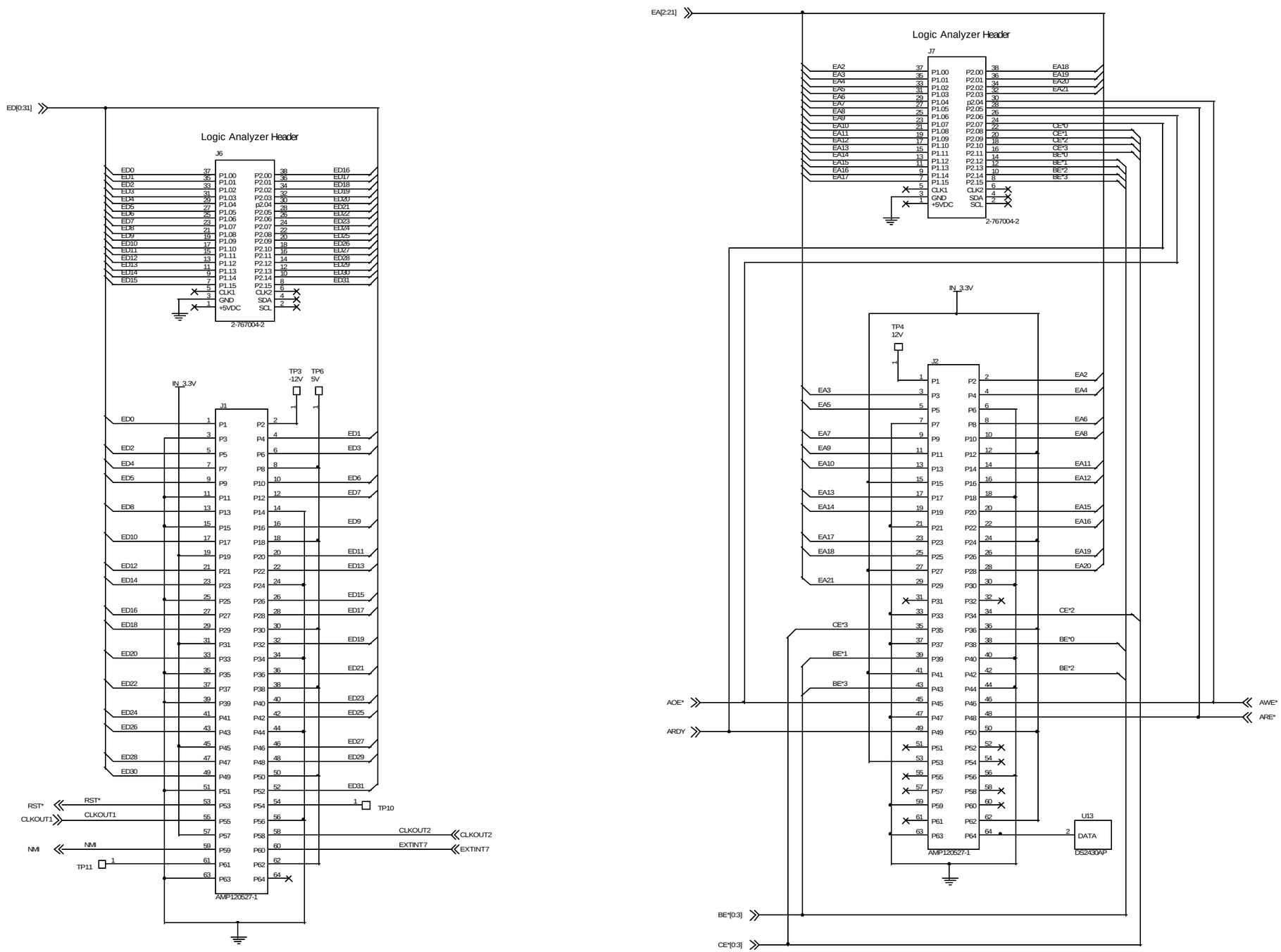
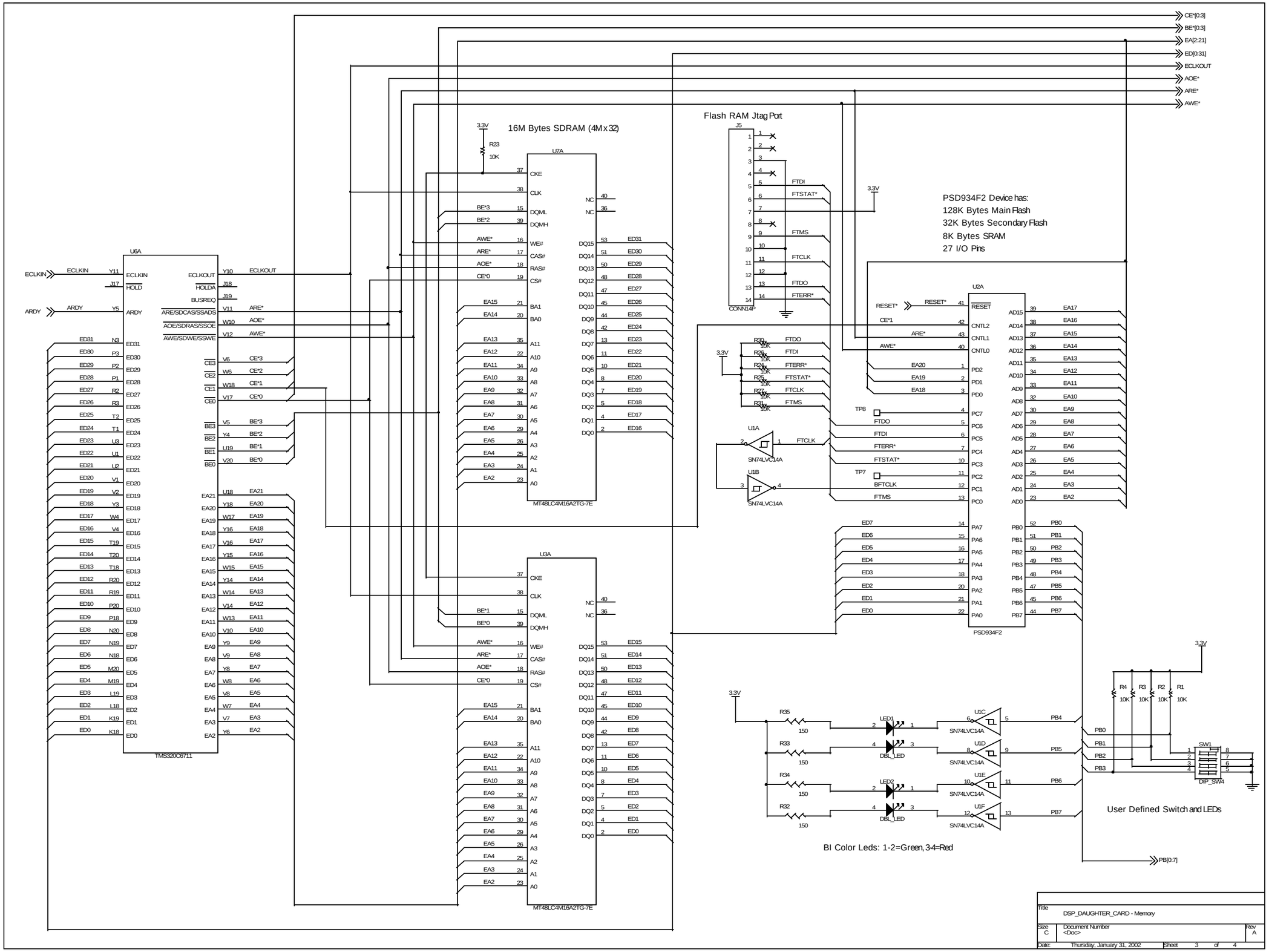

DSP JTAG Port
Note: Pin 6 is Keyed
JTAG Mode Switch
1-2=Emulation
3-2=Boundary Scan
UART Interface Mode (See TI Doc SPRA633)
IN = Serial Port Mode (Default), OUT = GPIO Mode
Logic Analyzer Header
Board ID:
HD4 HD3
0 0 6711 Daughter Card
0 1 64xx Daughter Card
1 0 Undefined
1 1 No Card Present
Boot Options:
HD8
0 = Big Endian
1 = Little Endian (Default)
HD4 HD3
0 0 Host Port
0 1 8 Bit ROM (Default)
1 0 16 Bit ROM
1 1 32 Bit ROM
Logic Analyzer Header
TMS320C6711
AMP120527-1
2-767004-2
MAX3221/SO
CONN MOD 8-8_J
Title
DSP_DAUGHTER _CARD - Host Port
Size C
Document Number <Doc>
Rev A
Date: Thursday, January 31, 2002
Sheet 1 of 4



Title	DSP_DAUGHTER_CARD - J1/2	
Size C	Document Number <Doc>	Rev A
Date: Thursday, January 31, 2002	Sheet 2 of 4	


16M Bytes SDRAM (4Mx32)
U7A
MT48LC4M16A2TG-7E
U3A
MT48LC4M16A2TG-7E
U6A
TMS320C6711
Flash RAM Jtag Port
J5
CONN14P
PSD934F2 Device has:
128K Bytes Main Flash
32K Bytes Secondary Flash
8K Bytes SRAM
27 I/O Pins
U2A
PSD934F2
U1A
U1B
U1C
U1D
U1E
U1F
SN74LVC14A
LED1
LED2
DBL_LED
SW1
DIP_SW4
User Defined Switch and LEDs
BI Color Leds: 1-2=Green, 3-4=Red
CE*[0:3]
BE*[0:3]
EA[2:21]
ED[0:31]
ECLKOUT
AOE*
ARE*
AWE*
PB[0:7]
Title
DSP_DAUGHTER_CARD - Memory
Size
C
Document Number
<Doc>
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A
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3
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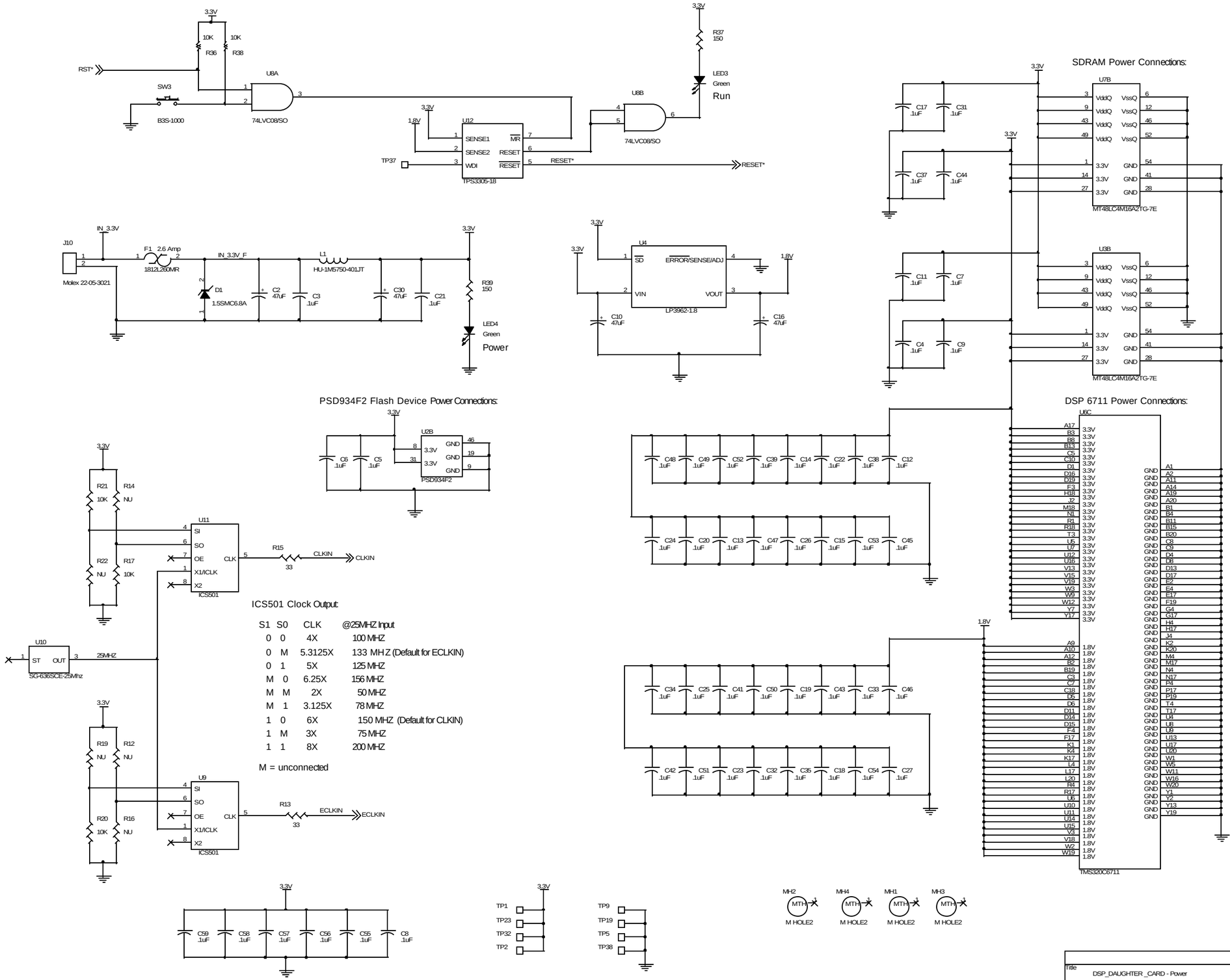

Title	DSP_DAUGHTER _CARD - Power		
Size C	Document Number <Doc>		Rev A
Date: Thursday, January 31, 2002		Sheet 4 of 4	