

Global Level 1

In the specification of a Global Level 1 Trigger system we assume the following parameters:

DSP Farmlet to Global Level 1 message: Packet size < 50 bytes.

Total Global Level 1 message frequency: 7.5757 MHz (132 ns BCOs).

Total required bandwidth: 3.030 Gb/s (378.78 Mby/s).

Total Number of DSPs in the L1 Trigger: 2500.

Total number of Highways: 4 to 8.

Number of DSPs per PC board: 4 to 8.

This example of the L1 Trigger Processor considers 2500 DSP-based processing elements supplying short messages with L1 Trigger analysis information to the Global Level 1 Processor (GL1). On average there is one message every BCO (132ns) for the whole system. Even when the DSP Farmlets will pack more than one DSP per board, the number of links to the GL1 is large. However, the individual required bandwidth of these links is low. Every DSP Processor in a Farmlet requires a bandwidth equal to the number of bytes in the message times the message frequency (i.e the DSP Trigger latency). This equals about 1.21 Mb/s. The total bandwidth from a Farmlet to the GL1 Processor is 1.21 Mb/s times the No of DSPs in the Farmlet (i.e. 9.7 Mb/s for an 8 DSP Farmlet).

Since, most likely, the DSP Farmlets will be packed in racks to optimize for space and simplify power and cooling, we can place a GL1 network concentrator. Figure 1 shows the GL1 network concentrator in yellow and the DSP Farmlets in blue. The GL1 network concentrator can have point-to-point low speed connections to the Farmlets and a higher-speed point-to-point connection to the GL1.

A second way of simplifying the network burden to the GL1 is, as also shown in Figure 1, by keeping a similar Highway structure in the GL1.

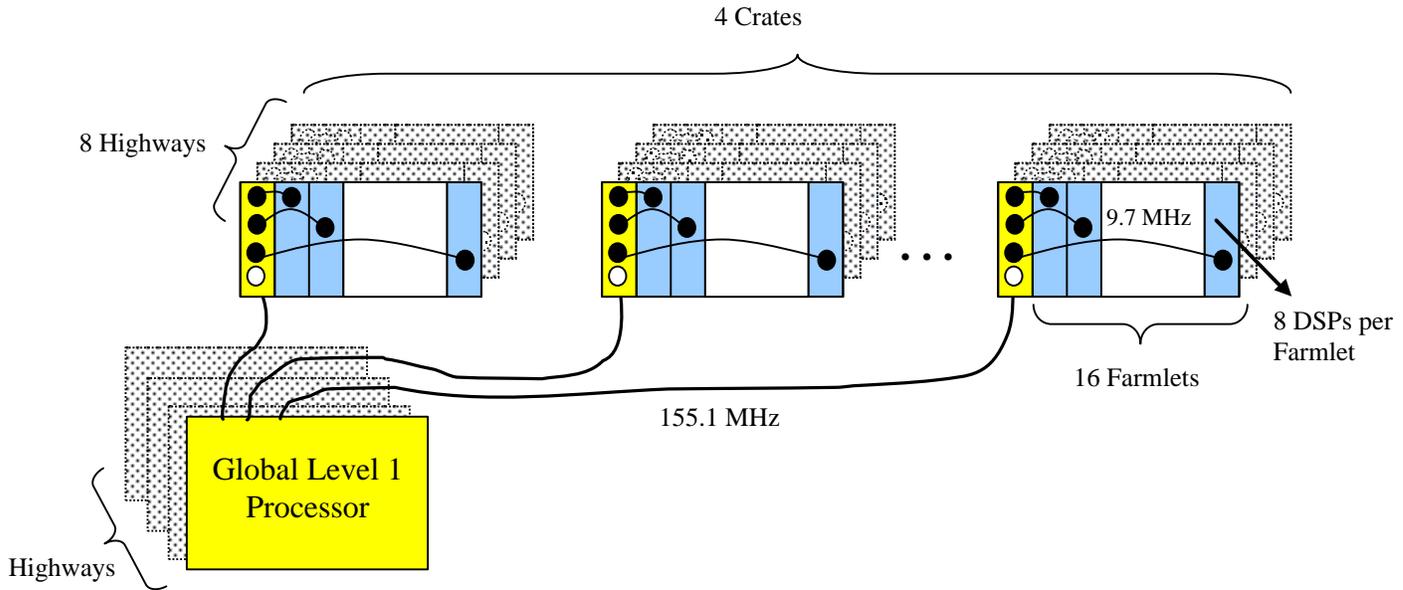


Figure 1: Example of DSP Farmlet to GL1 network

Table 1 shows the Number of DSP Farmlets and Crates and the Link bandwidths as a function of the number of Highways and DSP per Farmlet.

No Highways	DSPs/board	No DSP farmlets (per H_way) (Total No DSPs: 4000)	No Crates/Hway (16 boards/crate) (Total No DSPs: 4000)	GL1 Link Bwidth (Mb/s)	Farmlet Link Bwidth (Mb/s)
1	4	1000	63	77.6	4.85
1	6	667	42	116.4	7.28
1	8	500	32	155.2	9.7
4	4	250	16	77.6	4.85
4	6	167	11	116.4	7.28
4	8	125	8	155.2	9.7
8	4	125	8	77.6	4.85
8	6	84	6	116.4	7.28
8	8	63	4	155.2	9.7

Global Level 1 Architecture:

The GL1 Processor interfaces to the following systems:

- L1 Pixel Trigger Processor
- Muon Trigger Processor
- Front-end electronic system
- L2/3 Trigger
- Run/Control system
- Global Level 1 Supervisor and Monitoring system (GLSM)

The first 3 items of the list above are the inputs based on which the GL1 generates Trigger Accept/Reject primitives for the L2/3. Figure 2 is a simplified block diagram of the GL1 Processor.

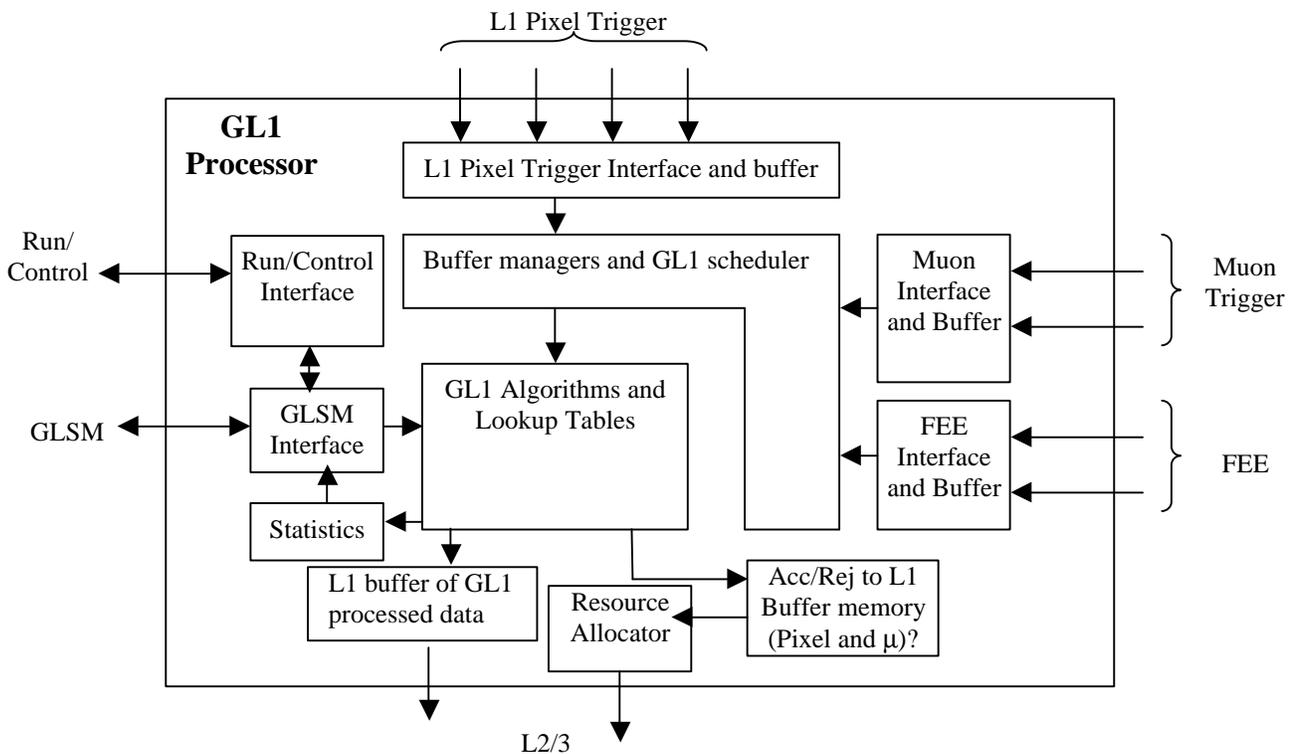


Figure 2: GL1 architecture block diagram

The Run/Control Interface must decode Run/Control primitives selecting
The Accept/Reject Link must send accept or reject primitives to the L1 buffers in the Segment Preprocessor and Track and Vertex Processor to allow the L1 buffers to deallocate memory. The GL1 system issues, on average, one Accept/Reject primitive every BCO (i.e every 132ns). This primitives must encode the BCO number, a code for accept or reject and eventually the address of the DSP Farmlet to which the message is addressed. The total bandwidth required by the Accept/Reject Link should be less than 360 Mb/s (i.e. 7.57MHz times 6 bytes/primitive).

There are two alternatives for the addressing of the Accept/Reject primitive, if the GL1 processor keeps record of the DSP node or farmlet that generated the data, the accept/reject can be addressed back to it, otherwise it must be broadcast. In either case the GL1 highway structure helps to reduce the accept/reject message addressing problem because only 1/N of the total DSP farmlets are connected to a GL1 Processor. Then, the total Accept/Reject Link bandwidth required is a factor of N lower (p.e. 45 Mb/s for an 8 way GL1 system). The Accept/Reject Link can be design in parallel with the DSP Farmlet to GL1 Link.

Compliance with the Global Level 1 Requirement Document

x.1. must be accomplished by the DSP Farmlet to GL1 network. The “highwaied” GL1 Processors must be able to produce trigger decisions at 1/N of 7.6MHz.

x.2. must be accomplished by the GL1 Algorithms and Lookup Tables module.

x.3. the GL1 Algorithms and Lookup Tables module must be able to run partitions. There may be more than one instance of the GL1 Algorithms and Lookup Tables module running at the same time in each GL1 Processor. Part of the work must be accomplished by the Resource Allocator.

x.4. this requirement must be accomplished by the GL1 Algorithms and Lookup Tables module plus the GL1 L1 Buffer manager (the manager of the GL1 processed data).

x.5. this requirement must be accomplished by the GLSM and GL1 Algorithms and Lookup Tables module.

x.6. this requirement must be accomplished by the GL1 L1 Buffer manager and the Accept/Reject Link Interface and Network.

x.6b. the list of crossing satisfied by each trigger must be generated by the GL1 Algorithms and Lookup Tables module and handled by the Resource Allocator.

x.7 statistics such as histogramming and error bookeeping must be performed by a separate computing module close to the GL1 Algorithm module and reported though the GLSM Interface.

x.8. Throttling must have a slow dynamics (otherwise it may cause system instability). Throttling can be handled through the GLSM based on status reported through the same link, such us luminosity index. Throttling can be achieved by modifying the trigger tables and trigger priorities (or cuts).

A second throttling mechanism based on memory buffer availability can be implemented without feedback outside the GL1 Processor. This throttling can be based on simple “open-loop” decisions like trigger priorities.

x.9. Minimum L1 Latency can be built into the Buffer managers and GL1 Scheduler.

x.10. Same as for x.9.

Unknown parameters:

Some parameters that will have a key impact in the design of the GL1 Processor are still not entirely defined, such as:

Complexity of the GL1 algorithm.

Memory size to encode lookup tables.

Average size of required pixel, muon, and FEE buffers.

Average size of required output buffer to store GL1 processed data.

No Highways	DSPs/board	Number of DSP boards (per Highway)for:		No Crates (16 boards/crate)	
		2500	4000	2500	4000
1	4	625	1000	40	63
1	6	417	667	27	42
1	8	313	500	20	32
4	4	157	250	10	16
4	6	105	167	7	11
4	8	79	125	5	8
8	4	79	125	5	8
8	6	53	84	4	6
8	8	40	63	3	4

No Highways	DSPs/board	No DSP farmlets (per H_way) (Total No DSPs: 4000)	No Crates (16 boards/crate) (Total No DSPs: 4000)	GL1 Link Bandwidth (Mb/s)	Farmlet Link Bandw (Mb/s)
1	4	1000	63	128	0.8
1	6	667	42	19.2	1.2
1	8	500	32	25.6	1.6
4	4	250	16	128	0.8
4	6	167	11	19.2	1.2
4	8	125	8	25.6	1.6
8	4	125	8	128	0.8
8	6	84	6	19.2	1.2
8	8	63	4	25.6	1.6