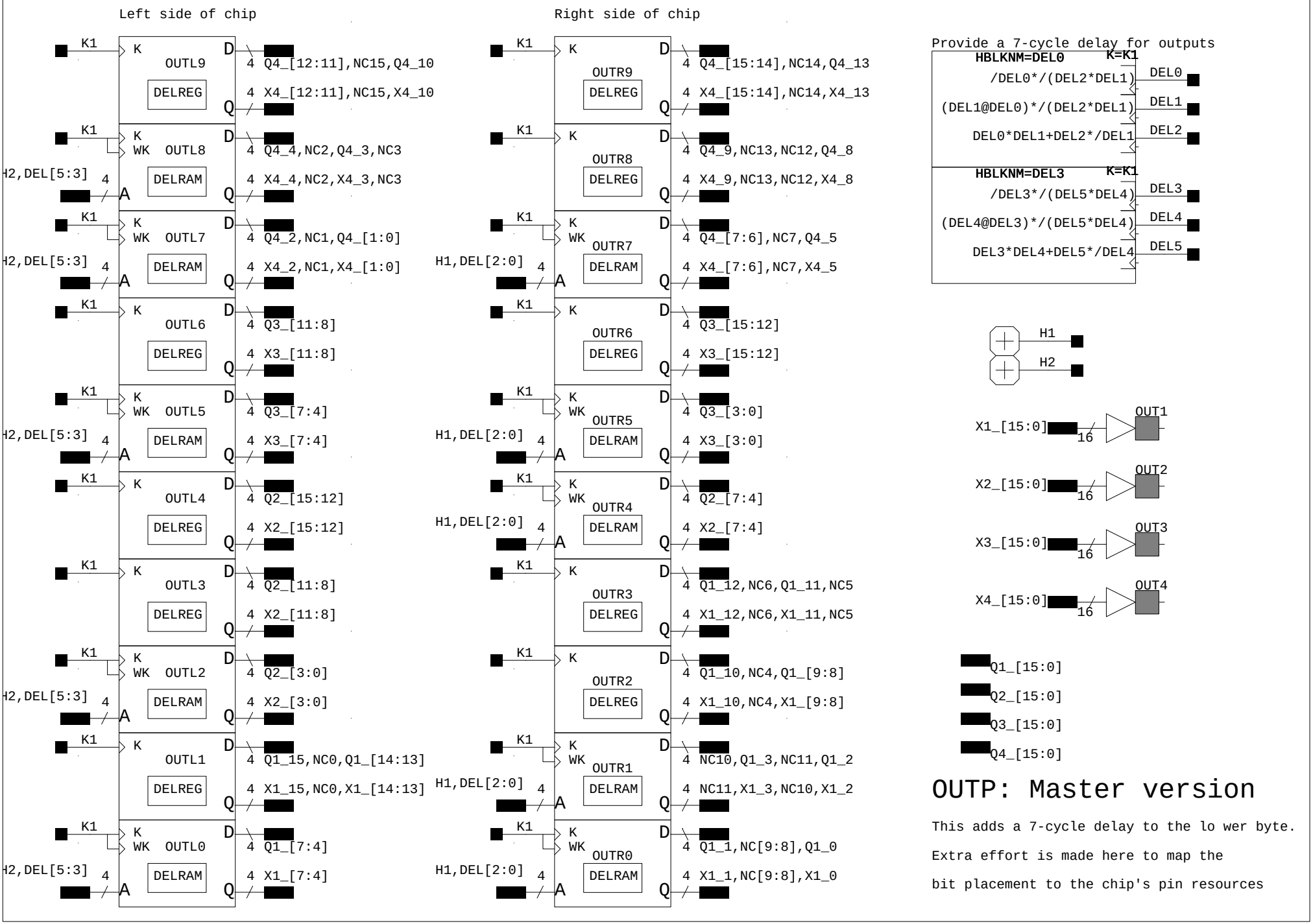
Left side of chip
Right side of chip
Provide a 7-cycle delay for outputs
HBLKNM=DEL0
K=K1
/DEL0*/(DEL2*DEL1)
(DEL1@DEL0)*/(DEL2*DEL1)
DEL0*DEL1+DEL2*/DEL1
DEL0
DEL1
DEL2
HBLKNM=DEL3
K=K1
/DEL3*/(DEL5*DEL4)
(DEL4@DEL3)*/(DEL5*DEL4)
DEL3*DEL4+DEL5*/DEL4
DEL3
DEL4
DEL5
H1
H2
X1_[15:0]
X2_[15:0]
X3_[15:0]
X4_[15:0]
16
OUT1
OUT2
OUT3
OUT4
Q1_[15:0]
Q2_[15:0]
Q3_[15:0]
Q4_[15:0]
OUTL9
DELREG
Q4_[12:11],NC15,Q4_10
X4_[12:11],NC15,X4_10
OUTL8
DELRAM
Q4_4,NC2,Q4_3,NC3
X4_4,NC2,X4_3,NC3
OUTL7
Q4_2,NC1,Q4_[1:0]
X4_2,NC1,X4_[1:0]
OUTL6
Q3_[11:8]
X3_[11:8]
OUTL5
Q3_[7:4]
X3_[7:4]
OUTL4
Q2_[15:12]
X2_[15:12]
OUTL3
Q2_[11:8]
X2_[11:8]
OUTL2
Q2_[3:0]
X2_[3:0]
OUTL1
Q1_15,NC0,Q1_[14:13]
X1_15,NC0,X1_[14:13]
OUTL0
Q1_[7:4]
X1_[7:4]
OUTR9
Q4_[15:14],NC14,Q4_13
X4_[15:14],NC14,X4_13
OUTR8
Q4_9,NC13,NC12,Q4_8
X4_9,NC13,NC12,X4_8
OUTR7
Q4_[7:6],NC7,Q4_5
X4_[7:6],NC7,X4_5
OUTR6
Q3_[15:12]
X3_[15:12]
OUTR5
Q3_[3:0]
X3_[3:0]
OUTR4
Q2_[7:4]
X2_[7:4]
OUTR3
Q1_12,NC6,Q1_11,NC5
X1_12,NC6,X1_11,NC5
OUTR2
Q1_10,NC4,Q1_[9:8]
X1_10,NC4,X1_[9:8]
OUTR1
NC10,Q1_3,NC11,Q1_2
NC11,X1_3,NC10,X1_2
OUTR0
Q1_1,NC[9:8],Q1_0
X1_1,NC[9:8],X1_0
K1
H2,DEL[5:3]
H1,DEL[2:0]
OUTP: Master version
This adds a 7-cycle delay to the lo wer byte.
Extra effort is made here to map the
bit placement to the chip's pin resources