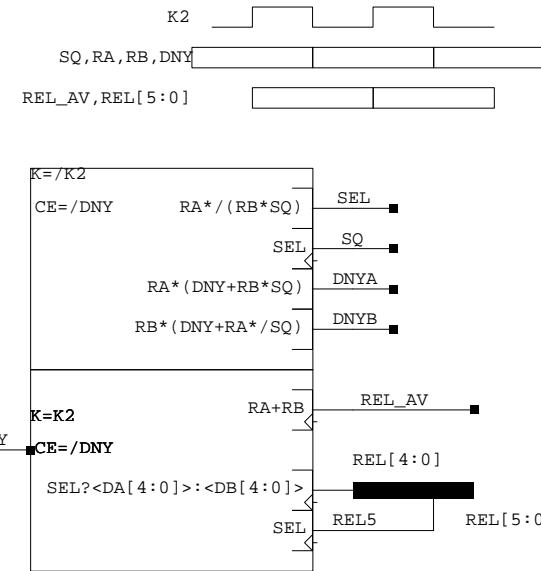


Last level of mergers is on rising clock to synchronize timing with the LL pipe.



Release

This takes release requests from 16 CPUs and merges them into a single stream of 6-bit numbers. The upper 4-bits indicate which CPU. The lower 2 bits are the buffer number. This is implemented as a tree: each stage selects one of two sources and passes it along. This could also be implemented as a simple FIFO with the merge function being done by the merge chip.