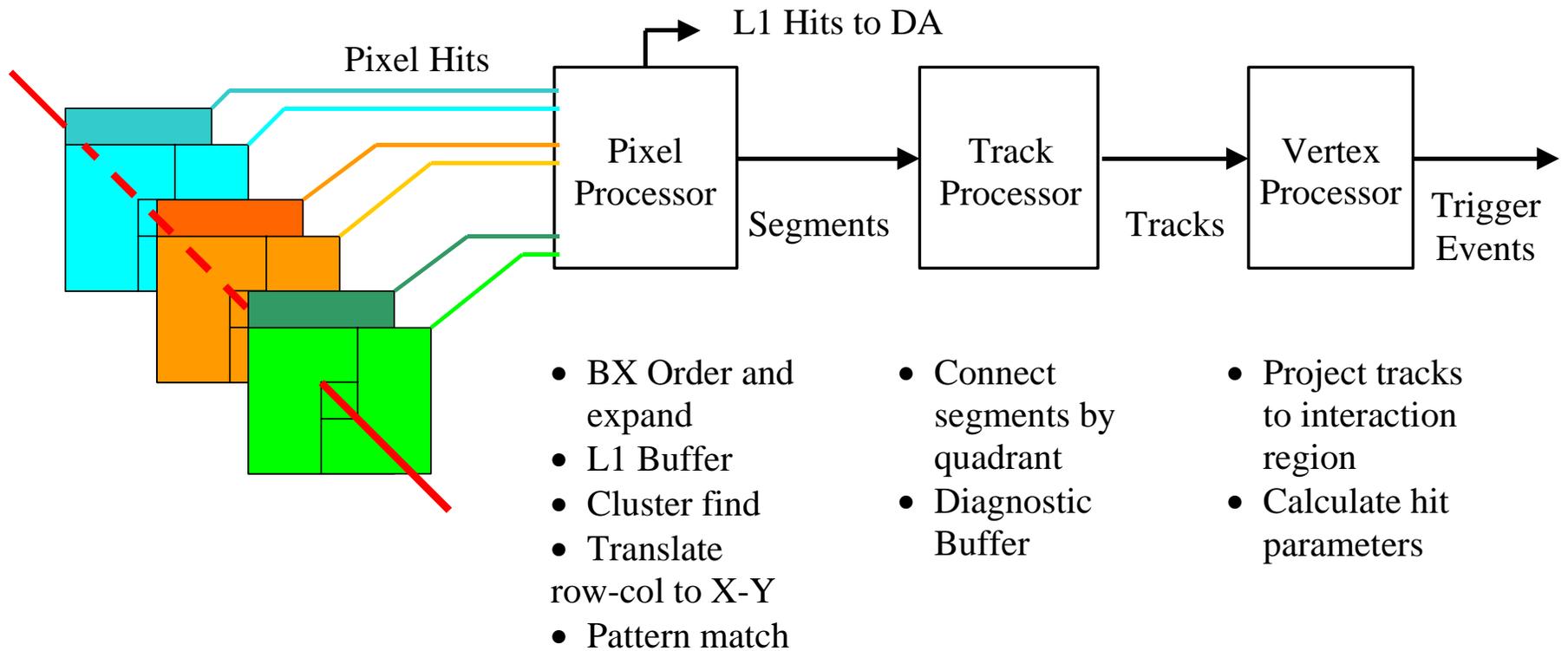
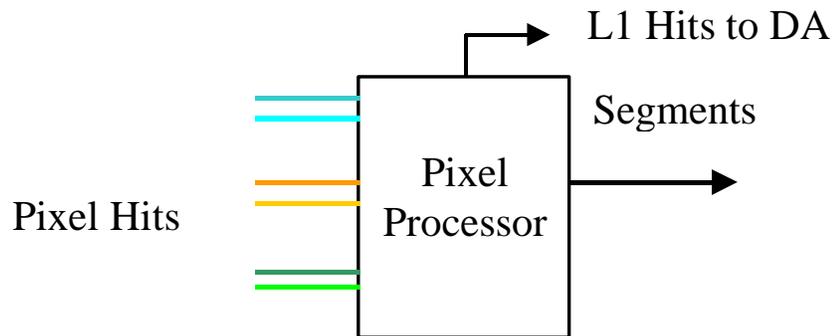


Pixel Trigger





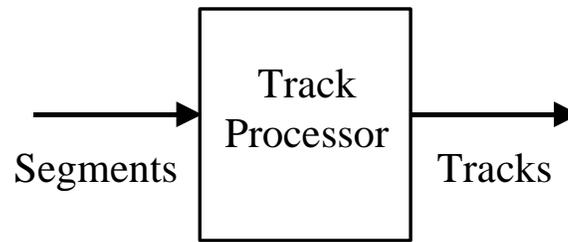
- BX Order and expand
- L1 Buffer
- Cluster find
- Xlate row-col to X-Y
- Pattern match

Current or Permanent:

- Implemented in FPGA.
- FO Links between detector area and trigger and DAQ upstairs.

Options that need more info:

- Hold raw data or translated data in L1 buffer.
- Simple or CENTER-OF-MASS cluster finder? Some analog or all digital data?
- Combine columns data into cluster processing?
- Need to simulate pattern-matching algorithms to select between BB33 and sweep.
- Where to split the hardware upstairs and downstairs?
- Define the dividing line between the pixel and trigger groups' efforts.



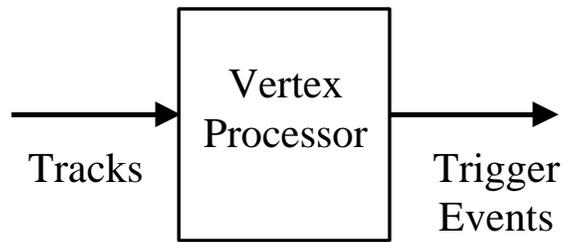
- Connect segments by quadrant
- Diagnostic Buffer

Current or Permanent:

- Implemented in a floating point Digital Signal Processor.

Options that need more info:

- Microprocessor, DSP or neural net?
- Partition as quadrants or in Z?
- Cut segments first or after track finding?
- Remove quadrant segmentation at this step?



- Project tracks to interaction region
- Calculate hit parameters

Current or Permanent:

- Implemented in a floating point Digital Signal Processor.

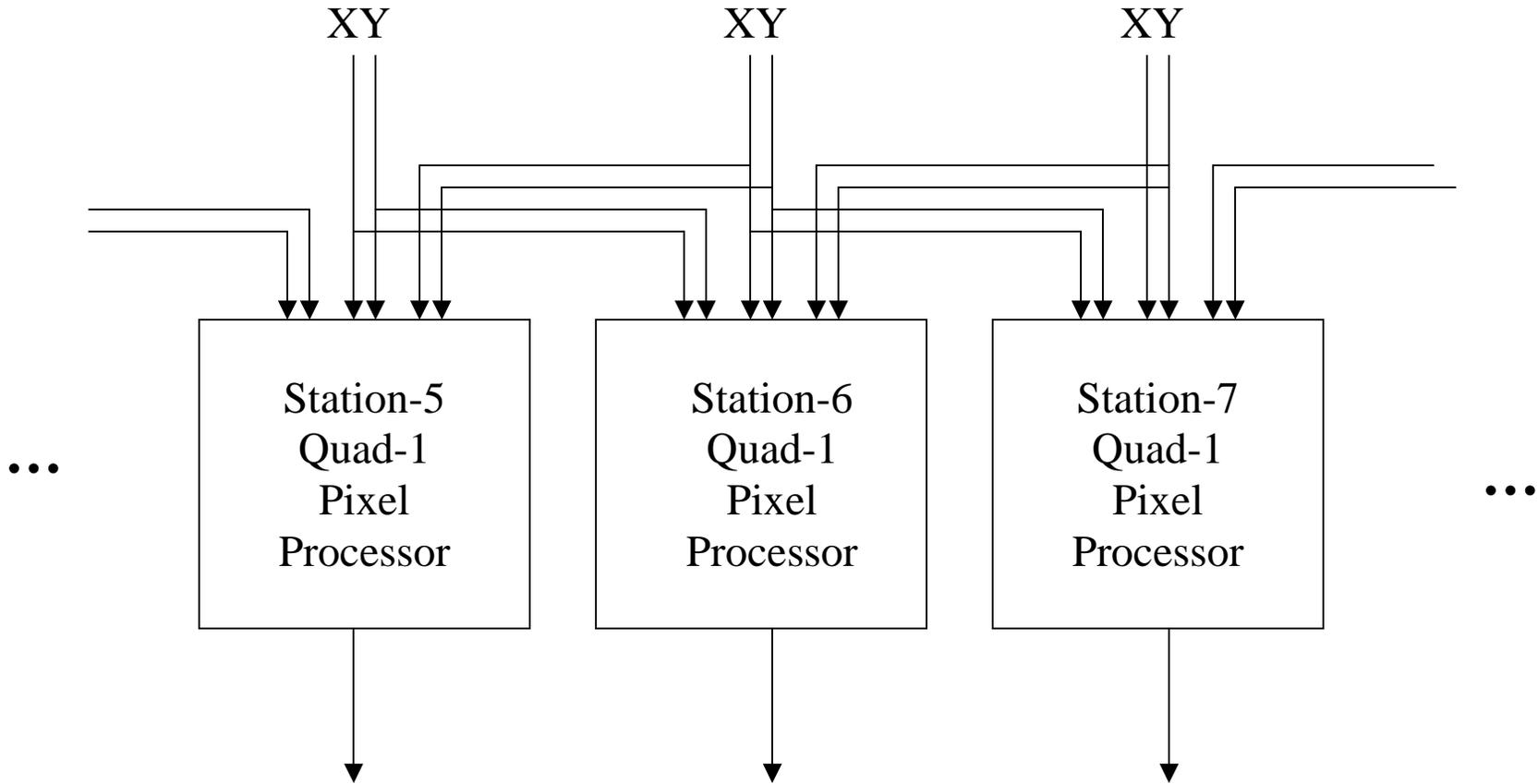
Options that need more info:

- Could this be done in the same fixed point DSP as the track processing?
- What information must the trigger output contain?

Current Efforts:

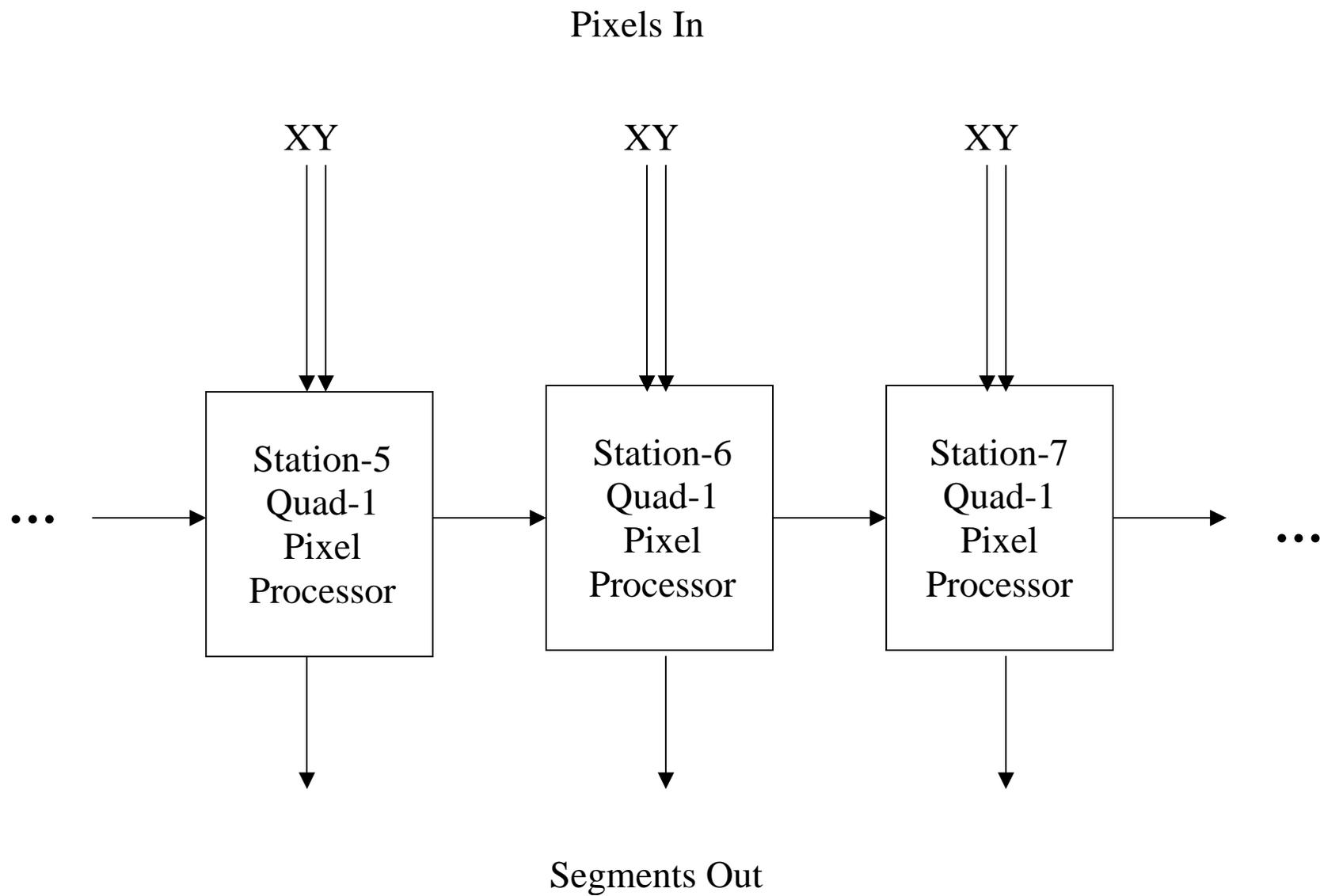
- Simulations of segment algorithms – Erik & Penny
- Data flow and queuing analysis - ESE
- Pixel processor subgroup - Gustavo
- DSP software investigation – Erik.

Pixels In

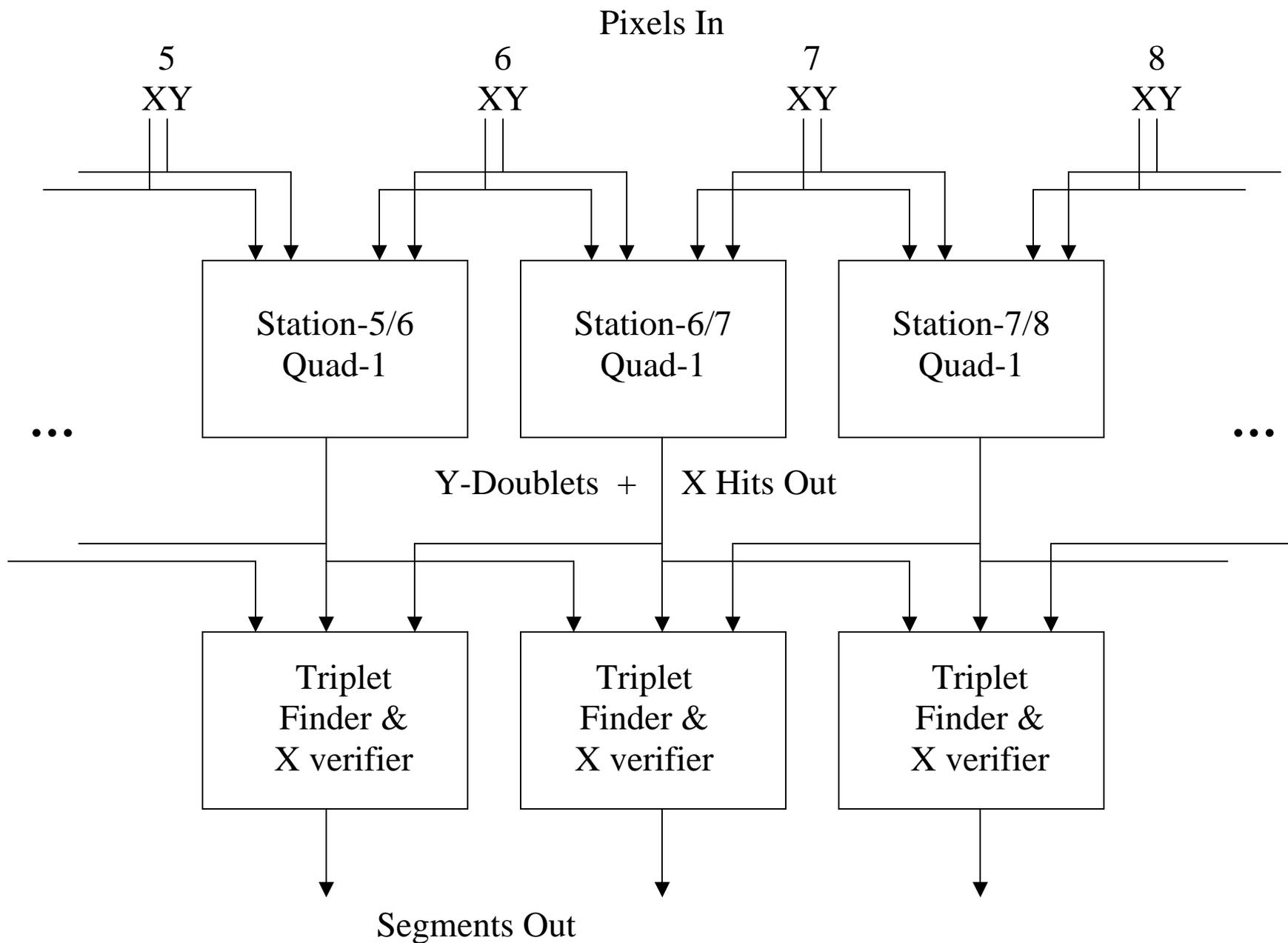


Segments Out

BB33 Algorithm



Sweep Algorithm



Combined Algorithm