

**Fermi National Accelerator Laboratory**

**SVX II Silicon Strip Detector Upgrade Project  
Readout Electronics**

**FIB SUBRACK FANOUT MODULE (FFO)  
Revision B**

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## 1. GENERAL INFORMATION

This document describes and specifies the “FIB Subrack Fanout Module”, hereafter referred to as the FIB Fanout or FFO. The FIB Fanout is a part of the SVXII DAQ system for CDF. This document describes the Revision B (production) PC board. An earlier version of this document, describes the Revision A (prototype) PC board. The two revisions of the FIB Fanout board **are not software compatible. Software written for the Revision A board will not work with the Revision B board.** This document describes the use of the FIB Fanout in a system in which it is interfaced with Fiber Interface Boards (FIBs) through the production version of the J3 Backplane (Rev.C, red in color). The J3 Backplane production version has different pin and slot assignment from the prototype version (Rev.B, green in color). **Caution should be used and an understanding of pinout and slot assignment is needed when using FFO boards with either the production or the prototype version of the J3 Backplane.**

### 1.1 Revisions

September 18<sup>th</sup>, 2002: changes in sections 6.1.2, 6.1.3 and 6.9.

### 1.2 System Introduction

A glossary and a diagram of the SVX Data Acquisition System can be found in Sections 0 and 6.10.

### 1.3 Description of Component & How It Fits Into The System

The FIB Fanout is a 9Ux400 VME card that resides in a Fiber Interface Board (FIB) subrack. The FIB Fanout interfaces to a custom J3 Backplane, the Silicon Readout Controller (SRC) module [Ref.1], and the VMEbus Backplane [Ref.30].

**FIB Fanout in the SVX Data Acquisition System**

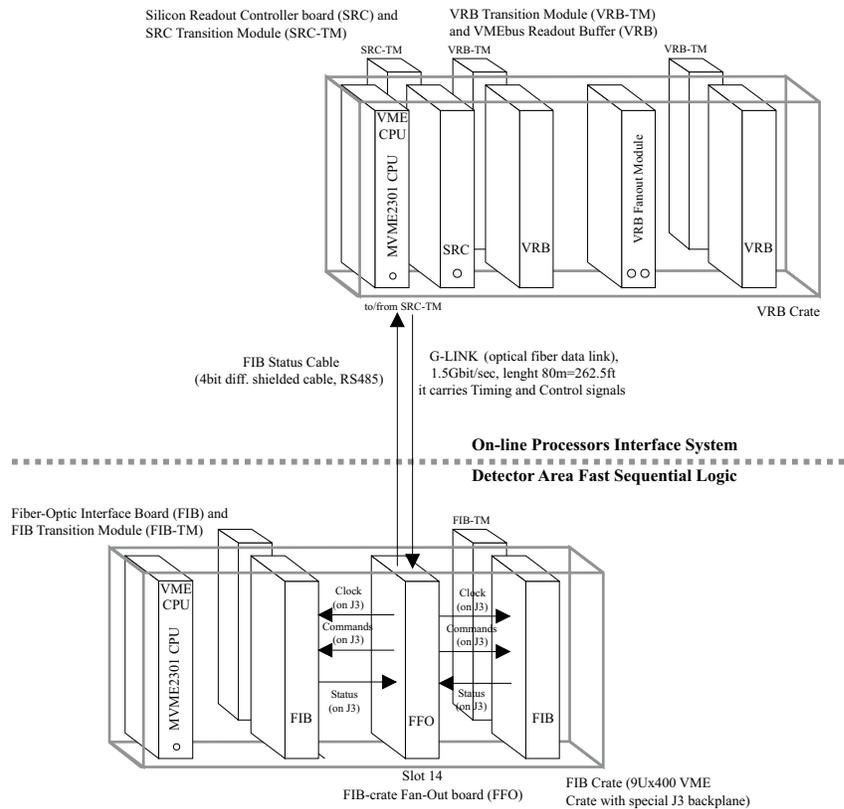


Figure 1.1, FIB Fanout in the SVX DAQ system.

There is a single FIB Fanout module in slot 14 of each FIB subrack. The FIB Fanout module receives commands and timing signals from the SRC module via a fiber optic link (G-Link) [Ref.8, 9, 10, 11, 12, 4] and places them on the J3 Backplane for use by the FIBs [Ref.3]. The VME master in the FIB subrack configures the FIB Fanout.

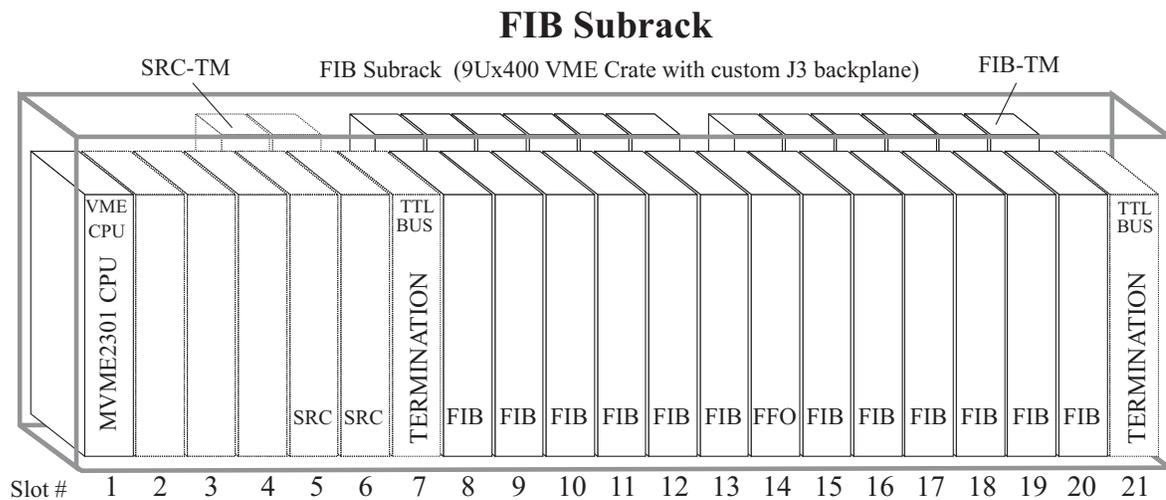


Figure 1.2, FIB subrack.

#### 1.4 List Of Component Requirements

The following is a list of the FIB Fanout requirements:

- 9U x 400mm single width VME module.
- VME slave interface for status and control.
- G-Link receiver daughter card interface for SRC control.
- Interface to custom J3 Backplane for sending control and timing information to FIBs.
- Provide MCLK and SYNC signals to each FIB slot.
- Provide internal test data capability for use with FIB.
- Contain error detection/trace circuitry to flag and save erroneous SRC data transmissions.



The FIB Fanout receives timing and control information from the SRC through an optical link. SRC timing information is conveyed by the optical link word clock itself, which runs at 53 MHz and is the source of the MCLK signal. The rest of the SRC data is presented as a 20-bit word which is placed on the J3 Backplane TTL bus for the FIB modules. In addition, the SYNC bit required by the FIB module to latch commands is extracted from the 20-bit data word and driven over a separate differential ECL low-skew path to each FIB.

At power-on the FIB Fanout will be in “INITIALIZE MODE”. In this mode the FFO drives the MCLK and SYNC signals to the FIB from a local oscillator and a local SYNC generator. The FFO drives the 20-bit data word from a local test FIFO that is used to “blank” (drive low) the J3 TTL data bus. The local Test FIFO can also be used to send command sequences to the FIB.

The data received on the optical link is not relayed to the FIBs until the optical link is in lock and the FIB Fanout receives a predefined sequence of command signals over the optical link. At this point the FFO will switch to “RUN MODE” and the MCLK, the SYNC and the data signals sent to the FIBs will be those received on the optical link.

The FIB Fanout does not change or modify G-Link data before sending it to the FIBs. Determination of whether a command sequence is legitimate or rational is left to the FIB. The FIB Fanout connects to bits 4..0 of the SRC data (the FIB command) to allow the SRC to send FIB Fanout-specific commands (see Table 2.2). According to the FIB specification the FIB responds to command values 0 through 0x37, leaving command values 0x38 through 0x3F available for use by the Fanout. Bits 25..21 of the J3 TTL bus are Open Collector lines (i.e. every FIB can drive one or more of them low) and are used for status communication between the FIBs and the FIB Fanout. The Fanout assumes that the data presented upon these lines shall follow the format given in

Figure 2.4 and Table 2.1.

## 2.2 Physical Interface Descriptions

This section details the signal levels and interfaces used to connect the FIB Fanout to other modules in the SVX system. Pinouts and timing are detailed later.

### 2.2.1 Physical interface from SRC to FIB Fanout

The SRC transmits all data to the FIB Fanout using a Finisar optical transmitter module (G-Link Transmitter) [Ref.9, 10] and a single optical fiber terminated in an ST connector. The FIB Fanout receives this data via a panel-mounted ST connector on the front panel of the Fanout which is connected to a Finisar optical receiver module (G-Link Receiver) [Ref.9, 10].

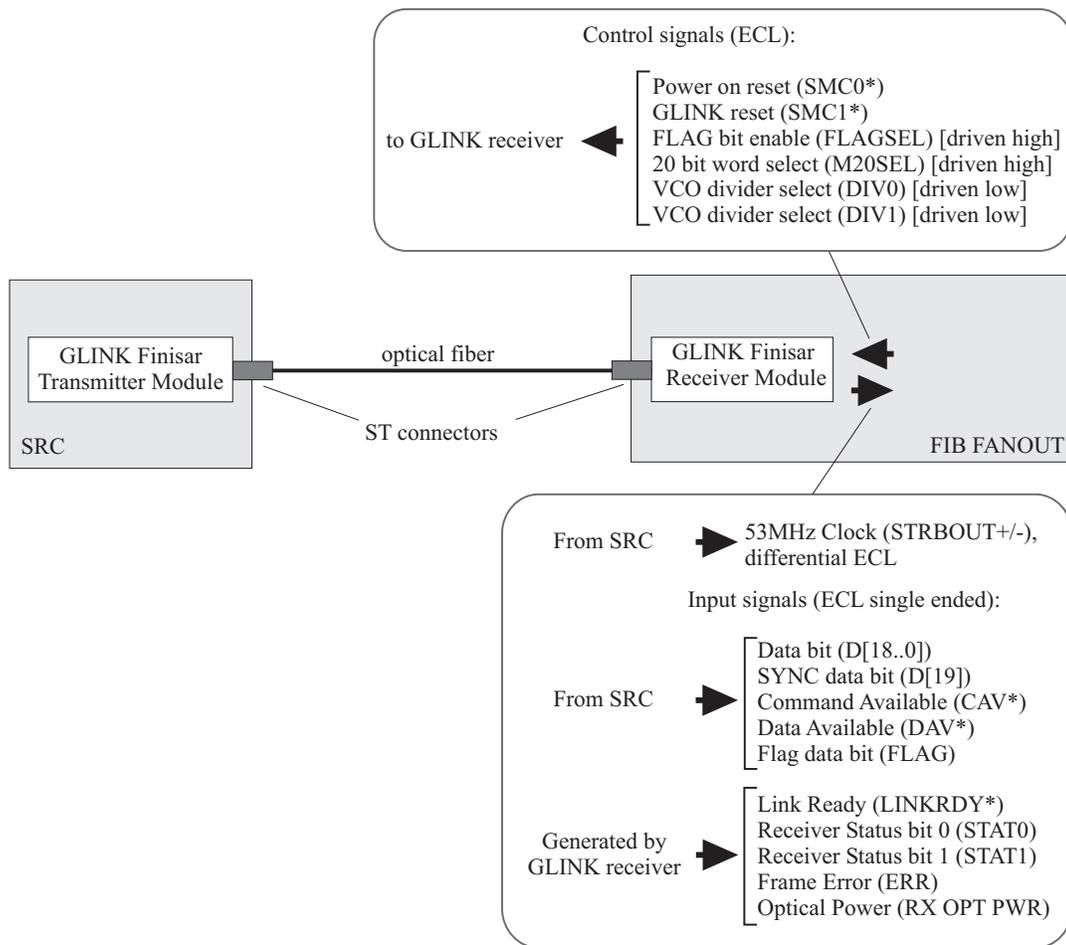


Figure 2.2, Interface from SRC to FIB Fanout.

### 2.2.2 Physical interface from FIB Fanout to SRC

Status data is returned from the FIB Fanout to the SRC via a four-bit shielded cable. RS-485 [Ref.31, 32] signals are sent differentially from the FIB Fanout to the SRC with the meaning of the four bits of Fanout status controlled by values written to the Fanout Status bit mapping registers. Each of the four bits is the logical 'OR' of various error and status conditions as selected by the mapping registers. A bias and termination scheme is assumed to exist within the SRC, which allows the SRC to detect the presence or absence of the cable. The cable may be grounded at the Fanout end to allow return of common-mode currents. The four status bits allow the SRC to monitor different error/status conditions within the Fanout.

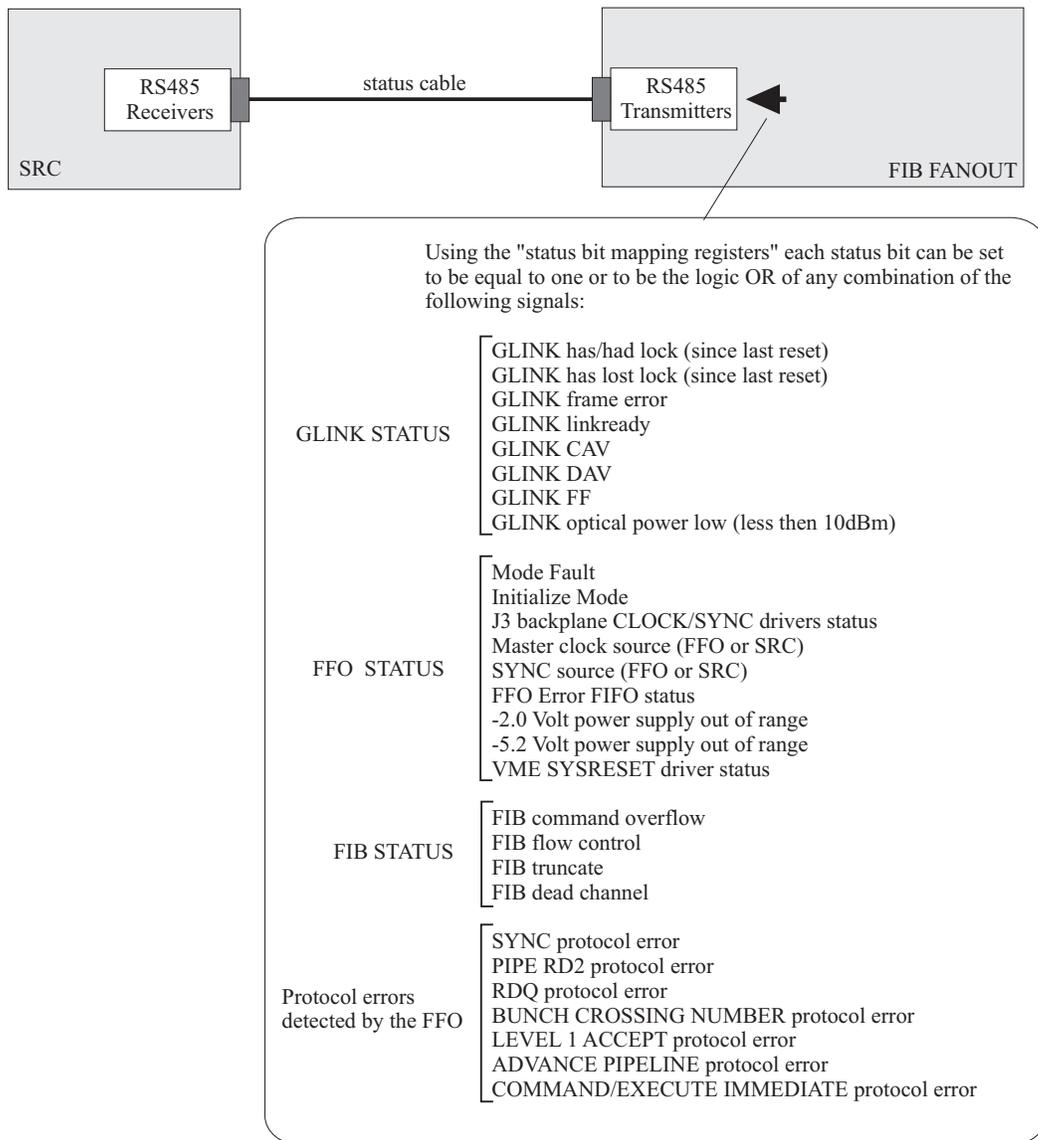


Figure 2.3, Interface from FIB Fanout to SRC.

### 2.2.3 Physical interface from FIB Fanout to FIB

The FIB Fanout drives clock signals and commands to the FIB over a custom J3 Backplane. Clock and SYNC signals are driven via differential 10K ECL lines [Ref.13, 26] point to point to each FIB, impedance-matching termination of the ECL MCLK and SYNC lines is provided by each FIB. The Clock and SYNC signals can be those received from the SRC through the optical link (Fanout in RUN mode) or those generated on the Fanout (Fanout in INITIALIZE mode).

Commands and other information are carried on a TTL bus common to all modules. The current TTL bus termination scheme on the J3 Backplane is an AC type that does not have any power requirements. An optional DC termination scheme can be used, in this case the power for the terminations of the TTL bus is provided by a reserved pin on the FIB Fanout. On the FFO front panel an LED labeled "J3B" is on indicating that power is being supplied to the reserved pin on the Fanout J3 Backplane connector in the event that the DC termination scheme was used.

The TTL bus between the FIB and the FIB Fanout is 25 bits wide as shown in

Figure 2.4 and Table 2.1. The Fanout drives this bus from the center of the Backplane, and both ends are terminated on the Backplane itself. TTL bus bits are numbered 1..25 instead of the more usual 0..24.

SRC commands are carried on bits 1..20, with bit 20 used as a strobe (SYNC signal). Bits 21..25 implement a five-bit status bus (open collector TTL) for communication between the FIBs and the FIB Fanout within the subrack. One bit is reserved for future use, the other four bits are driven by the FIBs and are part of the status signals that can be sent from the Fanout to the SRC on the status cable (if the correct bits are set within the FFO status bit mapping registers). The four status bits driven by the FIBs are open-collector signals, biased with a pull up resistor on the Fanout allowing more than one FIB to assert the status bit at the same time. Assertion of these status bits by the FIBs indicates a system problem that should be addressed by software.

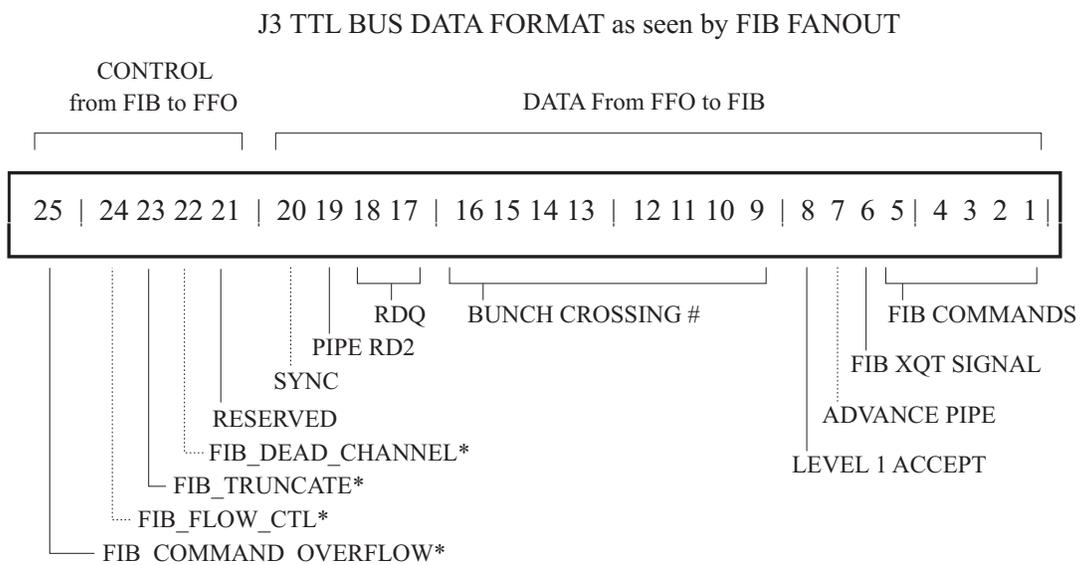


Figure 2.4, TTL Bus Mapping on J3 Backplane

The SRC command signals can be those received from the SRC through the optical link (Fanout in RUN mode) or those driven by the Fanout using the Test FIFO (Fanout in INITIALIZE mode). When the Fanout is in initialize mode and no data is being sent using the Test FIFO the first 19 bits of the 20 bit wide FFO to FIB TTL data bus are blanked (i.e. driven low). The 20th bit is driven with the signal from the local SYNC generator.

Bit #	Signal Name	Direction FFO-FIB	Notes
25	FIB_COMMAND_OVERFLOW*	⇐	Open-collector TTL signal indicating that one or more FIB modules have a command FIFO error.
24	FIB_FLOW_CTL*	⇐	Open-collector TTL signal asserted by FIBs to indicate that SRC should temporarily stop sending commands. Persists for as long as the condition exists within the FIB, minimum persistence 132 nsec. Generated by the 'almost empty' flag (i.e. error condition occurs if FIFO is NOT almost empty) in the FIB command FIFO.
23	FIB_TRUNCATE*	⇐	Open-collector TTL signal asserted by FIBs to indicate that an event was truncated. Persists for minimum 50 nsec.
22	FIB_DEAD_CHANNEL*	⇐	Open-collector TTL signal asserted by FIBs to indicate that one or more input pipelines had no data at all, requiring update of the FIB channel masks. Persists for no less than 50 nsec.
21	RESERVED	-	Unused TTL data bit.
20	SYNC	⇒	TTL bus bit 20. Driven by FFO by the same signal used to drive the ECL SYNC bit, it is unused by FIB. The SYNC signal is driven by the Local SYNC during "INIT MODE" and with the corresponding data bit received from the SRC (through G-Link) during "RUN MODE".
19	Pipe_RD2	⇒	TTL bus bit 19. Driven by FFO with the Test Data (if the feature is enabled) during "INIT MODE", and with the corresponding data bit received from the SRC (through G-Link) during "RUN MODE".
18..17	RDQ (Read-Digitize-Quiescent)	⇒	TTL bus bits 18..17. Same as above.
16..9	Bunch Crossing Number	⇒	TTL bus bits 16..9. Same as above.
8	Level 1 Accept	⇒	TTL bus bit 8. Same as above.
7	Advance_Pipeline	⇒	TTL bus bit 7. Same as above.
6	FIB XQT signal	⇒	TTL bus bit 6. Same as above.
5..1	FIB Command	⇒	TTL bus bits 5..1. Same as above.

Table 2.1, TTL Bus Mapping on J3 Backplane

### 2.2.4 RUN Sequence

As previously stated, the Fanout has two modes of operation, "run mode" and "initialize mode". The module powers up in initialize mode. In this mode the user may, through software (VME), access the module registers to read status (optical link status, power supply status, module temperature, etc..) and write register settings. Different types of test data sequences can be sent to the FIBs using the FFO Test FIFO. While the module is in the initialize mode the MCLK and SYNC signals sent to the FIBs are derived from a local oscillator and a local SYNC generator. To switch to run mode the optical link (G-Link) must be locked and the Fanout must receive the RUN signal. The RUN signal is actually a sequence of signals (as described in the next paragraph) from the SRC via the optical link or a command issued by software through a register (diagnostic register). If the Fanout is in run mode and the G-Link lock is lost the Fanout will return in initialize mode.

### 2.2.5 RUN mode via the SRC

Handshake protocol between the FFO and the SRC during the "lock acquisition" phase (using the 4-bit Status Cable) has not been defined yet. The Status cable is only used to send error information to the SRC as set in the Error Mapping Registers. Regarding the optical link, it's important to know that there are two types of fill frames the G-Link Transmitter can send, fill frame 1 and fill frame 0; refer to Figure 2.5 or to [Ref.8, 9, 10, 11, 12]. If the optical link lock is lost at any time the FFO will return in Initialize mode.

1. The Fanout module is driving MCLK and SYNC to the FIBs via the internal oscillator and SYNC generator.
2. The SRC G-Link transmitter starts sending "fill frame 1's" when the Fanout's G-Link Receiver state machine (see Figure 2.5) switches from state 0 to state 1 and then state 2. When the G-Link receiver state machine is in state 2 the G-Link is considered "in lock" and the G-Link Receiver has set the "link ready" signal.
3. The SRC asserts data values (0's or No-operation) onto the G-Link with the CAV\* (Command Available, active low) asserted and the DAV\* (Data Available, active low) line not asserted, indicating a control value as opposed to a FIB command. This condition is held for at least one full command frame (seven G-Link clock ticks), at which point the CAV\* is released and the DAV\* is asserted, with the data value equal to zero (no-op). The CAV\* pulse is considered by the FFO as a "RUN mode request".
4. Receipt of the CAV\* pulse (at least 7 clock ticks long) initiates the switching of the CLOCK/SYNC/DATA from the local signals (internal 53MHz oscillator, internal SYNC generator, Test FIFO data) to the G-Link signals (53MHz Master Clock, SYNC and SRC data).
5. The Fanout module waits for the DAV\* signal to be true and for a falling edge of the G-Link SYNC signal to complete the switching process. The G-Link CLOCK/SYNC/DATA then start driving the J3 Backplane to the FIBs.
6. At the FIB end, the FIB command processor first sees the SYNC end, then a pause in the MCLK, the MCLK resuming and then resumption of the SYNC. The Fanout insures that the MCLK drivers are disabled and then re-enabled with the MCLK at the same phase to avoid clock glitches at the FIBs.

### 2.2.6 RUN mode via other G-Link sources such as the General System Test Module (GSTM)

The steps are the same as if the SRC is used (previous paragraph; RUN mode via the SRC) but some different settings can be used:

- 1 The Fanout is driving MCLK and SYNC to the FIBs via the internal oscillator and SYNC generator.
- 2 The G-Link transmitter starts sending "fill frames 1". The Fanout's G-Link Receiver state machine (see Figure 2.5) switches from state 0 to state 1 and then to state 2. When the G-Link receiver state machine is in state 2 the G-Link is considered "in lock" and the G-Link Receiver sets the "link ready" signal.
- 3 The G-Link source asserts data values (0s or No-operation) onto the G-Link with the CAV\* (Command Available, active low) asserted and the DAV\* (Data Available, active low) line not asserted, indicating a control value as opposed to a FIB command. This condition is held for at least one full command frame (seven G-Link clock ticks), at which point the CAV\* is released and the DAV\* is asserted, with the data value equal to zero (no-op). The CAV\* pulse is considered by the FFO as a RUN mode request. The same effect can be obtained sending a "RUN mode request" through VME (diagnostic register bit 31).
- 4 Receipt of the CAV\* pulse (at least 7 clock ticks long) or a VME RUN request initiates the switching of the CLOCK/SYNC/DATA from the local signals (internal 53MHz oscillator, internal SYNC generator, Test FIFO data) to the G-Link signals (53MHz Master Clock, SYNC and SRC data).
- 5 The Fanout waits for the DAV\* signal to be true and for a falling edge of the G-Link SYNC signal to complete the switching process. The G-Link CLOCK/SYNC/DATA then starts driving the J3 Backplane to the FIBs. The diagnostic register allows these options:
  - a) The DAV\* wait to be disabled by setting bit 15.
  - b) Use of the local SYNC instead of the G-Link SYNC (bit 20 of G-Link data) by setting bit 16.

The change in the diagnostic register should be done before starting the run mode initialization sequence.

- 6 At the FIB end, the FIB command processor first sees the SYNC stop, then a pause in the MCLK, the MCLK resuming and then resumption of the SYNC. The Fanout insures that the MCLK drivers are disabled and then re-enabled at the same phase of MCLK to insure that there are no clock glitches at the FIB end.

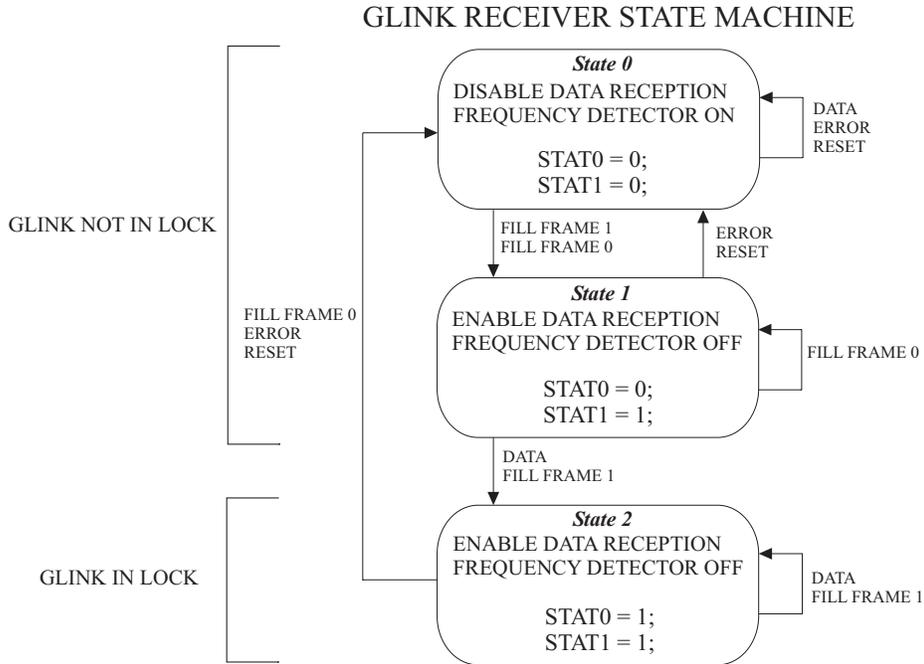


Figure 2.5, G-Link Receiver State Machine

**2.2.7 Recovery from the RUN mode back to the INIT mode**

Once the Fanout is in the RUN mode the expectation is that this mode will persist indefinitely. However, other system error conditions may require that the Fanout be returned back to INIT mode. Receipt of a command from the SRC (command 0x3D, see Table 2.2) will advance the FFO state machines back to INIT mode. The FFO can be forced into INIT mode using the diagnostic register (bit 30). Another way to force INIT mode is to reset the FFO clock controller (diagnostic register bit 24); however, this method will not produce a clean transition and should only be used when performing a full system reset. If during RUN mode the G-Link lock is lost the Fanout will return to INIT mode.

### 2.3 Diagnostic Features

The Fanout provides diagnostic information regarding the validity of data transferred over the G-Link and other meaningful error/status conditions. The Fanout is capable of detecting the following error conditions:

- 1) Bit errors in any of the 19 data bits transmitted over the G-Link within an SRC frame. With the exception of the SYNC bit, all data bits should be repeated seven times within a single frame. The Fanout uses a pipeline comparator to detect transitions within a frame and report an error if the data received from the SRC does not comply with the timing protocol (Figure 2.6, Master clock, data timing and frame structure.), these types of errors are considered "protocol errors".
- 2) Bit errors within the SYNC signal. In an SRC frame of seven G-Link data words, the SYNC is defined to be a '0' for the first five words, and a '1' in the last two. If this pattern is not found within an SRC frame a SYNC error is detected. This type of error is considered a "protocol error".
- 3) G-Link frame errors detected by the optical receiver.
- 4) Insufficient optical power received by G-Link receiver. A LED on the front panel of the Fanout provides visual indication and a bit in the Fanout error status register is set if the optical power received by the G-Link receiver is less than 10dBm. An accurate value of the optical power can be obtained from Fanout diagnostic register using the on-module ADC.
- 5) -5.2 Volt and -2.0 Volt power supply voltage out-of-range errors. Voltage comparators provide "out of range" information through the Fanout error status register. More precise indication of the power supply status can be obtained from Fanout diagnostic register using the on-board ADC.
- 6) Power supply failure of the -5.2 Volt, -2.0 Volt (generated on board by a voltage regulator using the -5.2 Volt power supply) and +5.0 Volt power supplies due to FFO over-voltage/over-current circuit protection intervention or to a failure within the VME subrack. LEDs on the front panel of the Fanout provide visual indication of the power supply status. A +5.0 Volt supply failure may only be sensed via the SRC by way of the status cable, as failure of the +5.0 Volt supply will disable the Fanout.
- 7) FIB errors, received on the J3 Backplane TTL open collector bus from the FIBs.

Protocol errors (i.e. errors mentioned in 1 and 2 above) can be stored in an Error FIFO which records pre and post-error data. The Error FIFO can be triggered by a protocol error if the feature is enabled through the Fanout diagnostic register (bit 23). Once an error is trapped the Error FIFO holds the trace until explicitly cleared by a VME access.

### 2.3.1 Test FIFO

The Fanout can provide clocks and data for FIB testing. When in INITIALIZE mode the Fanout drives the J3 Backplane with on-board generated 53MHz clock and SYNC and blanks (i.e. drives low) the J3 Backplane TTL data bus. The J3 TTL Data bus can be driven with data from the Fanout Test FIFO. The Test FIFO can supply up to 8192 words of test data (one word per 53MHz clock tick). The data can be written to the Test FIFO through a read only register (Fanout Test FIFO register).

The Test FIFO can be used in three different ways:

- 1) Immediate single command/data word read. This mode is used to write a single word in the Test FIFO and execute an immediate single word read. The word read will then be kept on the bus for one full command cycle (7 clocks) and the Test FIFO will be reset and the J3 TTL bus blanked (driven low).
- 2) Single command/data sequence read. This mode allows one to store and send a command/data sequence to the FIBs. At the end of the sequence the Test FIFO will be reset and the J3 TTL bus blanked (driven low).
- 3) Repetitive command/data sequence read (loop mode). This mode allows one to store and repetitively send a command/data sequence to the FIBs. When the mode is stopped (by a VME access) the Test FIFO will be reset and the J3 TTL bus blanked (driven low).

Detailed examples of the Test FIFO use are provided in Section 6.1.

**2.3.2 Protocol Error Detection (data frame and SYNC)**

All 20 bits of TEST FIFO/G-Link data, previously described, enter an error detection pipeline. The pipeline shifts with each 53 MHz clock tick (local clock in INITIALIZE mode, G-Link clock in RUN mode) and a comparator is used to detect bit transitions in the various bit fields of the data. Each of the bit field groups (defined in Table 2.1 and shown in

Figure 2.4) are sampled seven times within a single SRC frame. Bit errors in any group are routed from the protocol error detector to the Fanout error status register. The same bit errors are routed to the Fanout status bit mapping registers for inclusion in the four status bits returned by the Fanout to the SRC (on the RS-485 status cable). In addition, the protocol errors are priority encoded and sent to the Error FIFO for later readout over VME. Any protocol error (data bits or SYNC bit) is used to trigger the Error FIFO to save the current data stream.

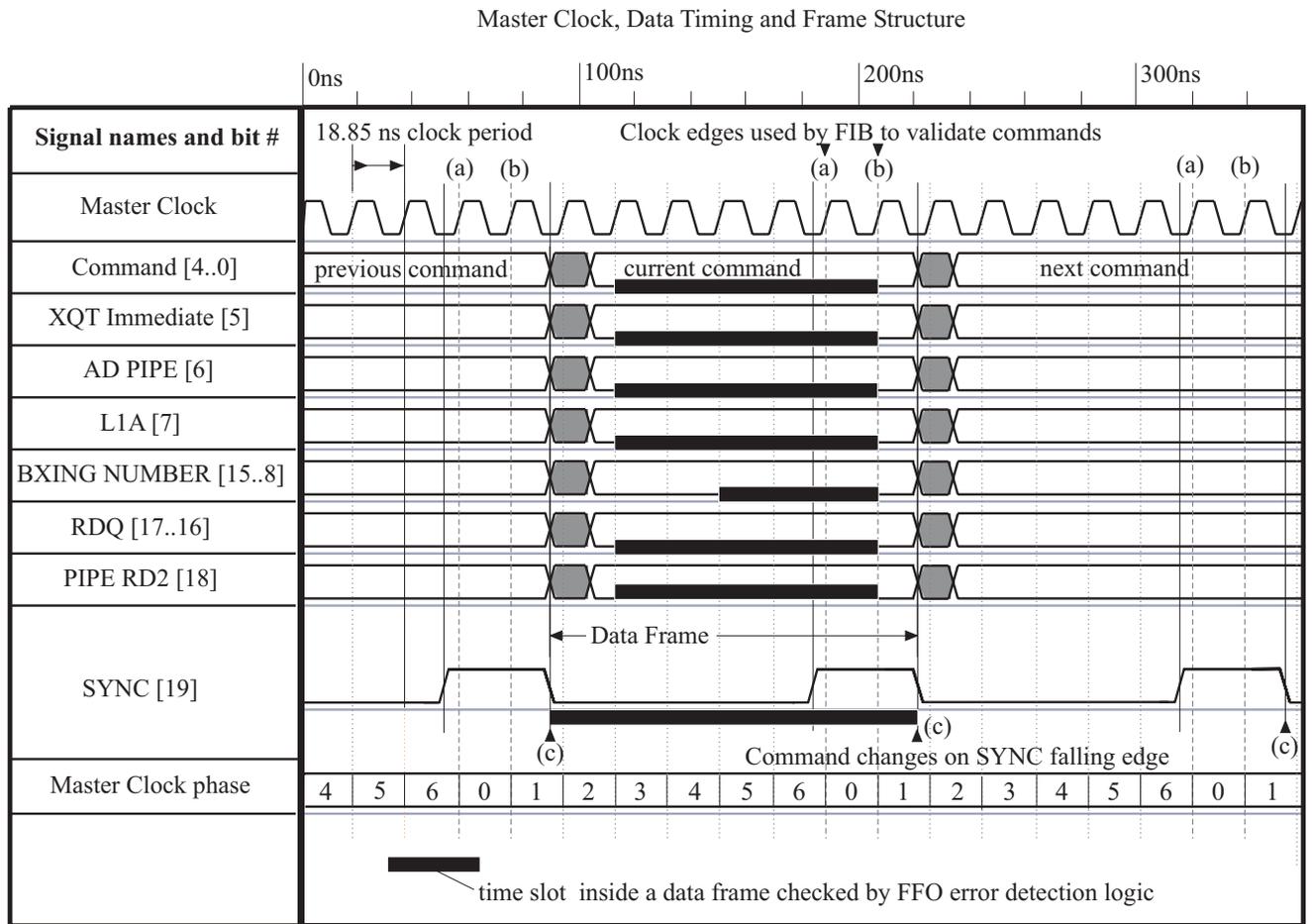


Figure 2.6, Master clock, data timing and frame structure.

The data protocol error detection pipeline is designed around a seven-word frame (Figure 2.6). Data is entered in to the error detection pipeline with every 53MHz clock tick. The data should only change during master clock phase 2. The SYNC pulse (bit 19 of data[19..0]) is used as a reference to determine the master clock phase. The FIB latches the command two times as frame phases 0 and 1 start (time "a" and "b" in Figure 2.6), the two results are compared and the command is executed only if they matched. The Fanout not only samples the data at the time the FIB (beginning of frame phases 0 and 1)

does but also in the four frame phases preceding them (3, 4, 5, 6). One exception to this rule is the Bunch Crossing signal which is sampled only at the beginning of four frame phases (5, 6, 0, 1). The bunch crossing difference is done to compensate for a shortcoming in the SRC board the do not allow the SRC to respect the communication protocol.

A secondary pipeline is used to detect errors in the SYNC signal. It is implemented as a seven-bit shift register that saves the state of the SYNC (1 or 0) at every 53MHz clock tick. For any data frame (set of seven words) two and only two of the SYNC bits in the register may be asserted. Any other combination is indicative of a SYNC error.

The Fanout can only detect protocol errors, it cannot prevent the transmission of a bad data frames or SYNC pulses to the FIB.

### 2.3.3 Error Trace FIFO

The Error FIFO can be used in three different ways:

- 1) Protocol Error Detection Mode. As previously stated the Fanout also provides a test FIFO that is capable of driving the J3 Backplane TTL data bus when no optical driver (G-Link Transmitter on SRC/GSTM) is present in the system or when the Fanout is in INITIALIZE mode. If enabled the error detection logic will work both in INITIALIZE mode (data frames from test FIFO) and in RUN mode (data frames from SRC through the optical link). If the protocol error detection logic is armed (Fanout diagnostic register bit 23) the error trace FIFO will continually memorize the data from the G-Link/Test FIFO. Whenever the error detection circuitry detects that any form of data transfer error has occurred the error FIFO will stop after another 1000 writes. This will leave a data trace in the error FIFO containing 7185 words of pre-trigger and 1000 words of post-trigger data. When the Protocol Error Detection Mode armed the error FIFO is reset and the Test Mode is disabled.
- 2) Test Mode. The error FIFO can be enabled to store only the sequence driven by the Test FIFO on the TTL data bus allowing checking if test FIFO is working properly. This mode can be armed by VME (Fanout diagnostic register bit 17). The error FIFO will stop memorizing data when almost full (8185 words) or when the test FIFO stops. When the Test Mode is armed the Error FIFO is reset and the Protocol Error Detection Mode is disabled.
- 3) VME Trigger. Bit 15 in the Fanout diagnostic register allows software to trigger the Error FIFO, causing the FIFO to act as a transaction capture memory. The error FIFO memorize 7185 words of pre-trigger and 1000 words of post-trigger data. The VME trigger can also be used when the Protocol Error Detection Mode or the Test Mode are armed. In the first case the Error FIFO will behave like a protocol error occurred (7185 words of pre-trigger and 1000 words of post-trigger data). If the Test Mode is armed the error FIFO will stop memorizing data when almost full (8185 words).

Detailed examples of the error FIFO use are provided in Section 6.1.

Once an error/sequence has been trapped by the error FIFO, the FIFO is disabled until it is explicitly re-armed or triggered by a VME write (diagnostic register bit 23, 17, 15). The entire data trace may be read out over VME (error trace FIFO register) after the error/trigger has occurred.

G-Link/Test FIFO protocol errors are priority encoded such that higher value errors will override lower value errors in the error FIFO (see Figure 3.8, Error FIFO register data format.). Should multiple



The out of range error, as any error mapped in the Fanout error status register, can be included (using the Fanout status bit mapping registers) in the OR function used to generate the four status bits returned by the Fanout to the SRC on the RS-485 status cable.

An accurate value of the voltages can be obtained using the on-board multi-channel ADC that is controlled by the Fanout diagnostic register.

The FIB Fanout assumes that  $-5.2$  Volts is presented to modules in the VIPA compatible subrack via the Vw, Vx and Vy pins of the J0 connector.

### **2.3.5 Optical Power Monitor**

An analog to digital converter (ADC) allows monitoring the analog optical power output of the Finisar G-Link receiver via the diagnostic register. Comparison with a reference value will trigger an error if the optical power drops below threshold (set to 10dBm). If the error condition is triggered an LED on the front panel will provide "optical power low" error visual indication and a bit in the Fanout error status register will be set.

The optical power low error, as any error mapped in the Fanout error status register, can be included (using the Fanout status bit mapping registers) in the OR function used to generate the four status bits returned by the Fanout to the SRC on the RS-485 status cable.

An accurate value of the optical power can be obtained using the on-board multi-channel ADC that is controlled by the Fanout diagnostic register. See Fanout diagnostic register description in Section 3.1.5 for more detailed information on optical power reading using the multi-channel ADC.

### **2.3.6 J3 Backplane Monitor Register**

The Fanout J3 Backplane monitor register allows the contents of the J3 Backplane TTL bus to be read back via a VME cycle. Being that a VME cycle is longer than a 53MHz clock period the register is able to provide only a snapshot of the current J3 TTL bus status. See Section 3.1.5 for a detailed register description.

### **2.3.7 Temperature Monitoring**

Two temperature sensors (one at the top and one at the bottom of the FFO module) allow software to remotely monitor the temperature on the FIB Fanout. The value of the temperature can be read from the Fanout diagnostic register using the on-board multi-channel ADC. See Fanout diagnostic register description in Section 3.1.5 for more detailed information on temperature reading using the multi-channel ADC.

### **2.3.8 On-board identification**

Two read-only registers are provided in the FIB Fanout, which identify a module uniquely, they are the Fanout identification register and the Fanout tracking register. The first contains an SVX ID code and module identity data. The second register contains the FNAL PREP tag number assigned that particular module.

### 2.3.9 SRC Commands specific to the FIB Fanout

The SRC sends commands numbered from 0x00 to 0x3F to the FIB subrack on the lower six bits of the G-Link data stream. The Fanout logic is designed to respond to command numbers 0x38 through 0x3F as Fanout-specific commands. The assumption is that these commands are treated as no-ops by the FIBs in the same subrack.

SRC command	Interpretation by Fanout
0x38	Create a 250msec pulse on VME SYSRESET* line to reset local CPU. This feature needs to be enabled through the Diagnostic Register (bit 22). The same 250msec pulse always (without the need to be enabled) drives the front panel lemo connector labeled "RESET OUT" allowing the reset of the local CPU by wire.
0x39	Reserved for future use.
0x3A	Force all four SRC status bits to '1'.
0x3B	Force all four SRC status bits to '0'.
0x3C	Allow all four SRC status bits to return to normal reporting mode (clear the effects of commands 0x3A and 0x3B).
0x3D	Request Fanout to return back to INITIALIZE mode.
0x3E	Resets all latched error conditions in Fanout error detection logic. See description of Fanout individual error status register and Fanout status bit mapping registers.
0x3F	Reserved for future use.

Table 2.2, SRC commands specific to the FIB Fanout.

### 2.4 FIB Fanout response to error conditions during RUN mode

The status lines (RS-485 status cable) will change state when errors occur according to the current Fanout status bit mapping register setting. In the event of a protocol error the error trace FIFO will capture data if the protocol error detection logic is enabled (Fanout diagnostic register bit 23). The FIB Fanout does not stop the clock or otherwise interfere with command flow from SRC to FIB. Reaction to detected errors is the sole responsibility of the SRC and software. Only when the optical link lock is lost will the Fanout switch from RUN mode to Initialize Mode, driving the J3 Backplane with on-board generated 53MHz clock and SYNC and blanking the J3 TTL command/data bus.

### 3. INTERFACE SPECIFICATIONS

The FIB Fanout has a A32:D32 VMEbus [Ref.30] slave interface. In accordance with SVX specifications no support of A24/Dxx, A32/D16 or A32/D08 transactions is provided. The FIB Fanout does not generate VMEbus errors or interrupts. The FIB Fanout responds to the following Address Modifiers:

AM Code	Function
0x0A	A32 Supervisory Data Access
0x09	A32 Non-Privileged Data Access

Table 3.1, Address modifiers recognized by the FIB Fanout.

The FIB Fanout has no CR or CSR locations.

The FIB Fanout derives its base VME address from the Geographic Address pins of the subrack. Table [3.2] shows the SVX Module Geographic Addressing Map.

Addressing space	Base address	Slot use in FIB Subrack
unused	ox 0000 0000	--
Slot 1	ox 0800 0000	CPU
Slot 2	ox 1000 0000	
Slot 3	ox 1800 0000	
Slot 4	ox 2000 0000	
Slot 5	ox 2800 0000	SRC module
Slot 6	ox 3000 0000	SRC module
Slot 7	ox 3800 0000	TTL bus termination, no module.
Slot 8	ox 4000 0000	FIB module
Slot 9	ox 4800 0000	FIB module
Slot 10	ox 5000 0000	FIB module
Slot 11	ox 5800 0000	FIB module
Slot 12	ox 6000 0000	FIB module
Slot 13	ox 6800 0000	FIB module
Slot 14	ox 7000 0000	Fib Fanout module
Slot 15	ox 7800 0000	FIB module
Slot 16	ox 8000 0000	FIB module
Slot 17	ox 8800 0000	FIB module
Slot 18	ox 9000 0000	FIB module
Slot 19	ox 9800 0000	FIB module
Slot 20	ox a000 0000	FIB module
Slot 21	ox a800 0000	TTL bus termination, no module.
unused	ox b000 0000 to ox FFFF FFFF	--

Table 3.2, SVX Module Geographic Addressing Map.

### 3.1 VME Data Space Description

The FIB Fanout provides twelve 32-bit wide register locations in data space as described in the following subsections. Table 3.3 shows the data space address map.

<b>Register</b>	<b>Access</b>	<b>Address</b>
Fanout Identification Register	read only	0x0000
Fanout Tracking Register	read only	0x0004
Fanout Status Bit 0 Mapping Register	read/write	0x0008
Fanout Status Bit 1 Mapping Register	read/write	0x000C
Fanout Status Bit 2 Mapping Register	read/write	0x0010
Fanout Status Bit 3 Mapping Register	read/write	0x0014
Fanout J3 Backplane Monitor Register	read only	0x0018
Test FIFO Register	write only	0x001C and 0x0030
Fanout Diagnostic Control Register	read/write	0x0020
Fanout Status Register	read only	0x0024
Error Trace FIFO	read only	0x0028
Individual Error Status Register	read only	0x002C
Non Volatile RAM	read/write	0x2000 to 0x3FFC

Table 3.3, VME Data space address map.



### 3.1.3 Fanout J3 Backplane Monitor Register: relative address 0x0018

This read-only register provides a snapshot of the current information on the J3 Backplane. The register is located within the ispGDX chip and reflects the data on the module's internal GLD bus. The J3 Backplane Monitor Register is intended for system commissioning purposes, where data is sent very slowly allowing the processor to see each word as it is sent. As the G-Link data is only 20 bits wide, the remaining 12 bits are used to display FIB and G-Link status as given in Table 3.5.

J3 Monitor Register VME Address: 0x0018 (READ ONLY)

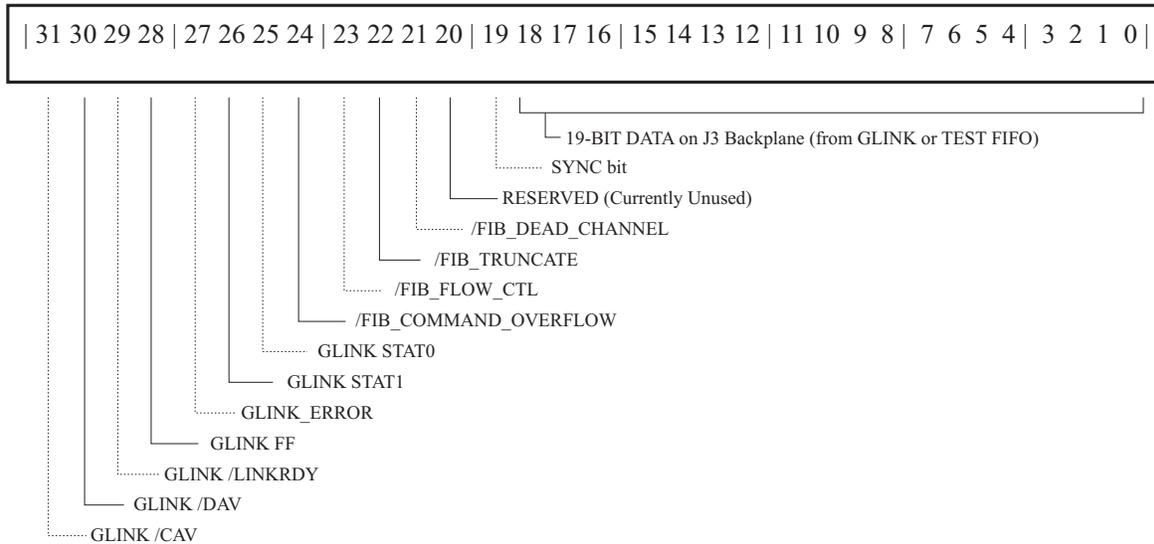


Figure 3.3, Fanout J3 monitor register.

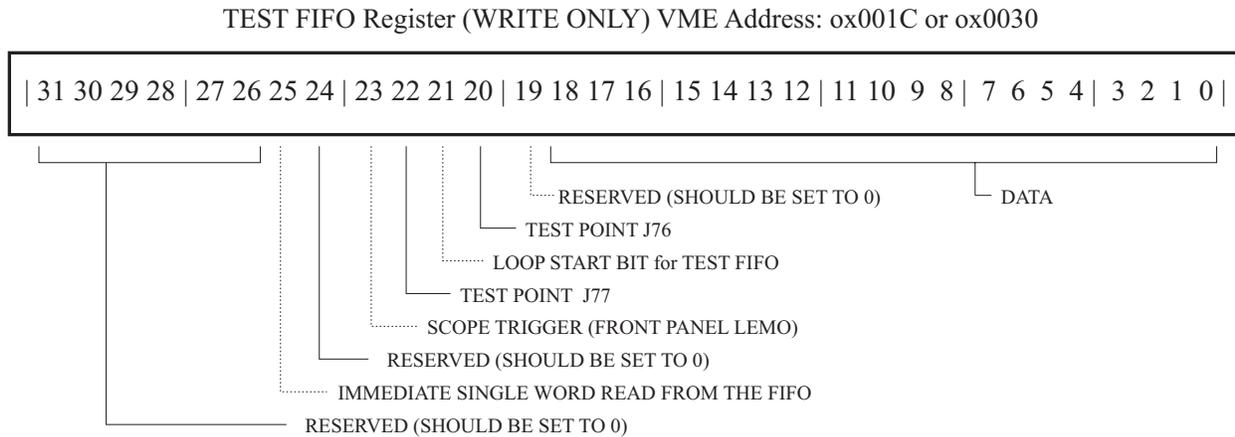
Bit	Meaning
31	CAV* status from G-Link
30	DAV* status from G-Link
29	LINKRDY* status from G-Link
28	FF status from G-Link
27	ERROR status from G-Link
26	STAT1 status from G-Link
25	STAT0 status from G-Link
24	FIB_COMMAND_OVERFLOW* from FIBs
23	FIB_FLOW_CTL* from FIBs
22	FIB_TRUNCATE* from FIBs
21	FIB_DEAD_CHANNEL* from FIBs
20	Readback of reserved bit
19	SYNC bit from G-Link or local SYNC generator.
18..0	20-bit data as asserted by G-Link or Test FIFO on J3 Backplane

Table 3.5, Fanout J3 monitor register bit assignment.

### 3.1.4 Test FIFO Register : relative address 0x001C or 0x0030

This write-only register provides access to load the Test FIFO. The Test FIFO is loaded from VME and, at user request, transmitted over the J3 Backplane to the FIB, taking the place of data received from the SRC over the optical link. The Test FIFO may only drive the Backplane if the Fanout is in INITIALIZE mode. Test FIFO data is clocked out by the local 53 MHz clock and is synchronized to the locally generated SYNC pulse such that the first and the last data values output by the Test FIFO occur synchronous to the falling edge of the locally generated SYNC.

All the SRC commands specific to the FIB Fanout (see Table 2.2) can be used in the Test FIFO and will be recognized and executed by it.



As described in Section 2.3.1 the Test FIFO can be used in three different ways: immediate single command/data word read, single command/data sequence read and repetitive command/data sequence read (loop mode). Detailed examples of Test FIFO operation are provided in Section 6.

The Test FIFO is 24 bits wide, with only bits 0..18 actually connected to the J3 Backplane. Some of the remaining bits are reserved for control flags:

- Bit 21 is a ‘loop start’ bit. If the ‘loop mode’ bit is set in the Diagnostic Control register, all data after the first word with the ‘loop start’ bit set is wrapped back into the Test FIFO such that the Test FIFO becomes an infinite loop of data. When the ‘loop mode’ is engaged the FIFO continuously transmits the looped section until the user stops the Test FIFO by performing a VME access to the FFO (read or write). Bit 23 is brought out to the front panel as a scope trigger for diagnostic use.
- Bits 20 and 22 are brought out to test points (J76 and J77) for diagnostic use.
- Bit 25 being set will execute an immediate single word read from the FIFO and the word read will be kept on the bus for one full command cycle (7 clocks). If the FIFO is empty the word that is read will be the one being written (with bit 25 set) otherwise the word will be read from the FIFO contents. At the end of the operation the FIFO will be reset.
- Bits 31..26 and 24 are reserved and should be set to 0 during writes.

### 3.1.5 Fanout Diagnostic Control Register: relative address 0x0020

The Fanout Diagnostic Control Register provides access to various control features of the module, mostly used for diagnostics purposes. Bits are written to this register to cause state changes in the Fanout. A separate read-only register, the Fanout Status Register, is provided for status checks.

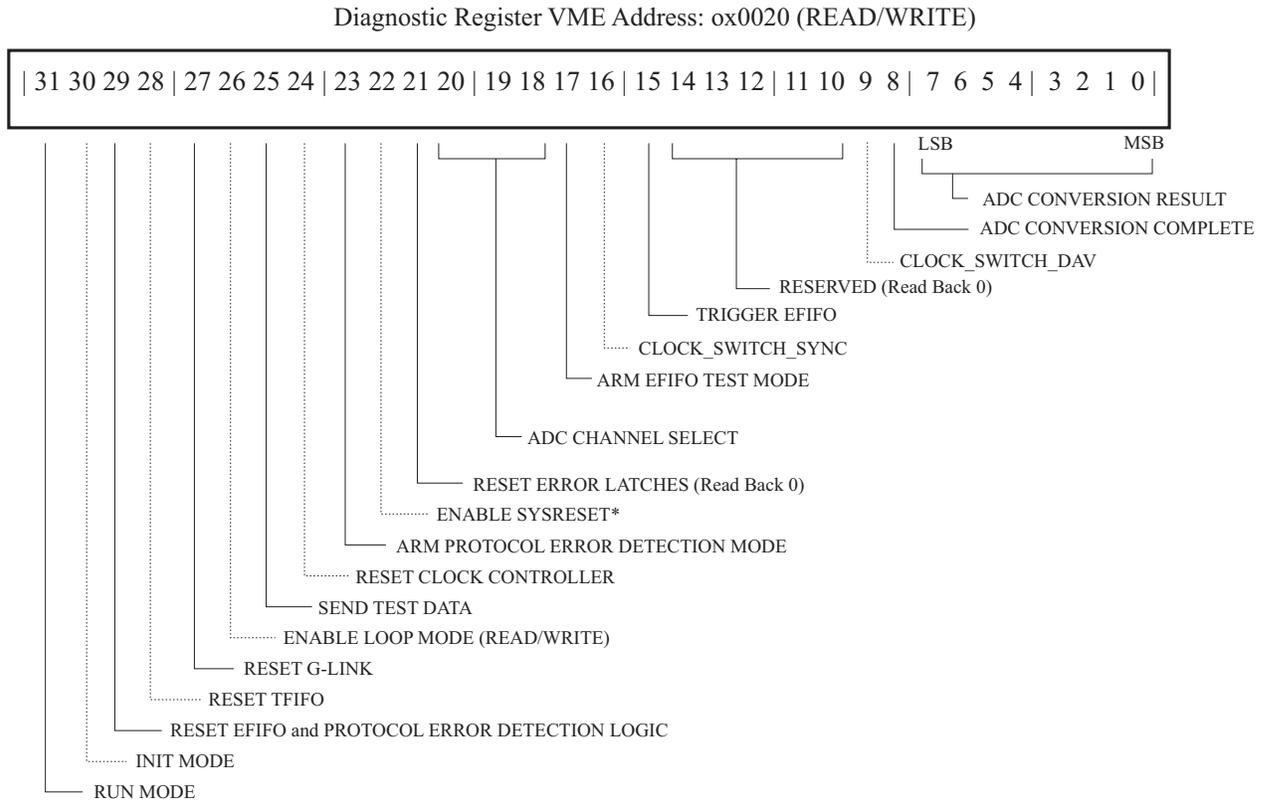


Figure 3.5, Fanout diagnostic control register.

Bit #	Name	Read/Write interpretation
31	RUN_MODE	Writing a 1 to this bit sets the Fanout to Run mode, this is similar to having received the CAV* sequence from the SRC. The difference is that when RUN MODE is requested by VME (writing a 1 to bit 31 of the Diagnostic Register when the Fanout was in INIT MODE), only a VME request can put the Fanout back into INIT MODE (writing a 1 to bit 30 of the Diagnostic Register). This bit reads back '1' if the Fanout is in the RUN mode (Slave State Machine in state 3), zero otherwise. When the bit is 1 the RUN MODE LED on the front panel is on. <b>Writing a 0 to this bit has no effect.</b>
30	INIT_MODE	When the module is in RUN mode, writing a 1 to this bit requests that the state machines leave RUN mode and return back to INIT mode. This is the 'clean' way to exit RUN mode, identical to a second CAV* sequence from the SRC. ). This bit reads back '1' if the Fanout is in the INIT mode, zero otherwise. When the bit is 1 the INIT MODE LED on the front panel is on. If both bit 31 and bit 30 are 0 the condition should be considered a MODE FAULT, the MODE FAULT LED on the front panel will be on. <b>Writing a 0 to this bit has no effect.</b>
29	RESET_EFIFO and PROTOCOL ERROR DETECTION LOGIC	Writing a 1 to this bit clears the Error FIFO and resets the Error FIFO State Machine and the protocol error detection logic. This bit will reset the effect of the two SRC commands (0x3A and 0x3B) used by the SRC to force high/low the four status cable signals. The bit always reads back zero.
28	RESET_TFIFO	Writing a 1 to this bit clears the Test FIFO and resets the Test FIFO State Machine. The bit always reads back zero.
27	RESET_G-Link	Writing a 1 to this bit resets the G-Link receiver. The bit always reads back zero.
26	ENABLE_LOOP_MODE	Writing a 1 to this bit enables the Test FIFO loop mode. In this mode, the Test FIFO reloads itself with data such that, when SEND_TEST_DATA is set, the Test FIFO sends its data pattern continuously. This bit reads back '1' if loop mode is enabled, '0' if it is not. This bit is reset to 0 if the Test FIFO is reset and at the end of each Test FIFO single read, send sequence or loop cycle.
25	SEND_TEST_DATA	Writing a 1 to this bit causes the Test FIFO data previously loaded from VME to be sent to the FIBs through the J3 TTL data bus at full system speed (53MHz clock). Once the TEST FIFO is emptied the Fanout will continue to send MCLK and SYNC pulses along with the last value written to the Test FIFO continuously asserted. When the bit is reset to 0 by a VME write to the Diagnostic Register, the FIFO cycle is terminated and the J3 TTL data bus is blanked (driven low). The bit reads back '1' after it is set until the end of the Test FIFO cycle (single read, send sequence or loop) when is reset to 0.
24	RESET CLOCK_CONTROLLER	Writing a 1 to this bit asynchronously resets the Clock Controller Logic placing the Fanout back to INIT state. This reset also includes the state machines for "RUN_MODE", "MASTER" and "SLAVE" and two bits of the Diagnostic Register (those showing [RCC]). Unlike using bit 30, the transition is not guaranteed to be clean; however, the actions of this bit are not dependent upon the presence of the G-Link clock like bit 30. The G-Link Receiver will not be reset. The bit reads back zero.
23	ARM ERROR FIFO PROTOCOL ERROR DETECTION MODE	Writing a 1 arm the protocol error detection logic and the error FIFO. When a protocol error occurs the error FIFO is triggered to store the data stream and the bit is reset. The bit reads back '1' if previously set, '0' otherwise and the default value is 0.
22	ENABLE_SYSRESET* [RCC]	Writing a 1 to this bit enables the module to drive the SYSRESET* signal (open collector) on the VME Backplane P1 connector. If enabled the SYSRESET* driver is controlled by the SRC through the command 0x38 issued on the G-Link data stream. The SRC command 0x38 drives (independent of the status of the ENABLE_SYSRESET* bit) the /RESET signal on the front panel lemo connector. The ENABLE_SYSRESET* bit reads back '1' if the SYSRESET* driver is enabled, otherwise '0'.
21	RESET ERROR LATCHES	Reset error latches in the error detection logic. The bit reads back 0.

20..18	A/D CHANNEL SELECT	<p>These three bits select one of eight channels in the multi-channel A/D converter. They read back the last channel selected.</p> <ul style="list-style-type: none"> <li>• Channel 0: G-Link optical power</li> <li>• Channel 1: FFO upper component side temperature sensor</li> <li>• Channel 2: FFO lower component side temperature sensor</li> <li>• Channel 3: Vw (nominal -5.2V) power supply</li> <li>• Channel 4: Test point J73</li> <li>• Channel 5: Test point J74</li> <li>• Channel 6: on-board -2.0V power supply</li> <li>• Channel 7: Test point J75.</li> </ul>
17	ARM EFIFO TEST MODE	<p>Writing a 1 arm the the error FIFO in test mode, this causes the Error FIFO to store data when the Test FIFO is used. After the error FIFO is triggered to store the data stream the bit is reset. The bit reads back '1' if previously set, '0' otherwise and the default value is 0.</p>
16	CLOCK SWITCH SYNC [RCC]	<p>Sets the FFO to use the local SYNC instead of the G-Link SYNC during clock switching (Local Clock to G-Link Clock). Default value is 0.</p> <p>0: Use locally generated SYNC. 1: Use SYNC received by G-Link</p>
15	TRIGGER ERROR FIFO	<p>Writing a 1 trigger the error FIFO to store data. The Error FIFO will store 7185 words of pre-trigger and 1000 words of post-trigger data. If the Error FIFO test mode is armed the error FIFO will store 8185 words of post-trigger data and then stop. The bit reads back '0'.</p>
14..10	RESERVED	<p>Reserved for future use. All bits read back zero and have no effect during a write operation. (Note: bits 8 to 14 are masked by the GDX ISP).</p>
9	CLOCK SWITCH DAV [RCC]	<p>Sets the FFO to ignore the G-Link DAV signal during clock switching (Local Clock to G-Link Clock). Default value is 0.</p> <p>0: Use G-Link DAV. 1: Ignore G-Link DAV</p>
8	CONVERSION_COMPLETE	<p>This READ_ONLY bit goes low when an A/D conversion begins and goes back high when valid data is available on bits 7..0. A new conversion is started automatically each time the diagnostic register is written to, the result will be available during the next read access. This bit has no effect during a write operation.</p>
7..0	CONVERSION_RESULT	<p>The eight-bit result of an A/D conversion. The bits are not in hexadecimal format, bit #7 is the LSB, bit #0 is the MSB. These bits have no effect during a write operation.</p>

Table 3.6, Fanout diagnostic control register bit assignment.

**3.1.5.1 Interpreting ADC Data**

It's important to notice that the ADC data read through the Diagnostic Register is not in hexadecimal format, the bits are in reverse order, bit 7 is the least significant bit (LSB) and bit 0 is the most significant bit (MSB). In order to convert the data to hex format the bits should be swapped. Table 3.7 provides a fast way to convert read data to the actual voltage values at the input of the ADC.

Hex Value Read	Volts												
00	0.00	25	3.22	4A	1.61	6F	4.82	94	0.80	B9	3.08	DE	2.41
01	2.51	26	1.96	4B	4.12	70	0.27	95	3.31	BA	1.82	DF	4.92
02	1.25	27	4.47	4C	0.98	71	2.78	96	2.06	BB	4.33	E0	0.14
03	3.76	28	0.39	4D	3.49	72	1.53	97	4.57	BC	1.20	E1	2.65
04	0.63	29	2.90	4E	2.24	73	4.04	98	0.49	BD	3.71	E2	1.39
05	3.14	2A	1.65	4F	4.75	74	0.90	99	3.00	BE	2.45	E3	3.90
06	1.88	2B	4.16	50	0.20	75	3.41	9A	1.75	BF	4.96	E4	0.76
07	4.39	2C	1.02	51	2.71	76	2.16	9B	4.25	C0	0.06	E5	3.27
08	0.31	2D	3.53	52	1.45	77	4.67	9C	1.12	C1	2.57	E6	2.02
09	2.82	2E	2.27	53	3.96	78	0.59	9D	3.63	C2	1.31	E7	4.53
0A	1.57	2F	4.78	54	0.82	79	3.10	9E	2.37	C3	3.82	E8	0.45
0B	4.08	30	0.24	55	3.33	7A	1.84	9F	4.88	C4	0.69	E9	2.96
0C	0.94	31	2.75	56	2.08	7B	4.35	A0	0.10	C5	3.20	EA	1.71
0D	3.45	32	1.49	57	4.59	7C	1.22	A1	2.61	C6	1.94	EB	4.22
0E	2.20	33	4.00	58	0.51	7D	3.73	A2	1.35	C7	4.45	EC	1.08
0F	4.71	34	0.86	59	3.02	7E	2.47	A3	3.86	C8	0.37	ED	3.59
10	0.16	35	3.37	5A	1.76	7F	4.98	A4	0.73	C9	2.88	EE	2.33
11	2.67	36	2.12	5B	4.27	80	0.02	A5	3.24	CA	1.63	EF	4.84
12	1.41	37	4.63	5C	1.14	81	2.53	A6	1.98	CB	4.14	F0	0.29
13	3.92	38	0.55	5D	3.65	82	1.27	A7	4.49	CC	1.00	F1	2.80
14	0.78	39	3.06	5E	2.39	83	3.78	A8	0.41	CD	3.51	F2	1.55
15	3.29	3A	1.80	5F	4.90	84	0.65	A9	2.92	CE	2.25	F3	4.06
16	2.04	3B	4.31	60	0.12	85	3.16	AA	1.67	CF	4.76	F4	0.92
17	4.55	3C	1.18	61	2.63	86	1.90	AB	4.18	D0	0.22	F5	3.43
18	0.47	3D	3.69	62	1.37	87	4.41	AC	1.04	D1	2.73	F6	2.18
19	2.98	3E	2.43	63	3.88	88	0.33	AD	3.55	D2	1.47	F7	4.69
1A	1.73	3F	4.94	64	0.75	89	2.84	AE	2.29	D3	3.98	F8	0.61
1B	4.24	40	0.04	65	3.25	8A	1.59	AF	4.80	D4	0.84	F9	3.12
1C	1.10	41	2.55	66	2.00	8B	4.10	B0	0.25	D5	3.35	FA	1.86
1D	3.61	42	1.29	67	4.51	8C	0.96	B1	2.76	D6	2.10	FB	4.37
1E	2.35	43	3.80	68	0.43	8D	3.47	B2	1.51	D7	4.61	FC	1.24
1F	4.86	44	0.67	69	2.94	8E	2.22	B3	4.02	D8	0.53	FD	3.75
20	0.08	45	3.18	6A	1.69	8F	4.73	B4	0.88	D9	3.04	FE	2.49
21	2.59	46	1.92	6B	4.20	90	0.18	B5	3.39	DA	1.78	FF	5.00
22	1.33	47	4.43	6C	1.06	91	2.69	B6	2.14	DB	4.29		
23	3.84	48	0.35	6D	3.57	92	1.43	B7	4.65	DC	1.16		
24	0.71	49	2.86	6E	2.31	93	3.94	B8	0.57	DD	3.67		

Table 3.7, ADC read data to voltage conversion table.

**3.1.5.2 Optical Power reading (ADC channel #0)**

ADC channel #0 is connected to the G-Link receiver. The output voltages of the G-Link receiver is multiplied by 2 by an operational amplifier.

The following graph and formulas allow conversions between the voltage values read by ADC and the optical power received by the G-Link receiver.

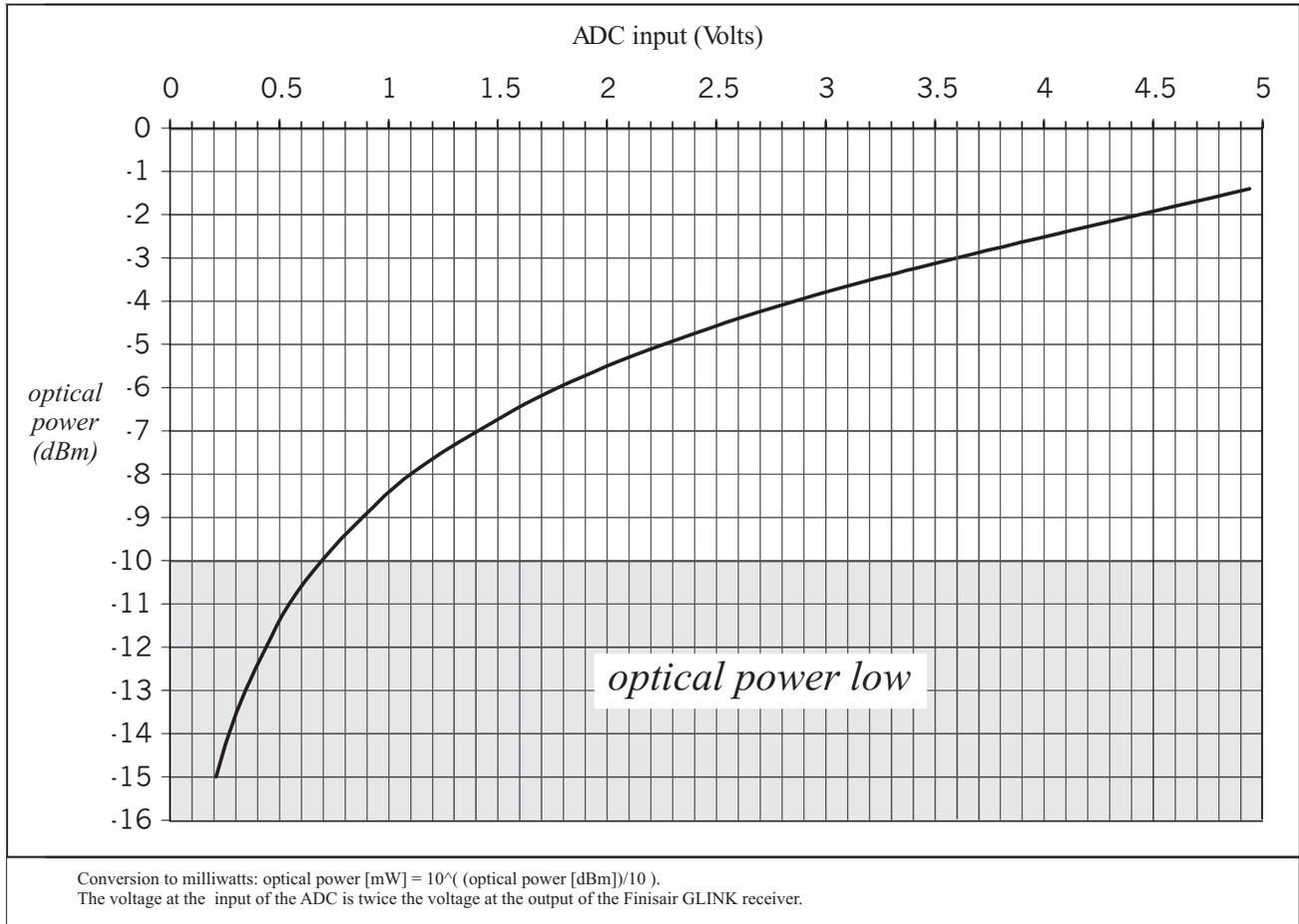


Figure 3.6, Optical power versus ADC voltage readout.

Approximate formulas:

Optical power [mW]  $\cong$  0.144\*V<sub>ADC-ch0</sub> [Volts];

Optical power [dBm]  $\cong$  10\*Log<sub>10</sub> (0.144\*V<sub>ADC-ch0</sub> [Volts] );

### 3.1.5.3 Temperature reading

ADC channels #1 and #2 are connected to the two temperature sensors installed on the Fanout (top and bottom of the module on the component side).

The output voltages of the LM35C temperature sensors are multiplied by 5 by an operational amplifier.

The following formulas allow conversions between the voltage values read by ADC and the temperature in Degrees Centigrade and Fahrenheit.

$$\text{Temp [C}^\circ\text{]} = 20 * V_{\text{ADC}} [\text{Volts}];$$

The reading is valid for:  $0.10 \text{ Volts} \leq V_{\text{ADC}} [\text{Volts}] \leq 5.00 \text{ Volts}$ .

The measurable temperature range is then  $2 \text{ C}^\circ \leq \text{Temp} [\text{C}^\circ] \leq 100 \text{ C}^\circ$ .

Temperatures below  $2 \text{ C}^\circ$  will be read as  $2 \text{ C}^\circ$  and temperatures above  $100 \text{ C}^\circ$  will be read as  $100 \text{ C}^\circ$ .

$$\text{Temp [F}^\circ\text{]} = 32 + 36 * V_{\text{ADC}} [\text{Volts}];$$

The reading is valid for:  $0.10 \text{ Volts} \leq V_{\text{ADC}} [\text{Volts}] \leq 5.00 \text{ Volts}$ .

The measurable temperature range is then  $35.6 \text{ F}^\circ \leq \text{Temp [F}^\circ] \leq 212 \text{ F}^\circ$ .

Temperatures below  $35.6 \text{ F}^\circ$  will be read as  $35.6 \text{ F}^\circ$  and temperatures above  $212 \text{ F}^\circ$  will be read as  $212 \text{ F}^\circ$ .

The relation between degrees Centigrade and Fahrenheit is:

$$\text{Temp [F}^\circ\text{]} = 32 + 1.8 * \text{Temp [C}^\circ\text{]}$$

or

$$\text{Temp [C}^\circ\text{]} = (9/5) * (\text{Temp [F}^\circ\text{]} - 32)$$

### 3.1.5.4 ECL Power Supply Voltage reading

ADC channels #3 and #6 allow monitoring of the  $V_{\text{EE}}$  (-5.2 Volt) and the  $V_{\text{TT}}$  (-2.0 Volt) voltages.

The voltage read from the ADC should be multiplied for a correction factor in order to obtain  $V_{\text{EE}}$  and  $V_{\text{TT}}$

$$V_{\text{EE}} = -(100/47) * V_{\text{ADC-ch3}} [\text{Volts}]$$

$$V_{\text{TT}} = -V_{\text{ADC-ch6}} [\text{Volts}]$$

**3.1.6 Fanout Status Register: relative address 0x0024**

This READ-ONLY register provides access to numerous status bits within the Fanout to aid in diagnostics and module-level tests. Writes to this register have no effect.

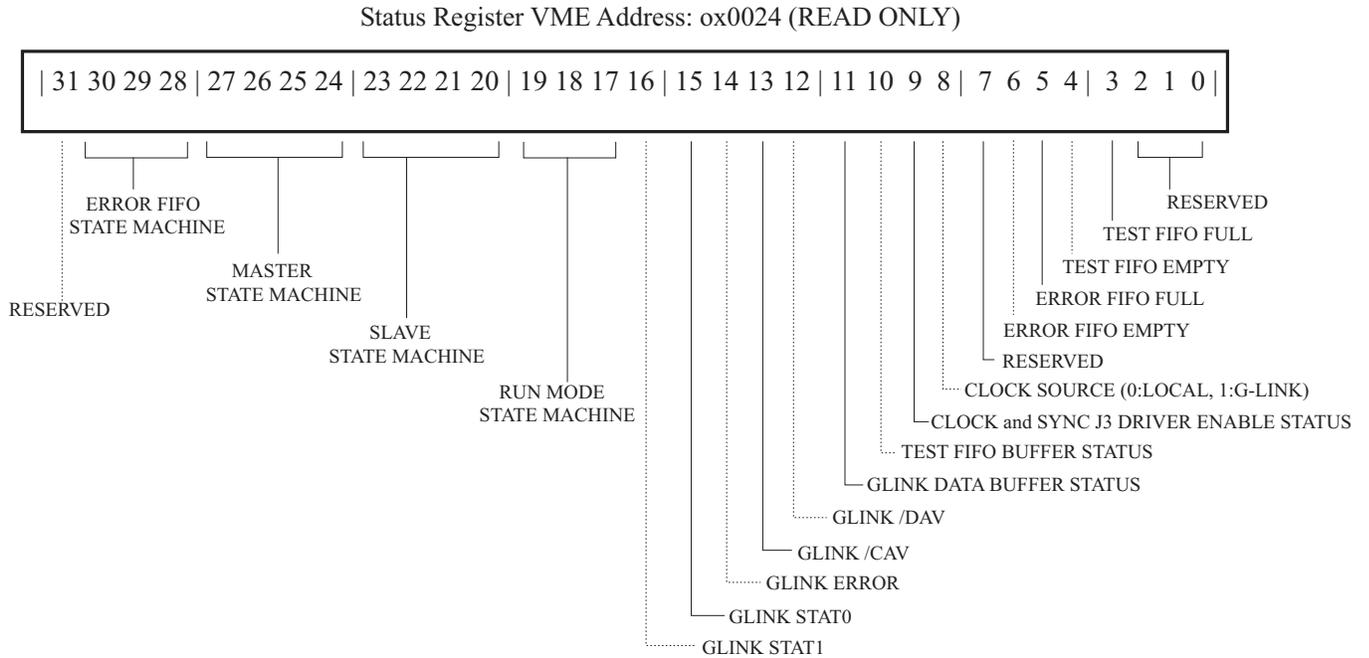


Figure 3.7, Fanout status register.

31	RESERVED	Reserved for future use. Bit reads back zero. This bit has no effect upon write.
30..28	Error FIFO Machine State	<p>These bits indicate the state of the Error FIFO state machine.</p> <p>The correct interpretation of this bit field is:</p> <ul style="list-style-type: none"> <li>• 0x1: Prestore in progress.</li> <li>• 0x2: Idle, waiting for trigger (from VME or from protocol error detection logic if armed).</li> <li>• 0x3: Post-store after trigger (1000 words)</li> <li>• 0x4: Data stream fully stored (8185 words), servicing VME reads.</li> <li>• 0x5: Test mode, waiting for trigger (from VME or from Test FIFO).</li> <li>• 0x6: Test mode post store after trigger.</li> <li>• 0x7: Test mode data stream fully stored (8185 words), servicing VME reads.</li> <li>• All other states are transient and not visible from VME.</li> </ul>
27..24	Master Machine State	<p>These bits indicate the state of the Master state machine.</p> <p>The correct interpretation of this bit field is:</p> <ul style="list-style-type: none"> <li>• 0x0: Fanout in Initialize mode, waiting for RUN request.</li> <li>• 0x1: G-Link locked, RUN request received, waiting for a SYNC rising edge.</li> <li>• 0x2: G-Link locked, RUN request received, waiting for a SYNC falling edge.</li> <li>• 0xB: G-Link locked, Slave machine in control.</li> <li>• 0xC: G-Link locked, RUN request received, waiting for a SYNC rising edge.</li> <li>• 0xD: G-Link locked, RUN request received, waiting for a SYNC falling edge.</li> </ul> <p>All other states are transient and not visible from VME.</p>
23..20	Slave Machine State	<p>These bits indicate the state of the Slave state machine.</p> <p>The correct interpretation of this bit field is:</p> <ul style="list-style-type: none"> <li>• 0x0: Fanout in Initialize mode.</li> <li>• 0x1: RUN received, waiting for DAV* and a rising edge of SYNC from G-Link.</li> <li>• 0x2: RUN received, waiting for DAV* and a falling edge of SYNC from G-Link.</li> <li>• 0x3: RUN Mode, MCLK, SYNC, TTL data and commands transmitted by the SRC (via G-Link).</li> <li>• 0x8,9,A,B,C,D,E,F: Internal Fanout error.</li> </ul> <p>All other states are transient and not visible from VME.</p>

19..17	Run Mode Machine State	<p>These bits indicate the state of the RUNMODE state machine.</p> <p>The correct interpretation of this bit field is:</p> <ul style="list-style-type: none"> <li>• 0x0: Fanout in Initialize state.</li> <li>• 0x1: In Run mode, having been placed in Run mode by SRC.</li> <li>• 0x4: In Run mode, having been placed in Run mode by a VME write.</li> <li>• 0x7: Fatal internal Fanout error.</li> </ul> <p>All other states are transient and not visible from VME.</p>
16	G-Link STAT1	Actual state of G-Link STAT1 signal.
15	G-Link STAT0	Actual state of G-Link STAT0 signal.
14	G-Link ERROR	Actual state of G-Link ERROR signal.
13	G-Link CAV	Actual state of G-Link CAV* signal (active low).
12	G-Link DAV	Actual state of G-Link DAV* signal (active low).
11	G-Link Data buffer status	<p>Status of the G-Link Data buffer enable. When enabled the buffers drive both the J3 Backplane and the local bus (GLD[19..0]) which is used by the ERROR FIFO.</p> <p>0: Disabled. 1: Enabled.</p>
10	Test FIFO buffer status	<p>Status of the Test FIFO Output Enable and the Test Data Driver Enable (they use the same enable signal). When enabled the data sent by the TEST FIFO is driving the J3 Backplane TTL Bus. The TEST FIFO is also used to blank the J3 Backplane TTL Bus when the FFO is in INIT Mode.</p> <p>0: Disabled. 1: Enabled.</p>
9	J3 Driver Enable status	<p>MCLK &amp; SYNC J3 Backplane ECL drivers (to FIBs) status.</p> <p>0: Disabled. 1: Enabled.</p>
8	Clock Source	<p>MCLK &amp; SYNC sent to J3 Backplane ECL Drivers (to FIBs).</p> <p>0: Locally generated; 1: Via G-Link (SRC).</p>
7	RESERVED	Reserved for future use. Bit read back zero. This bit has no effect upon write.
6	Error FIFO Empty Flag	1: EF Empty; 0: EF not empty.
5	Error FIFO Full Flag	1: EF Full; 0: EF not full.
4	Test FIFO Empty Flag	1: TF Empty; 0: TF not empty.
3	Test FIFO Full Flag	1: TF Full; 0: TF not full.
2..0	RESERVED	Reserved for future use. Bit reads back zero. This bit has no effect upon write.

Table 3.8, Fanout status register bit assignment.

### 3.1.7 Error FIFO: relative address 0x0028

Relative address 0x28 provides access to the Error FIFO, which provides a record of words preceding and following any protocol error. The FIFO can only be read. It cannot be directly written from VME. To test the Error FIFO, a test data sequence can be sent on the J3 Backplane TTL data bus using the Test FIFO. Figure 3.8 shows the format of data read from the Error FIFO.

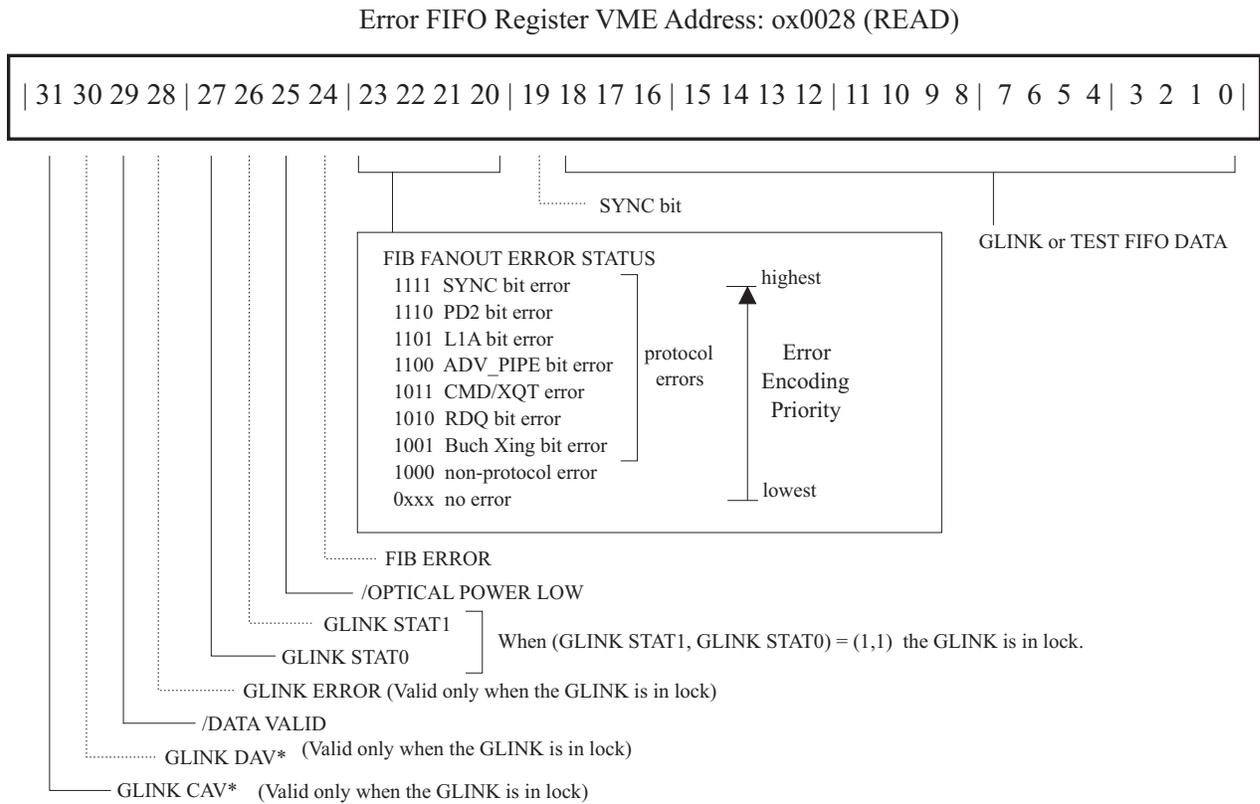


Figure 3.8, Error FIFO register data format.

**3.1.8 Fanout Status Bit Mapping Registers: relative address 0x0008, 0x000C, 0x0010, 0x0014.**

Relative address 0x0008 contains the first of four status bit mapping registers in the Fanout. Each register provides 29 bits of selection, where each bit corresponds to a status or error condition that the Fanout monitors. If the bit is set in the register, the state of that error or status condition is OR-ed with all other selected conditions to create the status bit.

The Fanout handles different error conditions in different ways. Some error conditions (showing “(r)” in Table 3.9) are latched by the Fanout and remain asserted until explicitly cleared by the SRC sending the “Reset Error Latches” command (see Table 2.2) or by VME through the Fanout diagnostic register (bit 21).

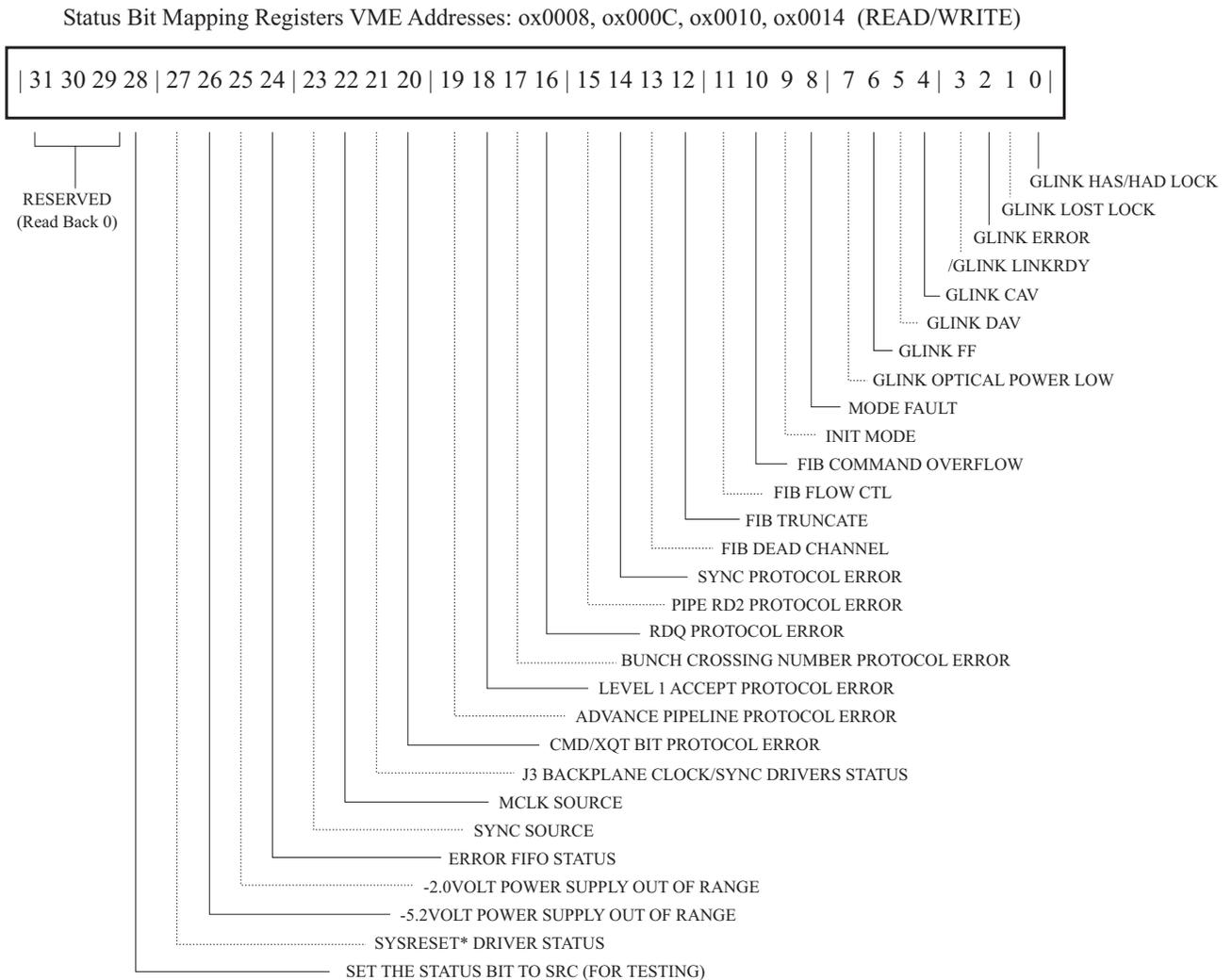


Figure 3.9, Fanout status bit mapping registers.

Bit Position	Status/error condition included if set
31..29	Unused bits – read back zero.
28	Force to 1 SRC Status Bit to test the FFO to SRC status cable connection. 1: set the SRC status bit 0: return to normal operation
27	SYSRESET* driver status bit - sets SRC Status Bit if SYSRESET* is asserted (low) by Fanout.
26 (Γ)	-5.2V error bit; sets SRC Status bit if -5.2V Power Supply voltage is more negative than -5.46V or more positive than -4.94V. It is <u>NOT</u> the latched version of the signal driving the -5.2V POWER LED on front panel.
25 (Γ)	-2.0V error bit; sets SRC Status bit if -2.0V Power Supply voltage is more negative than -2.2V or more positive than -1.8V. It is <u>NOT</u> the latched version of the signal driving the -2.0V POWER LED on front panel.
24	Error FIFO status bit; sets SRC Status bit if Error FIFO has a stored error.
23	SYNC Source status bit; set if SYNC is driven by local oscillator, clear if SYNC is driven by G-Link.
22	MCLK Source status bit; set if MCLK is driven by local oscillator, clear if MCLK driven by G-Link.
21	J3 Backplane Clock/SYNC Driver status bit; set if drivers are OFF (disabled, output low), cleared if drivers are ON (enabled).
20 (Γ)	CMD/XQT bit protocol error; sets SRC Status bit if error detected in bits 5..0 of 20-bit G-Link data-word
19 (Γ)	Advance Pipeline protocol error; sets SRC Status bit if error detected in ADVP bit of 20-bit G-Link data-word
18 (Γ)	Level 1 Accept protocol error; sets SRC Status bit if error detected in L1A bit of 20-bit G-Link data-word
17 (Γ)	Bunch Crossing Number protocol error; sets SRC Status bit if error detected in BXING section of G-Link 20-bit data-word
16 (Γ)	RDQ protocol error; sets SRC Status bit if error detected in RDQ section of 20-bit G-Link data-word
15 (Γ)	PIPE_RD2 protocol error; sets SRC Status bit if error detected in PIPE_RD2 bit of 20-bit G-Link data-word
14 (Γ)	SYNC protocol error; sets SRC Status bit if error detected in SYNC bit of 20-bit G-Link data-word
13 (Γ)	FIB DEAD CHANNEL status bit; sets SRC Status bit if any FIB asserts this error.
12 (Γ)	FIB TRUNCATE status bit; sets SRC Status bit if any FIB asserts this error.
11 (Γ)	FIB FLOW CTL status bit; sets SRC Status bit if any FIB asserts this error.
10 (Γ)	FIB Command Overflow status bit; sets SRC Status bit if any FIB asserts this error.
09	Fanout State Machine Idle status bit; sets SRC Status bit if Fanout state machines are in IDLE state. Equivalent to the INIT light on the front panel.
08	Fanout State Machine Not Locked status bit; sets SRC Status bit if Fanout state machines are not in IDLE state, but also not in LOCKED state. Equivalent to the MODE FAULT light on the front panel.
07 (Γ)	Optical Power Below Threshold error bit; sets SRC Status bit if optical power received by G-Link below threshold.
06	G-Link FF (FillFrame) status bit; sets SRC Status bit if G-Link is receiving Fill Frames
05	G-Link DAV* status bit; sets SRC Status bit if G-Link DAV* is asserted (low).
04	G-Link CAV* status bit; sets SRC Status bit if G-Link CAV* is asserted (low).
03	G-Link LINKRDY* status bit; sets SRC Status bit if LINKRDY* is NOT asserted
02 (Γ)	G-Link ERROR status bit; sets SRC Status bit if ERROR bit is asserted
01 (Γ)	G-Link LOST LOCK status bit; sets SRC Status bit if G-Link had lock and lost it.
00 (Γ)	G-Link HAS/HAD LOCK status bit; sets SRC Status bit if G-Link has been locked since last reset.

Table 3.9, Fanout status bit mapping registers bit assignment.

Inversions as necessary are performed within the Fanout such that all conditions are active HIGH. Reading the Status bit as HIGH indicates that at least one of the selected conditions is present as defined within Table 3.9. The bias network within the SRC will drive all four Status bits HIGH if the cable falls off or the +5.0V supply in the FIB subrack fails. Reading one of these registers will return the values set by the last write to the register.

The SRC can issue commands to the Fanout over the optical link (see Table 2.2), these are ignored (i.e. considered as no-operation commands) by the FIB. Three of the Fanout commands are used to allow the SRC to turn ON or OFF all the status lines or to allow them to report error/status conditions as programmed in the Fanout bit status registers. This allows the SRC to validate the optical and status links to the FIB Fanout.

Fanout Status Bit 1, 2, and 3 mapping registers (relative addresses 0x000C, 0x0010, 0x0014) are identical to the Fanout status bit 0 mapping register, save that they control SRC Status Bits 1, 2 and 3 as opposed to SRC status bit 0.



	<b>Bit Position</b>	<b>Error condition</b>
	31..28	Unused bits – read back zero.
Fanout status	27	SYSRESET* driver status bit – is set to 1 if SYSRESET* is asserted (low) by the FIB Fanout.
	26 (T)	-5.2V error bit; is set to 1 if -5.2V Power Supply voltage is more negative than -5.46V or more positive than -4.94V. It is NOT equivalent to the -5.2V POWER LED on the front panel.
	25 (T)	-2.0V error bit; is set to 1 if -2.0V Power Supply voltage is more negative than -2.2V or more positive than -1.8V. It is NOT equivalent to the -2V POWER LED on the front panel.
	24	Error FIFO status bit; is set to 1 if the Error FIFO has stored an error.
	23	SYNC Source status bit; is set to 1 if SYNC is driven by the local oscillator, clear if SYNC is driven by the G-Link.
	22	MCLK Source status bit; is set to 1 if MCLK is driven by the local oscillator, clear if MCLK is driven by the G-Link
	21	J3 Backplane Clock/SYNC drivers status bit; is set to 1 if drivers are OFF (disabled, output low), cleared if drivers are ON (enabled). The drivers are for both the G-Link clock/SYNC and the local clock/SYNC.
Protocol errors	20 (T)	CMD/XQT bit protocol error; is set to 1 if an error is detected in bits 5..0 of the 20-bit G-Link data-word.
	19 (T)	Advance Pipeline protocol error; is set to 1 if an error is detected in ADVP bit of the 20-bit G-Link data-word.
	18 (T)	Level 1 Accept protocol error; is set to 1 if an error is detected in L1A bit of the 20-bit G-Link data-word.
	17 (T)	Bunch Crossing Number protocol error; is set to 1 if an error is detected in BXING section of the 20-bit G-Link data-word.
	16 (T)	RDQ protocol error; is set to 1 if an error is detected in RDQ section of the 20-bit G-Link data-word.
	15 (T)	PIPE_RD2 protocol error; is set to 1 if an error is detected in PIPE_RD2 bit of the 20-bit G-Link data-word.
	14 (T)	SYNC protocol error; is set to 1 if an error is detected in SYNC bit of the 20-bit G-Link data-word.
FIB errors	13 (T)	FIB DEAD CHANNEL status bit; is set to 1 if any FIB asserts this error.
	12 (T)	FIB TRUNCATE status bit; is set to 1 if any FIB asserts this error.
	11 (T)	FIB FLOW CTL status bit; is set to 1 if any FIB asserts this error.
	10 (T)	FIB Command Overflow status bit; is set to 1 if any FIB asserts this error.
Fanout status	09	Fanout State Machine Idle status bit; is set to 1 if the Fanout state machines are in the IDLE state. It is equivalent to the INIT LED on the front panel.
	08	Fanout State Machine Not Locked status bit; is set to 1 if the Fanout state machines are not in the IDLE state and also not in the LOCKED state. It is equivalent to the MODE FAULT LED on the front panel.
G-Link errors/status	07 (T)	Optical Power Below Threshold error bit; is set to 1 if optical power received by the G-Link is below the set threshold of -10dBm.
	06	G-Link FF (Fill-Frame) status bit; is set to 1 if the G-Link is receiving Fill Frames.
	05	G-Link DAV* status bit; is set to 1 if G-Link DAV* is asserted (low).
	04	G-Link CAV* status bit; is set to 1 if G-Link CAV* is asserted (low).
	03	G-Link LINKRDY* status bit; is set to 1 if LINKRDY* is NOT asserted.
	02 (T)	G-Link ERROR status bit; is set to 1 if the G-Link ERROR bit is asserted.
	01 (T)	G-Link LOST LOCK status bit; is set to 1 if the G-Link had lock and lost it.
	00 (T)	G-Link HAS/HAD LOCK status bit; is set to 1 if G-Link has been locked since last reset.

Table 3.10, Fanout error status register bit assignment.

### 3.1.10 Non Volatile RAM

A 2KbyteX8 Non Volatile RAM exists in each Fanout.

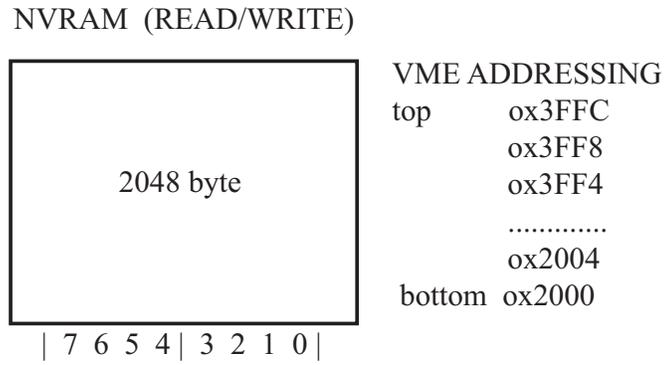


Figure 3.11, NVRAM address map.

### 3.2 Front Panel Description

The Fanout has one ST fiber optic connector (Finisar G-Link receiver) to receive clock/commands/data from the SRC and one 8-pin shielded data link connector (RS-485 protocol) to return the status bits to the SRC.

A single LEMO connector provides a TTL open collector, 250msec long reset pulse generated by the Fanout when the SRC issues the command ox38 on the G-Link data stream. This allows for cable interface to reset the local subrack CPU module. The same pulse is used to drive the VME SYSRESET\* signal when the driver is enabled through the Fanout diagnostic register (bit 22).

A 25-pin type 'D' connector allows front panel access to the internal In System Programmable logic programming chain. An additional LEMO connector is driven by a Test FIFO output (bit 23).

The Fanout has fifteen front panel LEDs to indicate several error/status conditions as specified in Table 3.11.

Label	Type	Info
SEL	Yellow LED	Indicate when the module is accessed as a VMEbus slave.
POWER +5V	Green LED	ON if +5.0V Power Supply voltage is present. <u>No control on the voltage range is performed.</u>
POWER -5.2V	Green LED	ON if -5.2V Power Supply voltage is present. <u>No control on the voltage range is performed.</u> Out of range information are provided by the -5.2V error bit in the Error Status Register.
POWER -2.0V	Green LED	ON if -2.0V Power Supply voltage is present. <u>No control on the voltage range is performed.</u> Out of range information are provided by the -2.0V error bit in the Error Status Register.
POWER J3B	Green LED	ON if +5.0V Power Supply is providing power (can be used for terminations) to the J3 Backplane. <u>No control on the voltage range is performed.</u>
MODE INIT	Green LED	ON if the Fanout is in INITIALIZE MODE.
MODE RUN	Green LED	ON if the Fanout is in RUN MODE
MODE FAULT	Red LED	ON if the Fanout is not in INITIALIZE or RUN modes. This LED will flash briefly when the Fanout switches modes.
CLK SRC	Green LED	ON if the G-Link Receiver is the source of the clock driving the FIBs (through the J3 Backplane).
CLK LOCAL	Yellow LED	ON if the Fanout Local Clock is the source of the clock driving the FIBs (through the J3 Backplane).
G-Link LOCK	Green LED	ON if the G-Link Receiver is locked (G-Link Status signals STAT1 and STAT0 are both high).
G-Link ERR	Red LED	ON if the G-Link Receiver is asserting the G-Link ERROR (frame error detected) status signal.
G-Link OPT PWR LOW	Red LED	ON if the optical power received by the G-Link receiver is below threshold. The threshold is set to -10dBm.
FIFOS TEST	Yellow LED	ON if the Test FIFO is driving the J3 Backplane TTL Data bus.
FIFOS ERROR	Red LED	ON when any G-Link/Test FIFO data protocol errors occurs.
RESET	Button	RESET the Fanout module. Equivalent to a power-on reset.
RESET OUT	LEMO connector	Provides a TTL open collector, 250msec long, reset pulse generated by the Fanout when the SRC issues the command 0x38 on the G-Link data stream. This allows for a cable interface to reset the local subrack CPU module. The same pulse is used to drive the VME SYSRESET* signal when the driver is enabled through the Fanout diagnostic register (bit 22).
SCOPE TRIG OUT	LEMO connector	Connected to bit 23 of the TEST FIFO output. Can be used as a scope trigger for field diagnostics.
RS-485 STATUS	8-pin shielded data link connector	Used to return the Status bits to the Silicon Readout Controller.
ISP LOADER	25-pin type 'D' connector	Provides access to the Fanout for programming the In-System Programmable Logic (Lattice Isp).
FIBER INPUT	ST connector	G-Link Receiver input (ST fiber optic connector).

Table 3.11, Front panel description.

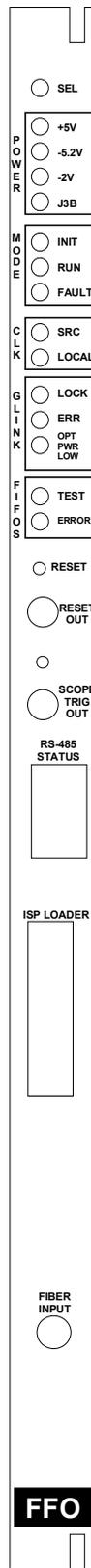


Figure 3.12, FIB Fanout front panel

### 3.3 J3 Backplane Connector, Slot Assignment, Drivers-Receivers-Termination Scheme

The J3 Backplane is used by the FFO to distribute the clocks and commands received from the SRC to the FIB modules. The J3 Backplane has 21 slots. Slots 1 to 4 have holes and positions for 3 row DIN connectors that make no electrical connection to the Backplane. Slots 5 and 6 are assigned to the SRC module. The positions of slots 7 and 21 are used for the TTL bus terminations. Slots 8 to 13 and 15 to 20 are assigned to FIB Modules and slot 14 is assigned to the FIB Fanout Module.

Slot #	Connector and pinout
1, 2, 3, 4	DIN Connectors
5, 6	Hard metric, SRC compatible pinout
7	No connector, TTL BUS terminations
8, 9, 10, 11, 12, 13	Hard metric, FIB pinout
14	Hard metric, FIB Fanout pinout
15, 16, 17, 18, 19, 20	Hard metric, FIB pinout
21	No connector, TTL BUS terminations

Table 3.12, FIB J3 Backplane slot assignment

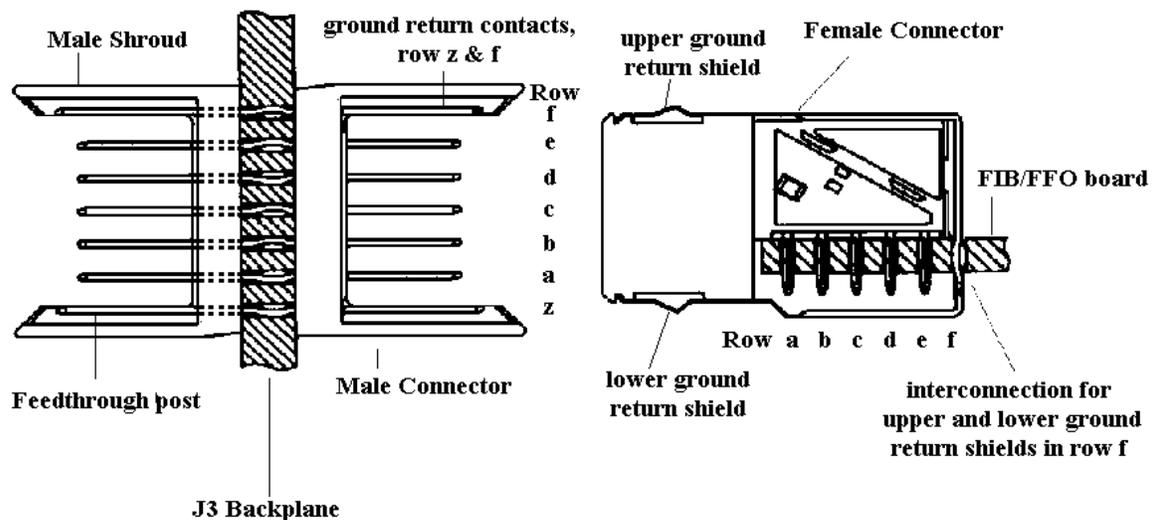


Figure 3.13, FIB J3 Backplane/modules connector

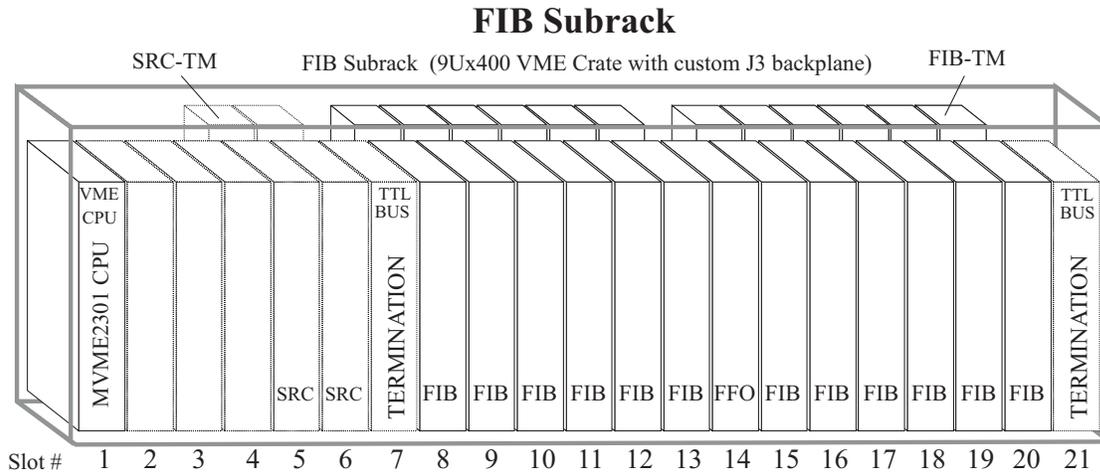


Figure 3.14, FIB subrack.

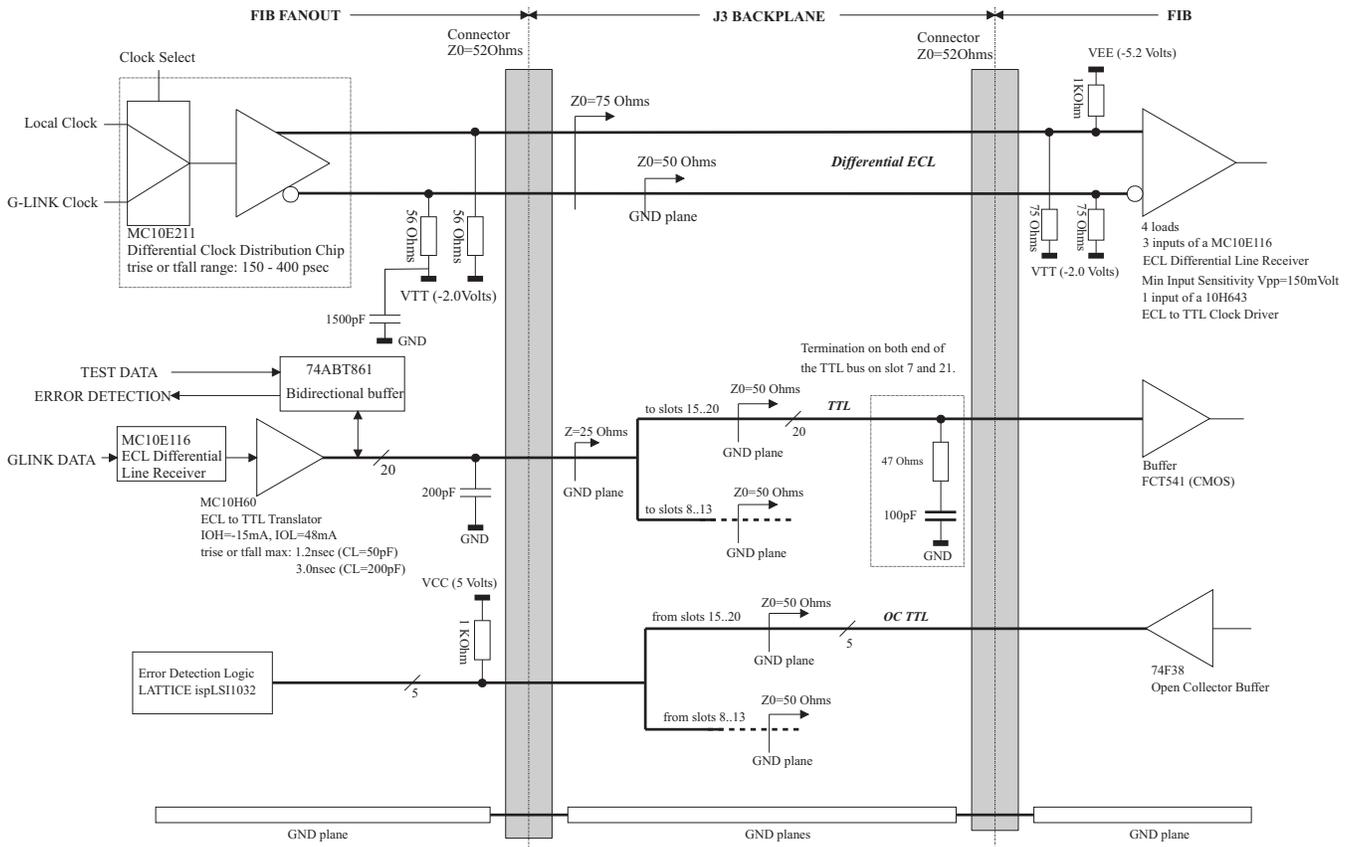


Figure 3.15, Drivers, Receivers and Terminations

**3.4 J3 Connector Pin Assignment for the FFO and for the FFO J3 Backplane slot.**

The pinout for the J3 connector on the FFO module and for slot 14 of the Backplane is shown on the following pages. The Fanout makes an electrical connection to pins in row “z” only if the bottom shield of the connector is installed. BUS [1..25] is the TTL data bus.

Bit #	J3 Pin	Signal Name	Signal Type	Direction FFO-FIB
25	C25	FIB_COMMAND_OVERFLOW*	Open Collector (♣)	⇐
24	C24	FIB_FLOW_CTL*	Open Collector (♣)	⇐
23	C23	FIB_TRUNCATE*	Open Collector (♣)	⇐
22	C22	FIB_DEAD_CHANNEL*	Open Collector (♣)	⇐
21	C21	RESERVED	- (♣)	-
20	C20	SYNC	TTL	⇒
19	C19	Pipe_RD2	TTL	⇒
18..17	C18, C17	RDQ (Read-Digitize-Quiescent)	TTL	⇒
16..9	C16 - C9	Bunch Crossing Number	TTL	⇒
8	C8	Level 1 Accept	TTL	⇒
7	C7	Advance_Pipeline	TTL	⇒
6	C6	FIB XQT signal	TTL	⇒
5..1	C5 – C1	FIB Command	TTL	⇒

Table 3.13, TTL Bus mapping for the J3 Backplane.

MCLK[8..13], MCLK[15..20], /MCLK[8..13], /MCLK[15..20] are the point to point differential ECL signals that distribute the Master Clock to the FIB modules. MCLK[n] and /MCLK[n] will provide the Master Clock signal to slot # n of the Vipa Subrack.

SYNC[8..13], SYNC[15..20], /SYNC[8..13], /SYNC[15..20] are the point o point differential ECL signals that distribute the SYNC signal to the FIB modules. SYNC[n] and /SYNC[n] will provide the SYNC signal to slot # n of the Vipa Subrack.

(♣) Bits 21 to 25 are pulled-up on the Fib Fanout module with a 1 KΩ resistor to VCC (+5.0 Volts).

Pin #	Row 'z'	Row 'a'	Row 'b'	Row 'c'	Row 'd'	Row 'e'	Row 'f'
1	GND (●)	(⊗)	MCLK8	BUS 1 (TTL OUT)	SYNC8	(⊗)	GND
2	GND (●)	(⊗)	/MCLK8	BUS 2 (TTL OUT)	/SYNC8	(⊗)	GND
3	GND (●)	(⊗)	MCLK9	BUS 3 (TTL OUT)	SYNC9	(⊗)	GND
4	GND (●)	(⊗)	/MCLK9	BUS 4 (TTL OUT)	/SYNC9	(⊗)	GND
5	GND (●)	(⊗)	MCLK10	BUS 5 (TTL OUT)	SYNC 10	(⊗)	GND
6	GND (●)	(⊗)	/MCLK10	BUS 6 (TTL OUT)	/SYNC10	(⊗)	GND
7	GND (●)	(⊗)	MCLK11	BUS 7 (TTL OUT)	SYNC11	(⊗)	GND
8	GND (●)	(⊗)	/MCLK11	BUS 8 (TTL OUT)	/SYNC11	(⊗)	GND
9	GND (●)	(⊗)	MCLK12	BUS 9 (TTL OUT)	SYNC12	(⊗)	GND
10	GND (●)	(⊗)	/MCLK12	BUS 10 (TTL OUT)	/SYNC12	(⊗)	GND
11	GND (●)	(⊗)	MCLK13	BUS 11 (TTL OUT)	SYNC13	(⊗)	GND
12	GND (●)	(⊗)	/MCLK13	BUS 12 (TTL OUT)	/SYNC13	(⊗)	GND
13	GND (●)	(⊗)	MCLK20	BUS 13 (TTL OUT)	SYNC20	(⊗)	GND
14	GND (●)	(⊗)	/MCLK20	BUS 14 (TTL OUT)	/SYNC20	(⊗)	GND
15	GND (●)	(⊗)	MCLK19	BUS 15 (TTL OUT)	SYNC19	(⊗)	GND
16	GND (●)	(⊗)	/MCLK19	BUS 16 (TTL OUT)	/SYNC19	(⊗)	GND
17	GND (●)	(⊗)	MCLK18	BUS 17 (TTL OUT)	SYNC18	(⊗)	GND
18	GND (●)	(⊗)	/MCLK18	BUS 18 (TTL OUT)	/SYNC18	(⊗)	GND
19	GND (●)	(⊗)	MCLK17	BUS 19 (TTL OUT)	SYNC17	(⊗)	GND
20	GND (●)	(⊗)	/MCLK17	BUS 20 (TTL OUT)	/SYNC17	(⊗)	GND
21	GND (●)	(⊗)	MCLK16	BUS 21 (OC IN)	SYNC16	(⊗)	GND
22	GND (●)	(⊗)	/MCLK16	BUS 22 (OC IN)	/SYNC16	(⊗)	GND
23	GND (●)	(⊗)	MCLK15	BUS 23 (OC IN)	SYNC15	(⊗)	GND
24	GND (●)	(⊗)	/MCLK15	BUS 24 (OC IN)	/SYNC15	(⊗)	GND
25	GND (●)	(⊗)	(⊗)	BUS 25 (OC IN)	(⊗)	GND	GND
26	GND (●)	(⊗)	(⊗)	GND	GND	(⊗)	GND
27	GND (●)	(⊗)	(⊗)	GND	(⊗)	(⊗)	GND
28	GND (●)	(⊗)	(⊗)	GND	(⊗)	GND	GND
29	GND (●)	(⊗)	(⊗)	GND	GND	(⊗)	GND
30	GND (●)	(⊗)	(⊗)	GND	(⊗)	(⊗)	GND
31	GND (●)	(⊗)	(⊗)	GND	(⊗)	GND	GND
32	GND (●)	(⊗)	(⊗)	+5.0 V	GND	(⊗)	GND
33	GND (●)	(⊗)	(⊗)	(⊗)	(⊗)	(⊗)	GND
34	GND (●)	(⊗)	(⊗)	N.C.	(⊗)	GND	GND
35	GND (●)	(⊗)	(⊗)	(⊗)	(⊗)	(⊗)	GND
36	GND (●)	(⊗)	(⊗)	N.C.	GND	(⊗)	GND
37	GND (●)	(⊗)	(⊗)	(⊗)	(⊗)	(⊗)	GND
38	GND (●)	(⊗)	(⊗)	N.C.	(⊗)	GND	GND
39	GND (●)	(⊗)	(⊗)	(⊗)	(⊗)	(⊗)	GND
40	GND (●)	(⊗)	(⊗)	N.C.	GND	(⊗)	GND
41	GND (●)	(⊗)	(⊗)	(⊗)	(⊗)	(⊗)	GND
42	GND (●)	(⊗)	(⊗)	N.C.	(⊗)	GND	GND
43	GND (●)	(⊗)	(⊗)	(⊗)	(⊗)	(⊗)	GND
44	GND (●)	(⊗)	(⊗)	N.C.	GND	(⊗)	GND
45	GND (●)	(⊗)	(⊗)	(⊗)	(⊗)	(⊗)	GND
46	GND (●)	(⊗)	(⊗)	N.C.	(⊗)	GND	GND
47	GND (●)	(⊗)	(⊗)	(⊗)	(⊗)	(⊗)	GND

(●) The Fanout makes connection to pins in row "z" only if the bottom shield of the connector is installed.  
(⊗) The pin is connected to ground on the Fanout module with a hardware modification (wiring)

Table 3.14, J3 Connector pin assignments for the FIB Fanout Module.

Pin #	Row 'z'	Row 'a'	Row 'b'	Row 'c'	Row 'd'	Row 'e'	Row 'f'
1	GND	GND	MCLK8	BUS 1	SYNC8	GND	GND
2	GND	N.C.	/MCLK8	BUS 2	/SYNC8	GND	GND
3	GND	GND	MCLK9	BUS 3	SYNC9	GND	GND
4	GND	N.C.	/MCLK9	BUS 4	/SYNC9	GND	GND
5	GND	GND	MCLK10	BUS 5	SYNC 10	GND	GND
6	GND	N.C.	/MCLK10	BUS 6	/SYNC10	GND	GND
7	GND	GND	MCLK11	BUS 7	SYNC11	GND	GND
8	GND	N.C.	/MCLK11	BUS 8	/SYNC11	GND	GND
9	GND	GND	MCLK12	BUS 9	SYNC12	GND	GND
10	GND	N.C.	/MCLK12	BUS 10	/SYNC12	GND	GND
11	GND	GND	MCLK13	BUS 11	SYNC13	GND	GND
12	GND	N.C.	/MCLK13	BUS 12	/SYNC13	GND	GND
13	GND	GND	MCLK20	BUS 13	SYNC20	GND	GND
14	GND	N.C.	/MCLK20	BUS 14	/SYNC20	GND	GND
15	GND	GND	MCLK19	BUS 15	SYNC19	GND	GND
16	GND	N.C.	/MCLK19	BUS 16	/SYNC19	GND	GND
17	GND	GND	MCLK18	BUS 17	SYNC18	GND	GND
18	GND	N.C.	/MCLK18	BUS 18	/SYNC18	GND	GND
19	GND	GND	MCLK17	BUS 19	SYNC17	GND	GND
20	GND	N.C.	/MCLK17	BUS 20	/SYNC17	GND	GND
21	GND	GND	MCLK16	BUS 21	SYNC16	GND	GND
22	GND	N.C.	/MCLK16	BUS 22	/SYNC16	GND	GND
23	GND	GND	MCLK15	BUS 23	SYNC15	GND	GND
24	GND	N.C.	/MCLK15	BUS 24	/SYNC15	GND	GND
25	GND	GND	GND	BUS 25	GND	GND	GND
26	GND	N.C.	GND	GND	GND	GND	GND
27	GND						
28	GND	N.C.	GND	GND	GND	GND	GND
29	GND						
30	GND	N.C.	GND	GND	GND	GND	GND
31	GND						
32	GND	N.C.	GND	+5.0 V	GND	GND	GND
33	GND						
34	GND	N.C.	GND	N.C.	GND	GND	GND
35	GND						
36	GND	N.C.	GND	N.C.	GND	GND	GND
37	GND						
38	GND	N.C.	GND	N.C.	GND	GND	GND
39	GND						
40	GND	N.C.	GND	N.C.	GND	GND	GND
41	GND						
42	GND	N.C.	GND	N.C.	GND	GND	GND
43	GND						
44	GND	N.C.	GND	N.C.	GND	GND	GND
45	GND						
46	GND	N.C.	GND	N.C.	GND	GND	GND
47	GND						

Table 3.15, J3 Connector pin assignments for slot 14 of the J3 Backplane.

### **3.5 Connector Pin Assignments for the FIB and for the FIB slots of the Backplane.**

The pinout for the J3 connectors for the FIB module and for the J3 Backplane (for FIB slots) are shown on the following pages. The FIB makes an electrical connection to pins in row “z” only if the bottom shield of the connector is installed.

MCLK[n], /MCLK[n] are the point to point differential ECL lines driven by the Fib Fanout to distribute the Master Clock signal to the FIB module in slot # n of the Vipa Subrack.

SYNC[n], / SYNC [n] are the point to point differential ECL lines driven by the Fib Fanout to distribute the SYNC signal to the FIB module in slot # n of the Vipa Subrack.

Pin #	Row 'z'	Row 'a'	Row 'b'	Row 'c'	Row 'd'	Row 'e'	Row 'f'
1	GND (●)	GND	GND	BUS 1 (TTL IN)	GND	GND	GND
2	GND (●)	B_MCLK	HDI-A-D0	BUS 2 (TTL IN)	(⊗)	HDI-B-D0	GND
3	GND (●)	GND	HDI-A-D1	BUS 3 (TTL IN)	GND	HDI-B-D1	GND
4	GND (●)	B_AD_PIPE	HDI-A-D2	BUS 4 (TTL IN)	(⊗)	HDI-B-D2	GND
5	GND (●)	GND	HDI-A-D3	BUS 5 (TTL IN)	GND	HDI-B-D3	GND
6	GND (●)	B_SYNC	HDI-A-D4	BUS 6 (TTL IN)	(⊗)	HDI-B-D4	GND
7	GND (●)	GND	HDI-A-D5	BUS 7 (TTL IN)	GND	HDI-B-D5	GND
8	GND (●)	FTM_CLK	HDI-A-D6	BUS 8 (TTL IN)	(⊗)	HDI-B-D6	GND
9	GND (●)	GND	HDI-A-D7	BUS 9 (TTL IN)	GND	HDI-B-D7	GND
10	GND (●)	N.C.	HDI-A-OBDRV	BUS 10 (TTL IN)	(⊗)	HDI-B-OBDRV	GND
11	GND (●)	GND	HDI-C-D0	BUS 11 (TTL IN)	GND	HDI-D-D0	GND
12	GND (●)	N.C.	HDI-C-D1	BUS 12 (TTL IN)	(⊗)	HDI-D-D1	GND
13	GND (●)	GND	HDI-C-D2	BUS 13 (TTL IN)	GND	HDI-D-D2	GND
14	GND (●)	N.C.	HDI-C-D3	BUS 14 (TTL IN)	(⊗)	HDI-D-D3	GND
15	GND (●)	GND	HDI-C-D4	BUS 15 (TTL IN)	GND	HDI-D-D4	GND
16	GND (●)	N.C.	HDI-C-D5	BUS 16 (TTL IN)	(⊗)	HDI-D-D5	GND
17	GND (●)	GND	HDI-C-D6	BUS 17 (TTL IN)	GND	HDI-D-D6	GND
18	GND (●)	C0	HDI-C-D7	BUS 18 (TTL IN)	(⊗)	HDI-D-D7	GND
19	GND (●)	GND	HDI-C-DVAL	BUS 19 (TTL IN)	GND	HDI-D-DVAL	GND
20	GND (●)	C1	HDI-E-D0	BUS 20 (TTL IN)	(⊗)	HDI-F-D0	GND
21	GND (●)	GND	HDI-E-D1	BUS 21 (TTL IN)	GND	HDI-F-D1	GND
22	GND (●)	C2	HDI-E-D2	BUS 22 (OC OUT)	(⊗)	HDI-F-D2	GND
23	GND (●)	GND	HDI-E-D3	BUS 23 (OC OUT)	GND	HDI-F-D3	GND
24	GND (●)	C3	HDI-E-D4	BUS 24 (OC OUT)	(⊗)	HDI-F-D4	GND
25	GND (●)	GND	HDI-E-D5	BUS 25 (OC OUT)	GND	HDI-F-D5	GND
26	GND (●)	C4	HDI-E-D6	(⊗)	(⊗)	HDI-F-D6	GND
27	GND (●)	GND	HDI-E-D7	SYNC(n)	GND	HDI-F-D7	GND
28	GND (●)	C5	HDI-E-DVAL	/SYNC(n)	(⊗)	HDI-F-DVAL	GND
29	GND (●)	GND	HDI-G-D0	(⊗)	GND	HDI-H-D0	GND
30	GND (●)	C_DATA	HDI-G-D1	MCLK(n)	(⊗)	HDI-H-D1	GND
31	GND (●)	GND	HDI-G-D2	/MCLK(n)	GND	HDI-H-D2	GND
32	GND (●)	C_CLK1	HDI-G-D3	N.C.	(⊗)	HDI-H-D3	GND
33	GND (●)	GND	HDI-G-D4	GND	GND	HDI-H-D4	GND
34	GND (●)	C_CLK2	HDI-G-D5	BNRB-A	(⊗)	HDI-H-D5	GND
35	GND (●)	GND	HDI-G-D6	BNRB-B	GND	HDI-H-D6	GND
36	GND (●)	PIPE_RD2	HDI-G-D7	BNRB-C	(⊗)	HDI-H-D7	GND
37	GND (●)	GND	HDI-G-DVAL	BNRB-D	GND	HDI-H-DVAL	GND
38	GND (●)	/L1A	HDI-I-D0	BNRB-E	(⊗)	HDI-J-D0	GND
39	GND (●)	GND	HDI-I-D1	BNRB-F	GND	HDI-J-D1	GND
40	GND (●)	FE_CLK1	HDI-I-D2	BNRB-G	(⊗)	HDI-J-D2	GND
41	GND (●)	GND	HDI-I-D3	BNRB-H	GND	HDI-J-D3	GND
42	GND (●)	FE_CLK2	HDI-I-D4	BNRB-I	(⊗)	HDI-J-D4	GND
43	GND (●)	GND	HDI-I-D5	BNRB-J	GND	HDI-J-D5	GND
44	GND (●)	BE_CLK1	HDI-I-D6	GND	(⊗)	HDI-J-D6	GND
45	GND (●)	GND	HDI-I-D7	(⊗)	GND	HDI-J-D7	GND
46	GND (●)	BE_CLK2	HDI-I-DVAL	(⊗)	(⊗)	HDI-J-DVAL	GND
47	GND (●)	GND	GND	(⊗)	GND	GND	GND

(●) The FIB makes connection to pins in row "z" only if the bottom shield of the connector is installed.  
 (⊗) The pin could be connected to ground on the FIB module with a hardware modification (wiring)

Table 3.16, J3 Connector pin assignments for the Fiber Interface Module (FIB).

Pin #	Row 'z'	Row 'a'	Row 'b'	Row 'c'	Row 'd'	Row 'e'	Row 'f'
1	GND	GND	GND	BUS 1	GND	GND	GND
2	GND	N.C.	N.C.	BUS 2	GND	N.C.	GND
3	GND	GND	N.C.	BUS 3	GND	N.C.	GND
4	GND	N.C.	N.C.	BUS 4	GND	N.C.	GND
5	GND	GND	N.C.	BUS 5	GND	N.C.	GND
6	GND	N.C.	N.C.	BUS 6	GND	N.C.	GND
7	GND	GND	N.C.	BUS 7	GND	N.C.	GND
8	GND	N.C.	N.C.	BUS 8	GND	N.C.	GND
9	GND	GND	N.C.	BUS 9	GND	N.C.	GND
10	GND	N.C.	N.C.	BUS 10	GND	N.C.	GND
11	GND	GND	N.C.	BUS 11	GND	N.C.	GND
12	GND	N.C.	N.C.	BUS 12	GND	N.C.	GND
13	GND	GND	N.C.	BUS 13	GND	N.C.	GND
14	GND	N.C.	N.C.	BUS 14	GND	N.C.	GND
15	GND	GND	N.C.	BUS 15	GND	N.C.	GND
16	GND	N.C.	N.C.	BUS 16	GND	N.C.	GND
17	GND	GND	N.C.	BUS 17	GND	N.C.	GND
18	GND	N.C.	N.C.	BUS 18	GND	N.C.	GND
19	GND	GND	N.C.	BUS 19	GND	N.C.	GND
20	GND	N.C.	N.C.	BUS 20	GND	N.C.	GND
21	GND	GND	N.C.	BUS 21	GND	N.C.	GND
22	GND	N.C.	N.C.	BUS 22	GND	N.C.	GND
23	GND	GND	N.C.	BUS 23	GND	N.C.	GND
24	GND	N.C.	N.C.	BUS 24	GND	N.C.	GND
25	GND	GND	N.C.	BUS 25	GND	N.C.	GND
26	GND	N.C.	N.C.	GND	GND	N.C.	GND
27	GND	GND	N.C.	SYNC(n)	GND	N.C.	GND
28	GND	N.C.	N.C.	/SYNC(n)	GND	N.C.	GND
29	GND	GND	N.C.	GND	GND	N.C.	GND
30	GND	N.C.	N.C.	MCLK(n)	GND	N.C.	GND
31	GND	GND	N.C.	/MCLK(n)	GND	N.C.	GND
32	GND	N.C.	N.C.	N.C.	GND	N.C.	GND
33	GND	GND	N.C.	GND	GND	N.C.	GND
34	GND	N.C.	N.C.	N.C.	GND	N.C.	GND
35	GND	GND	N.C.	N.C.	GND	N.C.	GND
36	GND	N.C.	N.C.	N.C.	GND	N.C.	GND
37	GND	GND	N.C.	N.C.	GND	N.C.	GND
38	GND	N.C.	N.C.	N.C.	GND	N.C.	GND
39	GND	GND	N.C.	N.C.	GND	N.C.	GND
40	GND	N.C.	N.C.	N.C.	GND	N.C.	GND
41	GND	GND	N.C.	N.C.	GND	N.C.	GND
42	GND	N.C.	N.C.	N.C.	GND	N.C.	GND
43	GND	GND	N.C.	N.C.	GND	N.C.	GND
44	GND	N.C.	N.C.	GND	GND	N.C.	GND
45	GND	GND	N.C.	GND	GND	N.C.	GND
46	GND	N.C.	N.C.	GND	GND	N.C.	GND
47	GND	GND	GND	GND	GND	GND	GND

Table 3.17, J3 Connector pin assignments for FIB slots of the J3 Backplane.

**3.6 J3 Connector Pin Assignments on SRC and on SRC slots of the Backplane.**

Pin #	Row 'z'	Row 'a'	Row 'b'	Row 'c'	Row 'd'	Row 'e'	Row 'f'
1	GND (●)	GND (◆)	N.C.	N.C.	N.C.	N.C.	GND
2	GND (●)	N.C.	N.C.	N.C.	N.C.	GND (◆)	GND
3	GND (●)	GND (◆)	N.C.	N.C.	N.C.	GND (◆)	GND
4	GND (●)	N.C.	N.C.	N.C.	N.C.	GND (◆)	GND
5	GND (●)	GND (◆)	N.C.	N.C.	N.C.	N.C.	GND
6	GND (●)	N.C.	N.C.	N.C.	N.C.	GND (◆)	GND
7	GND (●)	GND (◆)	N.C.	N.C.	N.C.	GND (◆)	GND
8	GND (●)	GND (◆)	N.C.	N.C.	N.C.	GND (◆)	GND
9	GND (●)	GND (◆)	N.C.	N.C.	N.C.	N.C.	GND
10	GND (●)	GND (◆)	N.C.	N.C.	N.C.	GND (◆)	GND
11	GND (●)	GND (◆)	N.C.	N.C.	N.C.	GND (◆)	GND
12	GND (●)	GND (◆)	N.C.	N.C.	N.C.	GND (◆)	GND
13	GND (●)	GND (◆)	N.C.	N.C.	N.C.	N.C.	GND
14	GND (●)	RF_DEL_CLK	N.C.	N.C.	N.C.	GND (◆)	GND
15	GND (●)	GND (◆)	N.C.	N.C.	N.C.	GND (◆)	GND
16	GND (●)	GL_CLK	N.C.	N.C.	N.C.	GND (◆)	GND
17	GND (●)	GND (◆)	N.C.	N.C.	N.C.	GND (◆)	GND
18	GND (●)	N.C.	N.C.	N.C.	N.C.	GND (◆)	GND
19	GND (●)	/RESET	N.C.	N.C.	N.C.	GND (◆)	GND
20	GND (●)	N.C.	N.C.	N.C.	N.C.	GND (◆)	GND
21	GND (●)	FF	N.C.	N.C.	N.C.	GND (◆)	GND
22	GND (●)	N.C.	N.C.	N.C.	N.C.	GND (◆)	GND
23	GND (●)	GND (◆)	N.C.	N.C.	N.C.	GND (◆)	GND
24	GND (●)	N.C.	N.C.	N.C.	N.C.	GND (◆)	GND
25	GND (●)	GND (◆)	GND (◆)	N.C.	GND (◆)	GND (◆)	GND
26	GND (●)	N.C.	READY	GND (◆)	GND (◆)	/CS0	GND
27	GND (●)	S1	SCLK	GND (◆)	/CS2	/CS1	GND
28	GND (●)	N.C.	S0	GND (◆)	/CS3	GND (◆)	GND
29	GND (●)	GND (◆)	GND (◆)	GND (◆)	GND (◆)	/CAV	GND
30	GND (●)	N.C.	GND (◆)	GND (◆)	GND (◆)	GND (◆)	GND
31	GND (●)	GND (◆)	FIB_ERR0	GND (◆)	ED	GND (◆)	GND
32	GND (●)	N.C.	FIB_ERR1	GND (◆)	/DAV	LOCK	GND
33	GND (●)	GND (◆)	FIB_ERR2	GND (◆)	GND (◆)	GND (◆)	GND
34	GND (●)	N.C.	FIB_ERR3	GND (◆)	GND (◆)	GND (◆)	GND
35	GND (●)	GLD18	GND (◆)	GND (◆)	GND (◆)	GLD19	GND
36	GND (●)	N.C.	GLD16	GND (◆)	GLD17	GND (◆)	GND
37	GND (●)	GND (◆)	GND (◆)	GND (◆)	GND (◆)	GND (◆)	GND
38	GND (●)	N.C.	GLD14	GND (◆)	GLD15	GND (◆)	GND
39	GND (●)	GLD12	GND (◆)	GND (◆)	GND (◆)	GLD13	GND
40	GND (●)	N.C.	GLD10	GND (◆)	GLD11	GND (◆)	GND
41	GND (●)	GND (◆)	GND (◆)	GND (◆)	GND (◆)	GND (◆)	GND
42	GND (●)	N.C.	GLD8	GND (◆)	GLD9	GND (◆)	GND
43	GND (●)	GLD6	GND (◆)	GND (◆)	GND (◆)	GLD7	GND
44	GND (●)	N.C.	GLD4	GND (◆)	GLD5	GND (◆)	GND
45	GND (●)	GND (◆)	GND (◆)	GND (◆)	GND (◆)	GND (◆)	GND
46	GND (●)	N.C.	GLD2	GND (◆)	GLD3	GND (◆)	GND
47	GND (●)	GLD0	GND (◆)	GND (◆)	GND (◆)	GLD1	GND

(●) The SRC makes connection to pins in row “z” only if the bottom shield of the connector is installed.  
 (◆) The pin is connected to ground on the SRC-TM and the SRC modules.

Table 3.18, J3 Connector pin assignments for the Silicon Readout Controller (SRC).

Pin #	Row 'z'	Row 'a'	Row 'b'	Row 'c'	Row 'd'	Row 'e'	Row 'f'
1	GND	GND	N.C.	N.C.	N.C.	N.C.	GND
2	GND	N.C.	N.C.	N.C.	N.C.	GND	GND
3	GND	GND	N.C.	N.C.	N.C.	GND	GND
4	GND	N.C.	N.C.	N.C.	N.C.	GND	GND
5	GND	GND	N.C.	N.C.	N.C.	N.C.	GND
6	GND	N.C.	N.C.	N.C.	N.C.	GND	GND
7	GND	GND	N.C.	N.C.	N.C.	GND	GND
8	GND	N.C.	N.C.	N.C.	N.C.	GND	GND
9	GND	GND	N.C.	N.C.	N.C.	N.C.	GND
10	GND	N.C.	N.C.	N.C.	N.C.	GND	GND
11	GND	GND	N.C.	N.C.	N.C.	GND	GND
12	GND	N.C.	N.C.	N.C.	N.C.	GND	GND
13	GND	GND	N.C.	N.C.	N.C.	N.C.	GND
14	GND	N.C.	N.C.	N.C.	N.C.	GND	GND
15	GND	GND	N.C.	N.C.	N.C.	GND	GND
16	GND	N.C.	N.C.	N.C.	N.C.	GND	GND
17	GND	GND	N.C.	N.C.	N.C.	GND	GND
18	GND	N.C.	N.C.	N.C.	N.C.	GND	GND
19	GND	N.C.	N.C.	N.C.	N.C.	GND	GND
20	GND	N.C.	N.C.	N.C.	N.C.	GND	GND
21	GND	N.C.	N.C.	N.C.	N.C.	GND	GND
22	GND	N.C.	N.C.	N.C.	N.C.	GND	GND
23	GND	GND	N.C.	N.C.	N.C.	GND	GND
24	GND	N.C.	N.C.	N.C.	N.C.	GND	GND
25	GND	GND	GND	N.C.	GND	GND	GND
26	GND	N.C.	N.C.	GND	GND	N.C.	GND
27	GND	N.C.	N.C.	GND	N.C.	N.C.	GND
28	GND	N.C.	N.C.	GND	N.C.	GND	GND
29	GND	GND	GND	GND	GND	N.C.	GND
30	GND	N.C.	GND	GND	GND	GND	GND
31	GND	GND	N.C.	GND	N.C.	GND	GND
32	GND	N.C.	N.C.	N.C.	N.C.	N.C.	GND
33	GND	GND	N.C.	GND	GND	GND	GND
34	GND	N.C.	N.C.	GND	GND	GND	GND
35	GND	N.C.	GND	GND	GND	N.C.	GND
36	GND	N.C.	N.C.	GND	N.C.	GND	GND
37	GND						
38	GND	N.C.	N.C.	GND	N.C.	GND	GND
39	GND	N.C.	GND	GND	GND	N.C.	GND
40	GND	N.C.	N.C.	GND	N.C.	GND	GND
41	GND						
42	GND	N.C.	N.C.	GND	N.C.	GND	GND
43	GND	N.C.	GND	GND	GND	N.C.	GND
44	GND	N.C.	N.C.	GND	N.C.	GND	GND
45	GND						
46	GND	N.C.	N.C.	GND	N.C.	GND	GND
47	GND	N.C.	GND	GND	GND	N.C.	GND

Table 3.19, J3 Connector pin assignments for SRC slots of the Backplane.

### 3.7 G-Link Receiver Daughter Card Interface Connector

The G-Link RX card connector is implemented by a 60 conductor 50 mil pitch connector with the pinout shown in Table 3.20. Input and Output signals are defined referring to the FIB Fanout. The names of the signals correspond to those used in the FINISAR FRC-1101 Module documentation.

See document # ESE-SVX-951018 for detailed information on the G-Link daughter card used by the FIB Fanout.

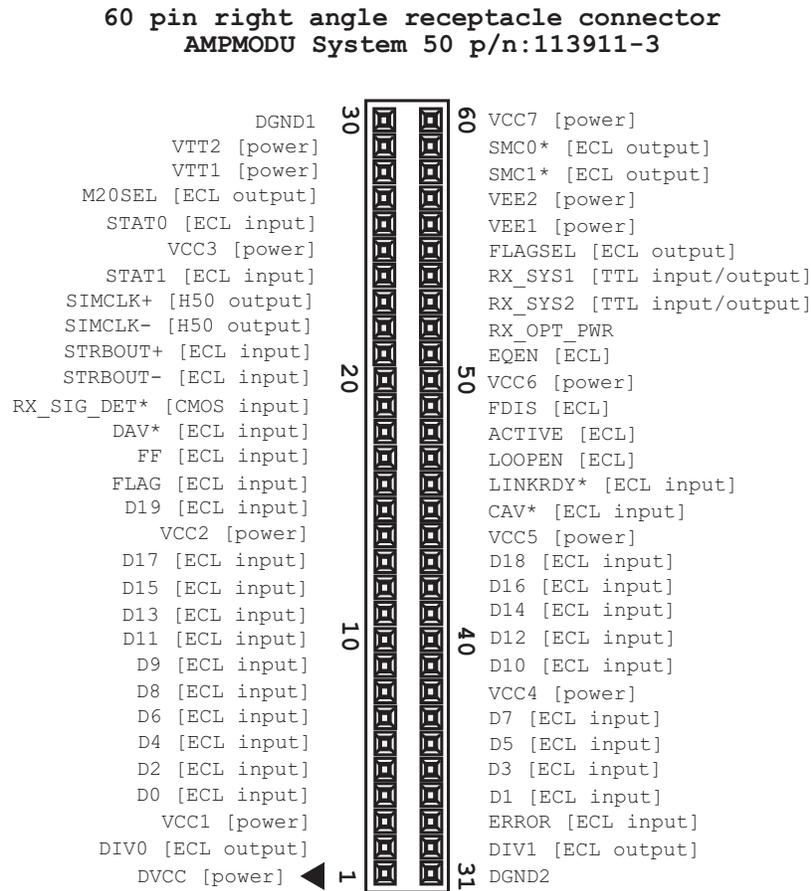


Figure 3.16, G-Link receiver daughter card interface connector.

Pin Number	Signal [type]	Information
1	DVCC [power]	Digital +5Volts for optics.
2	DIV0 [ECL output]	<b>VCO Divider Select</b> pin0. This pin together with pin DIV1 program the VCO divider chain to operate at full speed, half speed, quarter speed or one-eighth speed.
3	VCC1 [power]	ECL_VCC (Connected to Ground).
4	D0 [ECL input]	D0 to D19 are the G-Link receiver data outputs. 20-bits of data are received and decoded when M20SEL is Active, otherwise 16-bits of data are decoded and D16..D19 are undefined. All of these pins are designed to interface directly with the 100K ECL logic family.
5	D2 [ECL input]	Data input.
6	D4 [ECL input]	Data input.
7	D6 [ECL input]	Data input.
8	D8 [ECL input]	Data input.
9	D9 [ECL input]	Data input.
10	D11 [ECL input]	Data input.
11	D13 [ECL input]	Data input.
12	D15 [ECL input]	Data input.
13	D17 [ECL input]	Data input.
14	VCC2 [power]	ECL_VCC (Connected to Ground).
15	D19 [ECL input]	Data input.
16	FLAG [ECL input]	<b>Flag Bit:</b> If both Tx and Rx have FLAGSEL asserted, this input indicates the value of the transmitted flag bit, then this received bit can be treated <u>just like an extra data bit</u> . If both Tx and Rx have FLAGSEL set low, FLAG is used to differentiate the even frame from the odd frame in the line code.
17	FF [ECL input]	<b>Fill Frame Status:</b> During a given STRBOUT clock cycle, if neither DAV, CAV or ERROR are active, then the currently received frame is a fill frame. The type of fill frame received is indicated by FF pin. If FF is low, then FF0 has been received. If FF is High, then either FF1a or FF1b has been received.
18	DAV* [ECL input]	<b>Data Available Output:</b> This active-low signal indicates that the Rx chip (on the Finisar G-Link receiver module) data output D0..D19, have received data frames. Data should be latched on the rising edge of STRBOUT. Note that during link startup, false data indications may be given. The DAV* and LINKRDY outputs can be used together to avoid confusion during link startup.
19	RX_SIG_DET* [CMOS input]	CMOS output, active low, must be left open or be tied to pin 16 on the FTM-8510 transmitter. This line is used to drive a low current (<3mA) LED for link status indication on the Finisar FRC-1101-1 module. Refer to Finisar FRM-8510 Data Sheet and to Finisar AN-2010.
20	STRBOUT- [ECL input]	<b>Recovered Frame-rate Data Clock Output</b> (complementary input) The terminations should be compliant to the Hewlett Packard HDMP-1014 Receiver Data Sheet.
21	STRBOUT+ [ECL input]	<b>Recovered Frame-rate Data Clock Output:</b> this signal is the PLL recovered frame rate clock. D0..D19, FLAG, DAV, CAV, FF, LINKRDY, and ERROR should all be latched on the rising edge of STRBOUT.
22	SIMCLK- [H50 output]	Reference clock (inverting output). To the Rx module during simplex operation. See Hewlett Packard HDMP-1014 Receiver Data Sheet, Simplex Method III: Simplex with Reference Oscillator.
23	SIMCLK+ [H50 output]	Reference clock. To the Rx module during simplex operation. See Hewlett Packard HDMP-1014 Receiver Data Sheet, Simplex Method III: Simplex with Reference Oscillator.
24	STAT1 [ECL input]	<b>State Machine Status input.</b> This signal together with STAT0 indicates the current Rx Link Control state-machine state. See Hewlett Packard HDMP-1014 Receiver Data Sheet, Rx Control State Machine Operation Principle.

25	VCC3 [power]	ECL_VCC (Connected to Ground).
26	STAT0 [ECL input]	<b>State Machine Status input.</b> This signal together with STAT1 indicates the current Rx Link Control state-machine state. See Hewlett Packard HDMP-1014 Receiver Data Sheet, Rx Control State Machine Operation Principle.
27	M20SEL [ECL output]	<b>16 or 20 bit Word Select:</b> When this signal is high, the link operates in 20-bit data reception mode. Otherwise, the link operates in 16 bit mode and data signals D16..D19 are undefined. The termination must be done just before the Connector with a Resistor (matched to the transmission line) to VTT.
28	VTT1 [power]	ECL_VTT - 2Volts (typically -2Volts).
29	VTT2 [power]	ECL_VTT - 2Volts (typically -2Volts).
30	DGND1	Digital ground for optics.
31	DGND2	Digital ground for optics.
32	DIV1 [ECL output]	<b>VCO Divider Select</b> pin1. This pin together with pin DIV0 program the VCO divider chain to operate at full speed, half speed, quarter speed or one-eighth speed.
33	ERROR [ECL input]	<b>Received Data Error:</b> Asserted when a frame is received that does not correspond to either a valid Data, Control, or Fill frame encoding. When FLAGSEL is not active, the Hewlett Packard Rx chip also tests for strict alternation of flag bits during data frames. A flag bit alternation error will also cause an ERROR indication.
34	D1 [ECL input]	Data input.
35	D3 [ECL input]	Data input.
36	D5 [ECL input]	Data input.
37	D7 [ECL input]	Data input.
38	VCC4 [power]	ECL_VCC (Connected to Ground).
39	D10 [ECL input]	Data input.
40	D12 [ECL input]	Data input.
41	D14 [ECL input]	Data input.
42	D16 [ECL input]	Data input.
43	D18 [ECL input]	Data input.
44	VCC5 [power]	ECL_VCC (Connected to Ground).
45	CAV* [ECL input]	<b>Control Frame Available Output:</b> This Active-low signal indicates that the Hewlett Packard Rx chip data outputs are receiving Control Frames. False CAV indications may be generated during link startup.
46	LINKRDY* [ECL input]	<b>Link Ready Indicator.</b> This active-low signal is a re-timed version of ACTIVE signal. The LINKRDY* signal is normally driven by the HP chip's Rx State Machine output. LINKRDY* then indicates that the startup sequence is complete and that the data and control indications are valid.
47	LOOPEN [ECL]	<b>Loop back Control.</b> When asserted, this signal causes the loop back data inputs (LIN, LIN*) to be used instead of the normal data inputs (DIN, DIN*). The G-Link chip Rx state machine normally controls this input of the HP chip.
48	ACTIVE [ECL]	This signal is driven by the G-Link chip's Rx state machine output (PACTIVE pin). The ACTIVE signal is internally re-timed (in the HP chip) by STRBOUT and presented to the user as LINKRDY signal. This is how the G-Link chip Rx state machine signals the user that the startup sequence is complete.
49	FDIS [ECL]	<b>Frequency Detector Disable Input.</b> When active this input (HP chip) disables the Rx PLL Frequency detector and enable a phase detector. The frequency detector is used during the start-up sequence to acquire wide-band lock on Fill Frames, but must be disabled prior to sending data patterns. The G-Link Rx state machine normally controls this input.
50	VCC6 [power]	ECL_VCC (Connected to Ground)
51	EQEN [ECL]	<b>Enable Input for Cable Equalization.</b> When asserted this signal activates the cable equalization amplifier on the DIN, DIN* serial data inputs.
52	RX_OPT_PWR	Not for Host use.
53	RX_SYS2 [TTL input/output]	Internal signal.

54	RX_SYS1 [TTL input/output]	Internal signal.
55	FLAGSEL [ECL output]	<b>Flag bit mode select.</b> When this output is high, the extra FLAG bit input is effectively an extra transparent data bit. Otherwise, the FLAG bit is checked for alternation during data frames. Any break in strict alternation results in an ERROR indication to the user.
56	VEE1 [power]	ECL_VEE (typically -5.2V)
57	VEE2 [power]	ECL_VEE (typically -5.2V)
58	SMC1* [ECL output]	<b>State Machine Reset Input.</b> Each of the SMC1* and SMC2* (active low) signals reset the Rx state machine to the initial startup state. This initiates a complete PLL restart and handshake at both ends of the duplex link. Normally, SMC0* is connected to power-up reset circuit or a host system reset signal. The SMC1* pin is normally connected to the Tx LOCKED output. The LOCKED signal holds the state machine in the start-up state until the Tx PLL is locked. (same as SMCRST1* on HP chip data sheet).
59	SMC0* [ECL output]	<b>State Machine Reset Input.</b> Each of the SMC1* and SMC2* (active low) signals reset the Rx state machine to the initial startup state. This initiates a complete PLL restart and handshake at both ends of the duplex link. Normally, SMC0* is connected to power-up reset circuit or a host system reset signal. The SMC1* pin is normally connected to the Tx LOCKED output. The LOCKED signal holds the state machine in the start-up state until the Tx PLL is locked. (same as SMCRST1* on HP chip data sheet).
60	VCC7 [power]	ECL_VCC (Connected to Ground)

Table 3.20, G-Link Receiver Module FRC-1101-1 Connector pinout

### 3.8 Fanout to SRC Feedback Connector

This four-bit cable utilizes the AMP [Ref.33] Shielded Data Link Connector, 8 conductor, side entry panel and PCB ground, part number 3-520459-3. The eight wires in the cable carry four RS-485 signals [Ref.31, 32] as shown in Table 3.21:

Pin #	Signal
1	STATUS 0 (true side)
2	STATUS 0 (invert side)
3	STATUS 1 (true side)
4	STATUS 1 (invert side)
5	STATUS 2 (true side)
6	STATUS 2 (invert side)
7	STATUS 3 (true side)
8	STATUS 4 (invert side)

Table 3.21, Pinout of RS-485 status/error link to SRC

## **4. ELECTRICAL & MECHANICAL SPECIFICATIONS**

### **4.1 Packaging & Physical Size**

The FIB Fanout is a 9U x 400mm VME card in accordance with the VME 9U X 400 mm format standard.

### **4.2 PC Board Construction**

The printed circuit board is 0.093 +/-0.008 in thick. The PC board is eight layers: TTL Power, ECL Power, Ground (2) and Signal Layers (4).

### **4.3 Power Requirements**

The FIB Fanout requires 2.0 Amperes @ 5.0Volts and 2.5 Amperes @ -5.2Volts.

### **4.4 Cooling Requirements**

Fans mounted in the crate that the Vipa Subrack will reside in will provide cooling.

## **5. SAFETY FEATURES & QUALITY ASSURANCE PROCEDURES**

### **5.1 Module Fusing & Transient Suppression**

The FIB Fanout includes fusing, transient suppression and a LC filter network for the VCC (+5.0V) and VEE (-5.2V) incoming voltages [Ref.36]. The fuses, transient suppression diodes and the LC filter networks are placed close to the voltage entry point on the module. The fuses are sized such that the module is protected against a power short on the module.

### **5.2 Other Safety & Quality Assurance features**

Termination power supplied to the J3 Backplane by the Fanout is separately fused. Power for the J3 Backplane comes from pins that are not used to provide module power [Ref.36].

Two temperature monitors are available on-board which may be read over VME.

## 6. APPENDICES

### 6.1 Examples

#### 6.1.1 Use of the Test FIFO “Immediate Single-Word Read”

The “Immediate Single-Word Read” operation is used to write a single word to the Test FIFO and execute an immediate single word read, the word read will then be kept on the bus for one full command cycle (7 clocks) and the FIFO will then be reset. If the FIFO is empty the word that is read will be the one that is being written otherwise a few words will be read from the FIFO contents. Before using the TEST FIFO for an “Immediate Single-Word Read” operation it is necessary to perform a “Test FIFO Reset” through the Diagnostic Register. As stated above, at the end of the “Immediate Single-Word Read” operation the Test FIFO will be automatically reset and then all bits of the J3 TTL Data Bus will be driven low (0s). The Test FIFO is now ready (if desired) for another “Immediate Single-Word Read” operation.

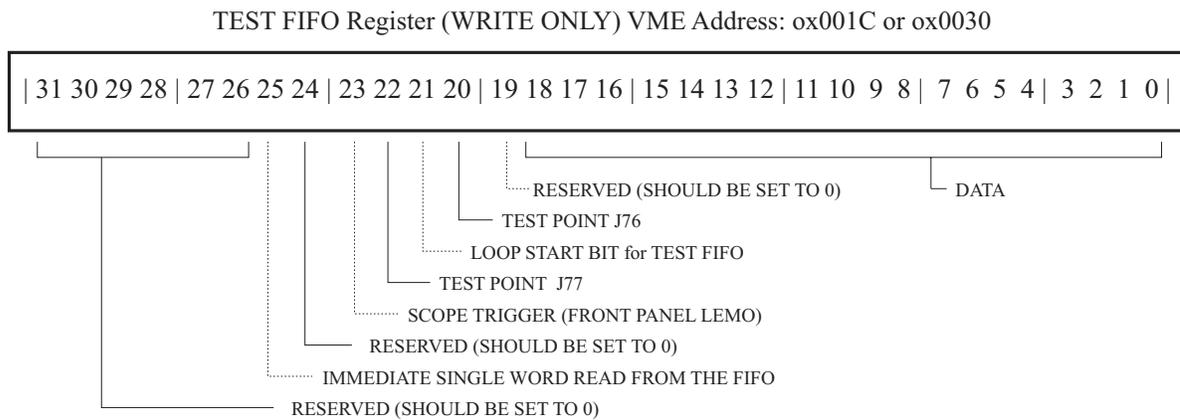


Figure 6.1, Fanout Test FIFO register

**Example:**

1. Read Diagnostic Register (address 0x0020), check that bits 31 and 30 are respectively 0 and 1 (Fanout in INIT Mode), change bit 28 (RESET TFIFO) to a 1 and then write this value back.
2. Write a single word to the Test FIFO Register with bits 31..21 set low (0) and bit 25 set high (1), this bit being high asks for an “Immediate Single Word Read”. Bits 20..1 represent the data-word that will be sent on the J3 TTL Data Bus to the FIBs. The J3 TTL Bus data format is the following:

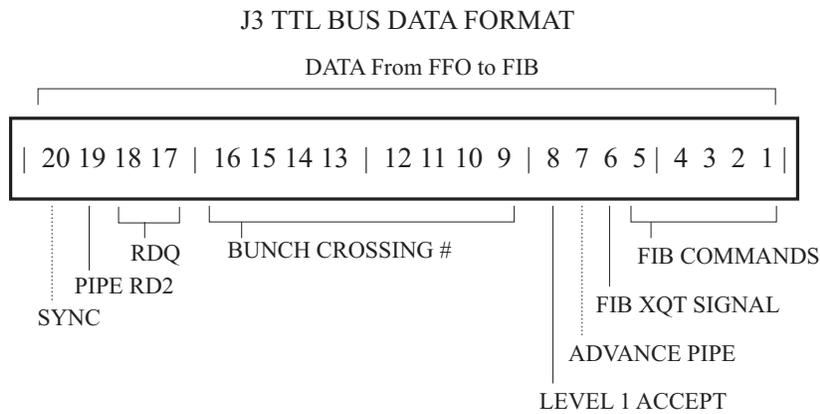


Figure 6.2, J3 TTL bus data format.

Example: Lets say we want send a Data Frame (7 clock cycles) to the FIB containing the command 0x13 (RESET FIB), we should then write to the Test FIFO Register (address 0x001C or 0x0030): **0x02000013**.

3. Repeat step 2 to perform another “Immediate Single-Word Read” operation.

The following figure shows the relevant signals during an “Immediate Single-Word Read” operation.

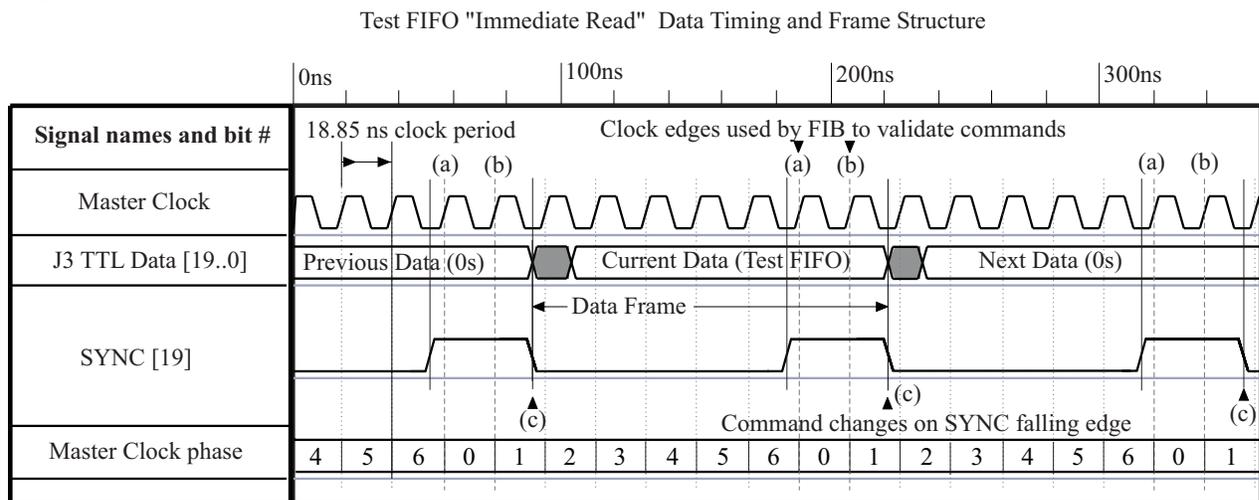


Figure 6.3, Test FIFO timing during an “Immediate Read”.

### 6.1.2 Use of the Test FIFO to send a sequence of commands/data to the FIBs

The Test FIFO allows one to store and send a data sequence to the FIBs. The data should be written to the Test FIFO Register and then “SEND TEST DATA” (bit 25) of the Diagnostic Register should be set in order to start sending the sequence to the FIBs on the J3 TTL Data Bus. Each word stored in the Test FIFO will be kept on the bus for only one clock cycle (not one full command cycle as in the “Immediate Single-Word Read” operation). Before using the TEST FIFO to send a data sequence it is suggested that a “Test FIFO Reset” be executed through the Diagnostic Register. At the end of the sequence the last word written in the Test FIFO will be kept on the bus until the bit “SEND TEST DATA” (bit 25) of the Diagnostic Register is reset to 0. After the desired sequence has been entered into the Test FIFO it is suggested that a “NO-OP” word be written into the FIFO, this will drive the J3 TTL Data Bus low (0s) after the transmission of the sequence (because the “NO-OP” word will be the last word in the FIFO).

#### Example:

- 1 Read the Diagnostic Register (address 0x0020), check that bits 31 and 30 are respectively 0 and 1 (Fanout in INIT Mode), change bit 28 (RESET TFIFO) to 1 and then write this value back. This step is fundamental for the correct operation of the Test FIFO.
- 2 Write a sequence of words to the Test FIFO Register with bits 31..21 set low (0). Bits 20..1 represent the data-word that will be sent on the J3 TTL Data Bus to the FIBs.
- 3 After the sequence has been entered in the Test FIFO through the Test FIFO Register write a NO-OP word (**0x00000000**) if you want to blank (i.e. drive low) the J3 TTL Data Bus after the sequence is sent.
- 4 Read the Diagnostic Register (address 0x0020), set bit 25 (SEND TEST DATA) high (1) and write this value back. The sequence stored in the FIFO is sent on the J3 TTL Data Bus and the last word contained in the FIFO is kept on the bus.
- 5 Read the Diagnostic Register, set bit 25 (SEND TEST DATA) low (0) and write this value back. The FIFO is reset and the J3 TTL Data Bus is driven low (or the value of the last word written into FIFO).
- 6 Repeat from step 2 to send another data sequence.

The following figure shows the relevant signals during the transfer of a command/data sequence of “n” words to the FIBs.

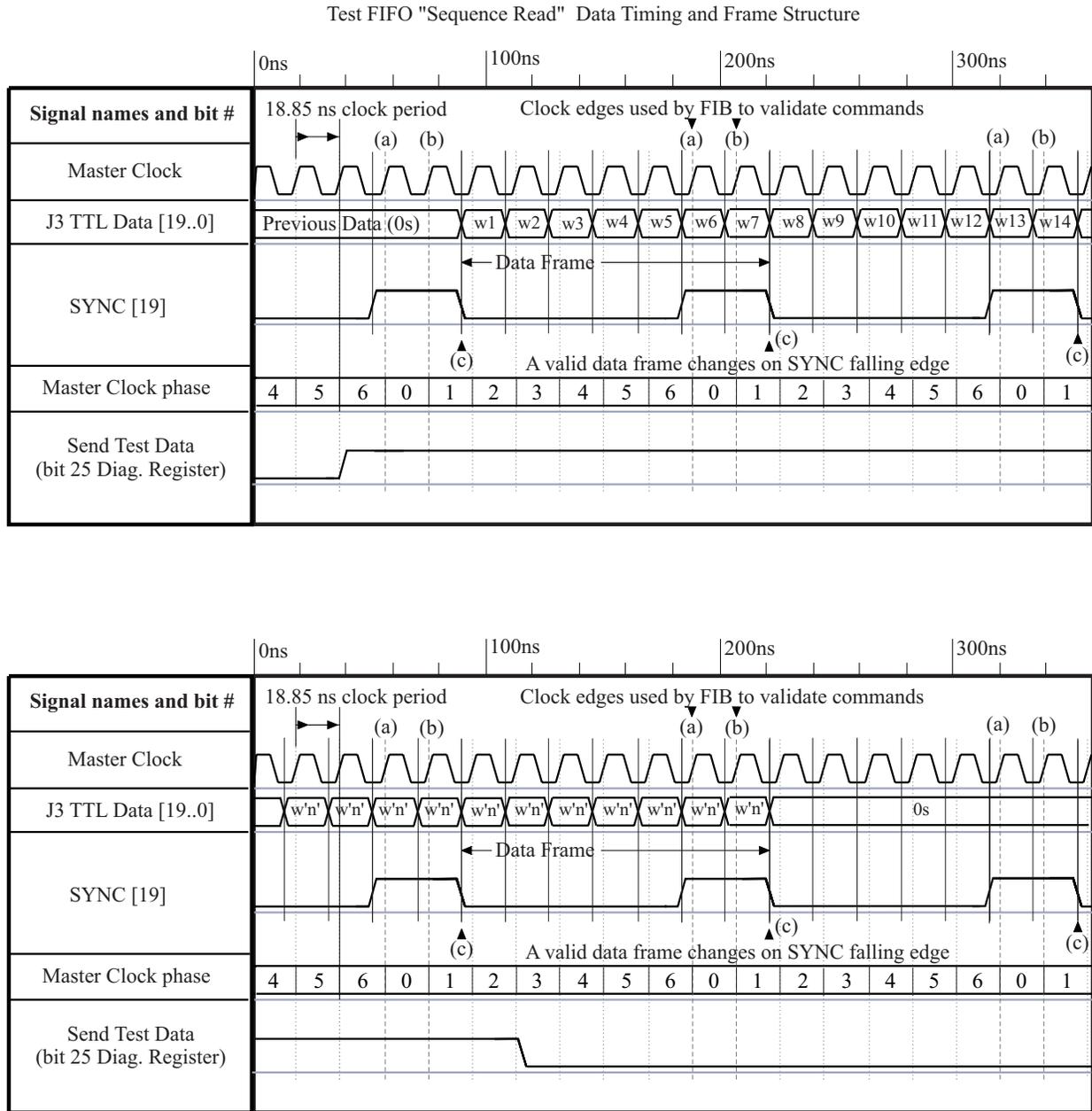


Figure 6.4, Test FIFO timing when a sequence of commands/data is sent to the FIBs

### 6.1.3 Use of the Test FIFO to send a repetitive sequence of commands/data to the FIBs

The Test FIFO allows one to repetitively send a data sequence to the FIB. The use is the same when a command/data sequence is sent, with a few minor differences:

- a) The data sequence to repetitively send should be written to the Test FIFO Register with the “LOOP\_START” bit (bit 21) set high (1). The data loop will start after the second word of the sequence with bit 21 set. In order to maintain the right timing with the SYNC the leading words of the sequence should be five NO-OP 32-bit words (0x00000000) and two NO-OP with bit 21 set (0x00200000)
- b) The “LOOP MODE” will be enabled by setting bit 26 of the Diagnostic Register high (1).

As in the case of a single command/data sequence the bit “SEND TEST DATA” (bit 25) of the Diagnostic Register should be set high (1) in order to start sending the sequence to the FIBs on the J3 TTL Data Bus. Each word stored in the Test FIFO will be kept on the bus for only one clock cycle. Also, in this case before using the TEST FIFO (i.e. before start writing the data into it) it is suggested that a “Test FIFO Reset” command be issued through the Diagnostic Register. The FIFO keeps looping until the module is accessed (read or write) by VME. The FIFO will then be reset and the J3 TTL Data Bus will be driven low (0s).

**Note:** In order to perform the data looping the Test FIFO uses both FIB Fanout module local buses; the one used to drive/read the J3 TTL Data bus (GLD) and the one used by VMEbus to access the module registers (DB). Every VME access to the module will stop the “loop mode” to avoid corruption of the data in the Test FIFO.

#### Example:

- 1 Read the Diagnostic Register (address 0x0020), check that bits 31 and 30 are respectively 0 and 1 (Fanout in INIT Mode), set bit 28 (RESET TFIFO) high (1) and write this value back.
- 2 Write to the Test FIFO Register 5 NO-OP 32-bit words (0x00000000)
- 3 Write to the Test FIFO Register 2 NO-OP words with bit 21 set (0x00200000)
- 4 Write to the Test FIFO Register a sequence of words with bits 31..22 set low (0) and bit 21 set high (1). Bits 20..1 represent the data-word that will be sent on the J3 TTL Data Bus to the FIBs. Every data word should be repeated seven times in order to maintain the correct timing with the SYNC pulse.
- 5 Read the Diagnostic Register (address 0x0020), set bit 26 (LOOP MODE) high (1), set bit 25 (SEND TEST DATA) high (1) and write this value back.
- 6 The sequence stored in the FIFO is repetitively sent out on the J3 TTL Data Bus.
- 7 To Stop the Test FIFO from sending data perform a VME read to address: 0x003C. The FIFO is reset and the J3 TTL Data Bus is driven low (0s).

Note: the leading sequence of NO-OPs in step 2 and 3 can be replaced by a leading sequence of commands. Also, in this case every word should be repeated seven times in order to maintain the correct timing with the SYNC pulse.

### 6.1.4 Use of the Error FIFO for protocol error detection (Error Detection Mode)

The protocol error detection mode can be armed setting bit 23 of the Fanout diagnostic register.

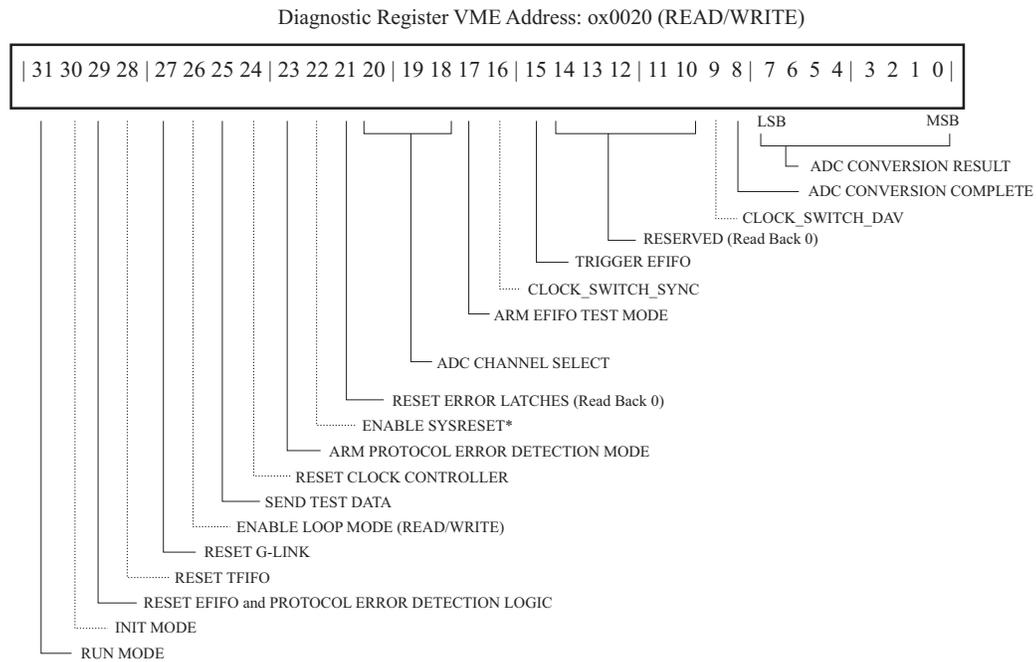


Figure 6.5, Fanout Diagnostic register.

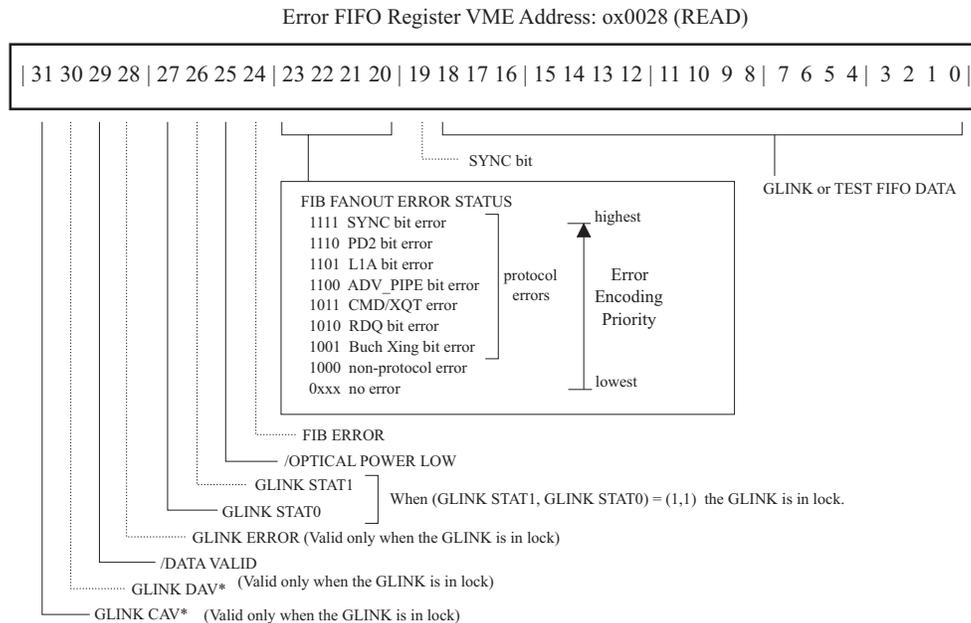


Figure 6.6, Fanout Error FIFO register.

If armed the error detection logic will work both in INITIALIZE mode (data frames from test FIFO) and in RUN mode (data frames from SRC through the optical link). The error FIFO will

continually memorize the data from the G-Link/Test FIFO until a data transfer error is detected, at this point the error FIFO will stop after another 1000 writes. This will leave a data trace in the error FIFO containing 7185 words of pre-trigger and 1000 words of post-trigger data. The data stored in the error FIFO will be accessible through the Error FIFO register (VME address 0x0028).

**Example 1 (Initialize Mode):**

1. Read diagnostic register (address 0x0020), check that bits 31 and 30 are respectively 0 and 1 (Fanout in Initialize Mode), set bit 29 (reset error FIFO and protocol error detection logic), set bit 28 (reset test FIFO), set bit 21 (reset error latches) and then write this value back.
2. Read diagnostic register (address 0x0020), set bit 23 (arm protocol error detection mode) and then write this value back. The error FIFO is memorizing the data stream that is driving the J3 TTL data bus (from test FIFO and local SYNC generator) and is waiting for a trigger from the protocol error detection logic. As soon as an error occurs the front panel error LED will flash and the Error FIFO will stop after 1000 writes. Normally no error should occur during this test. When the error FIFO protocol error detection mode is armed the Fanout will accept a VME trigger and the error FIFO will behave like a protocol error occurred.
3. At this point there are three options:
  - a. Wait for an error to occur.  
Periodically check bit 25 (error FIFO status) of the Fanout error status register (address 0x002C). Reading the error status register will also inform you of several non-protocol errors (Power supplies out of range, FIB errors, etc.).
  - b. Use the test FIFO to send a data sequence containing protocol errors.  
(See examples in section 6.1.1, 6.1.2, 6.1.3).
  - c. Trigger the error FIFO by VME. Read diagnostic register (address 0x0020), set bit 15 (trigger error FIFO) and then write this value back. The error FIFO will behave like a protocol error occurred.
4. After the Error FIFO is triggered it will have 8185 words of the data stream memorized in it. This data is accessible by VME through the error FIFO register (address 0x0028). The error FIFO (Figure 6.6) also stores information about the G-Link connection status, FIB errors and the type of protocol error. Bit 29 of the error FIFO register is the data valid bit it is set to 1 when the data read from the register is not valid (Error FIFO Empty).

**Example 2 (Run Mode):**

1. Read diagnostic register (address 0x0020), check that bits 31 and 30 are respectively 1 and 0 (Fanout in Run Mode), set bit 29 (reset error FIFO and protocol error detection logic), set bit 28 (reset test FIFO), set bit 21 (reset error latches) and then write this value back.
2. Read diagnostic register (address 0x0020), set bit 23 (arm protocol error detection mode) and then write this value back. The error FIFO is memorizing the data stream that is driving the J3 TTL data bus (from G-Link) and is waiting for a trigger from the protocol error detection logic. As soon as an error occurs the front panel error LED will flash and the Error FIFO will stop after 1000 writes. Normally no error should occur during this test. When the error FIFO protocol error detection mode is armed the Fanout will accept a VME trigger and the error FIFO will behave like a protocol error occurred.
3. At this point there are two options:
  - a. Wait for an error to occur.  
Periodically check bit 25 (error FIFO status) of the Fanout error status register (address 0x002C). Reading the error status register will also inform you of several non-protocol errors (Power supplies out of range, FIB errors, G-Link connection status, etc.).
  - b. Trigger the error FIFO by VME. Read diagnostic register (address 0x0020), set bit 15 (trigger error FIFO) and then write this value back.
4. After the Error FIFO is triggered it will have 8185 words of the data stream memorized in it. This data is accessible by VME through the error FIFO register (address 0x0028). The error FIFO (Figure 6.6) also stores information about the G-Link connection status, FIB errors and the type of protocol error. Bit 29 of the error FIFO register is the data valid bit, it is set to 1 when the data read from the register is not valid (Error FIFO Empty).

### 6.1.5 Use of the Error FIFO to check the Test FIFO (Test Mode)

#### Example

1. Read diagnostic register (address 0x0020), check that bits 31 and 30 are respectively 0 and 1 (Fanout in Initialize Mode), set bit 29 (reset error FIFO and protocol error detection logic), set bit 28 (reset test FIFO), set bit 21 (reset error latches) and then write this value back.
2. Read diagnostic register (address 0x0020), set bit 17 (arm error FIFO test mode) and then write this value back. The error FIFO will wait for a trigger from the test FIFO. As soon as the test FIFO starts dumping data onto the J3 backplane TTL data bus the error FIFO will start storing it. The Test FIFO will start dumping data when bit 25 on the diagnostic register (send test data) is set. The Error FIFO will stop storing data when it gets almost full (8185 words) or when the test FIFO stops dumping. When the error FIFO test mode is armed the Fanout will also accept a VME trigger, this causes the Error FIFO to store an after trigger sequence of 8185 words.
3. At this point there are four options:
  - a. Use the test FIFO immediate single word read (see example in section 6.1.1). The error FIFO will store 7 words of data.
  - b. Use the test FIFO to send a data sequence (see example in section 6.1.2). The error FIFO will store the data sequence and will keep storing data until it gets almost full (8185 words).
  - c. Use the test FIFO to send a repetitive data sequence (see example in section 6.1.3). The error FIFO will store data until it gets almost full (8185 words).
  - d. Trigger the error FIFO by VME. Read diagnostic register (address 0x0020), set bit 15 (trigger error FIFO) and then write this value back. The error FIFO will store 8185 words of post-trigger data.
4. After the Error FIFO is triggered it will have between 7 (option a) and 8185 words of the data stream memorized in it. This data is accessible by VME through the error FIFO register (address 0x0028). Bit 29 of the error FIFO register is the data valid bit, it is set to 1 when the data read from the register is not valid (Error FIFO Empty).

Use of the Error FIFO as transaction memory (VME Trigger)

The error FIFO can be triggered at any time by VME (diagnostic register bit 15). If the Error FIFO test mode is armed the error FIFO will store 8185 words of post-trigger data, in all the other cases (no mode armed or protocol error detection mode armed) the error FIFO will store 7185 words of pre-trigger and 1000 words of post-trigger data. See sections 6.1.4 and 6.1.5.

### 6.1.6 Setting the FIB Fanout to report errors to the SRC via the SRC status cable

Each of the four status bit mapping registers (see section 3.1.8):

Status bit 0 mapping register (address 0x0008)

Status bit 1 mapping register (address 0x000C)

Status bit 2 mapping register (address 0x0010)

Status bit 3 mapping register (address 0x0014)

Provides 29 bits of selection, where each bit corresponds to a status or error condition that the Fanout monitors. If the bit is set in the register, the state of that error or status condition is OR-ed with all other selected conditions to create the status bit. Some error conditions are latched by the FIB Fanout (see paragraphs 3.1.8 and 3.1.9), the latches can be reset by VME (diagnostic register bit 21) or by the SRC (command 3E, see Table 2.2).

#### **Example:**

Setting the Fanout to report the following error conditions to the SRC:

- G-Link not in lock on status bit 0;
- Fanout Initialize Mode on status bit 1;
- FIB Errors on Status bit 2;
- Protocol Errors on Status bit 3.

1. Reset the error latches setting bit 21 of diagnostic register (address 0x0020);
1. Write 0x00000008 to Status bit 0 mapping register (address 0x0008);
2. Write 0x0000200 to Status bit 1 mapping register (address 0x000C);
3. Write 0x00003C00 to Status bit 2 mapping register (address 0x0010);
4. Write 0x001FC000 to Status bit 3 mapping register (address 0x0014);

### 6.1.7 Checking the SRC Status Cable connection

See section 3.8 for a description of the SRC status cable interface.

The SRC status cable connection can be checked using VME accesses to the Fanout status bit mapping registers or using commands sent on the optical link from the SRC.

#### Example (using the Fanout status bit mapping registers):

In order to test the status cable the mapping all the error conditions should be disabled writing 0x00000000 to the mapping registers. Bit 28 (set the status bit of SRC) can then be used to set and reset the status lines to check their functionality. To perform this test the cable could be connected to the SRC or to a multi-meter (to verify the presence of the correct TTL levels).

#### Example (using the SRC commands on the optical link):

There is a set of SRC commands specific to the FIB Fanout (see Table 2.2), these commands are considered as no-ops by the FIBs. Three SRC commands allow the SRC to test the status cable connection: 0x3A, 0x3B and 0x3C.

1. Send the command 0x3A on the optical link. When the Fanout receives the command 0x3A all four status bits will be forced high, this condition will persist until command 0x3B or 0x3C is received or the error logic is reset (diagnostic register bit 29).
2. Send the command 0x3B on the optical link. When the Fanout receives the command 0x3B all four status bits will be forced low, this condition will persist until command 0x3A or 0x3C is received or the error logic is reset (diagnostic register bit 29).
3. Send the command 0x3C on the optical link. When the Fanout receives the command 0x3C all four status bits will be return to their normal reporting mode (as configured by the four status bit mapping registers).

### 6.1.8 Measuring the ECL power supplies voltages

The on-board ADC controlled by the diagnostic register (section 3.1.5) allows measuring the ECL power supply voltages. ADC channels #3 and #6 allow monitoring of the  $V_{EE}$  (-5.2 Volt) and the  $V_{TT}$  (-2.0 Volt) voltages

Example (measuring  $V_{EE}$ ):

1. Read diagnostic register (address 0x0020), set bits 20, 19 and 18 (ADC channel select) to 011 (ADC channel 3) and then write this value back. The ADC starts a new conversion every time the diagnostic register is accessed by being written to and the result is available on the next read access.
2. Read diagnostic register (address 0x0020), verify that bit 8 is set (ADC conversion complete), bits [7..0] represent the conversion result. Use Table 3.7 to convert the read value to a voltage. If for example the read value is 0x1E the corresponding voltage is 2.35Volts.
3. Convert the voltage to the actual value using the formula (from section 3.1.5.4):

$$V_{EE} = -(100/47) * V_{ADC-ch3} \text{ [Volts]}$$

Using 2.35Volts we obtain:

$V_{EE} = -5.0$  Volts (you better check the test-stand power supply as the voltage is too positive).

### 6.1.9 Measuring the temperature of the PCB

The on-board ADC controlled by the diagnostic register (section 3.1.5) allows measuring the temperature of the printed circuit board. ADC channels #1 and #2 are connected to the two temperature sensors installed on the Fanout (top and bottom of the module on the component side).

Example (temperature sensor on the bottom of the board)

1. Read diagnostic register (address 0x0020), set bits 20, 19 and 18 (ADC channel select) to 010 (ADC channel 2) and then write this value back. The ADC starts a new conversion every time the diagnostic register is accessed by being written to and the result is available on the next read access.
2. Read diagnostic register (address 0x0020), verify that bit 8 is set (ADC conversion complete), bits [7..0] represent the conversion result. Use Table 3.7 to convert the read value to a voltage. If for example the read value is 0x17 the corresponding voltage is 4.55Volts.
3. Convert the voltage to a temperature value using the formulas (from section 3.1.5.3):

$$\text{Temp [C}^\circ\text{]} = 20 * V_{\text{ADC}} [\text{Volts}]; \quad (\text{range } 2 \text{ C}^\circ \leq \text{Temp [C}^\circ\text{]} \leq 100 \text{ C}^\circ)$$

$$\text{Temp [F}^\circ\text{]} = 32 + 36 * V_{\text{ADC}} [\text{Volts}]; \quad (\text{range } 35.6 \text{ F}^\circ \leq \text{Temp [F}^\circ\text{]} \leq 212 \text{ F}^\circ).$$

Using 4.55Volts we obtain:

$$\text{Temp} = 91 \text{ C}^\circ = 195.8 \text{ F}^\circ. \text{ (you better check the cooling system).}$$

### 6.1.10 Measuring the optical power received by the G-Link receiver.

The on-board ADC controlled by the diagnostic register (section 3.1.5) allows measuring the optical power received by the G-Link receiver. The ADC channels #0 is the one connected to the G-Link receiver.

Example:

1. Read diagnostic register (address 0x0020), set bits 20, 19 and 18 (ADC channel select) to 000 (ADC channel 0) and then write this value back. The ADC starts a new conversion every time the diagnostic register is accessed by being written to and the result is available on the next read access.
2. Read diagnostic register (address 0x0020), verify that bit 8 is set (ADC conversion complete), bits [7..0] represent the conversion result. Use Table 3.7 to convert the read value to a voltage. If for example the read value is 0xD8 the corresponding voltage is 0.53Volts.
3. Convert the voltage to the optical power using Figure 3.6.

Using 0.53Volts we obtain:

$$\text{Optical power} = -11\text{dBm} = 0.28\text{mWatt}. \text{ (you are going to get soon a mix of protocol errors, G-Link errors, etc.).}$$

### 6.2 Module and subrack keying.

The VIPA subracks used for the upgrade electronics allows for keying of the module front panels to control insertion of cards into the subrack. The keying system uses six keying locations in the front panel, three on top and three on the bottom. Each location accepts a plastic key insertable in four different position or no key at all. [Ref.6, 7]. The keying system has the following goals:

- a) Protect the boards and backplanes from power supply incompatibilities.
- b) Protect boards and backplanes from incompatibilities between the SVX and CDF style VIPA crates.
- c) Protect pins on boards and backplanes from incompatible J3 (P5/P6) connectors.
- d) Protect boards from incompatible user defined signals.
- e) Aid ensuring that modules are inserted in the correct slot in each crate.

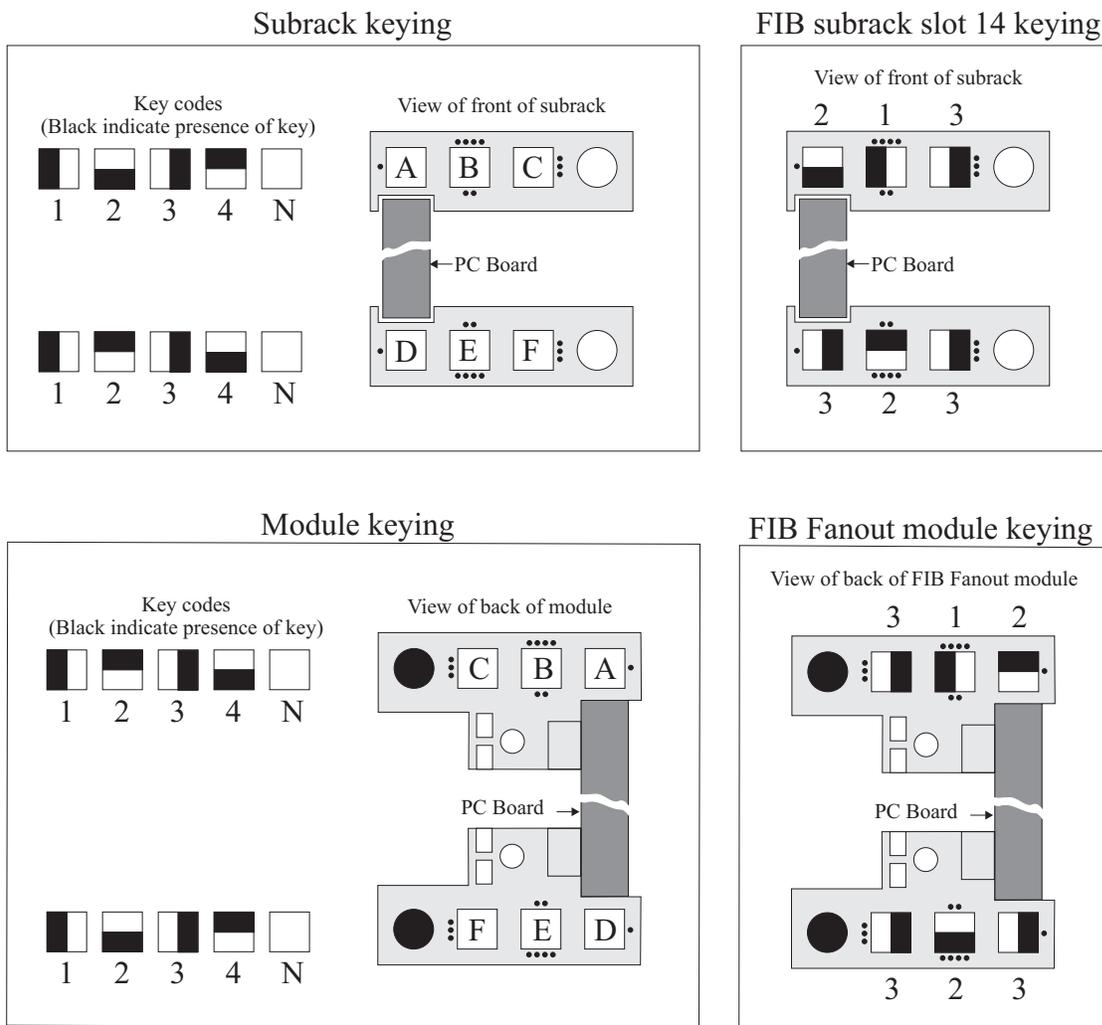


Figure 6.7, Keying of Fanout module and FIB subrack slot 14.

### 6.3 List of FIB Fanout technical documentation

- a) Board electrical schematic. The board was designed using OrCAD Schematic Capture 7.2 and OrCAD Layout 7.10b [Ref.36]. A separate document contain the schematic.
- b) Synario schematics and ABEL files for the ten Lattice Semiconductor programmable logic chips on the FIB Fanout [Ref.35] [Ref.37]. The schematic and the ABEL files are available in separate documents.
- c) Testing procedure for the FIB Fanout module [Ref.39].
- d) Components data sheets. Listed in section 6.8 and available on the internet from the chips manufacturers.

### 6.4 List of Rev.B FIB Fanout boards produced

Board serial number	PREP tracking number	G-Link receiver serial number
100	550302	028
101	550303	021
102	550304	026
103	550305	033
104	550312	031
105	550313	020
106	550314	019
107	550315	023
108	550316	027
109	550317	029
110	550318	032
111	550319	022
112	550320	024
113	550321	030

Table 6.1, List of Rev.B FIB Fanout produced

### 6.5 State Machines

The following figures show the state machines implemented on the FIB Fanout programmable logic. For a full understanding of the programmable logic you need to refer to the programmable logic schematics/ABEL files [Ref.35] and to the FIB Fanout OrCAD schematic [Ref.36].

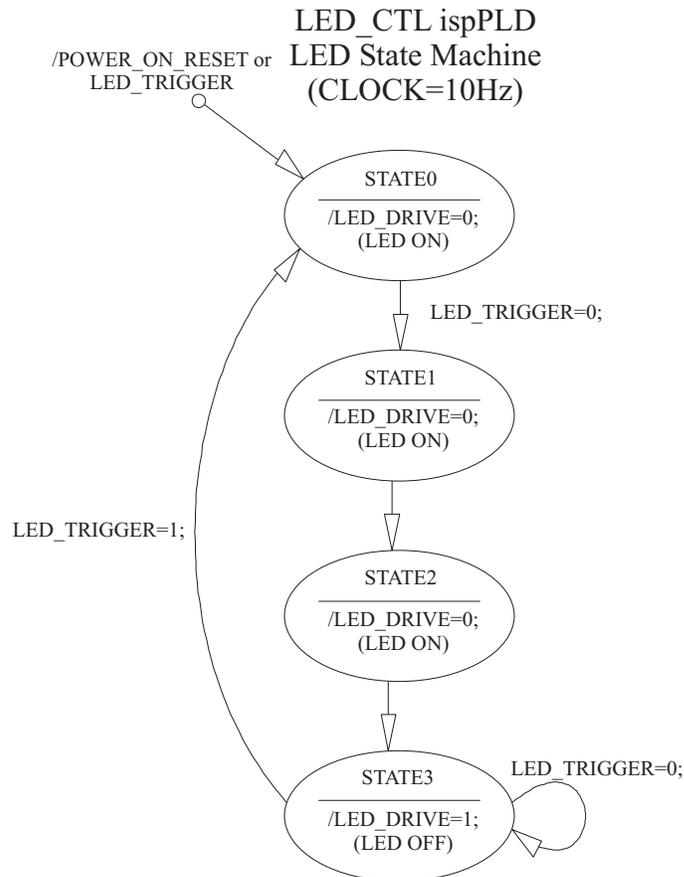


Figure 6.8, LED State Machine.

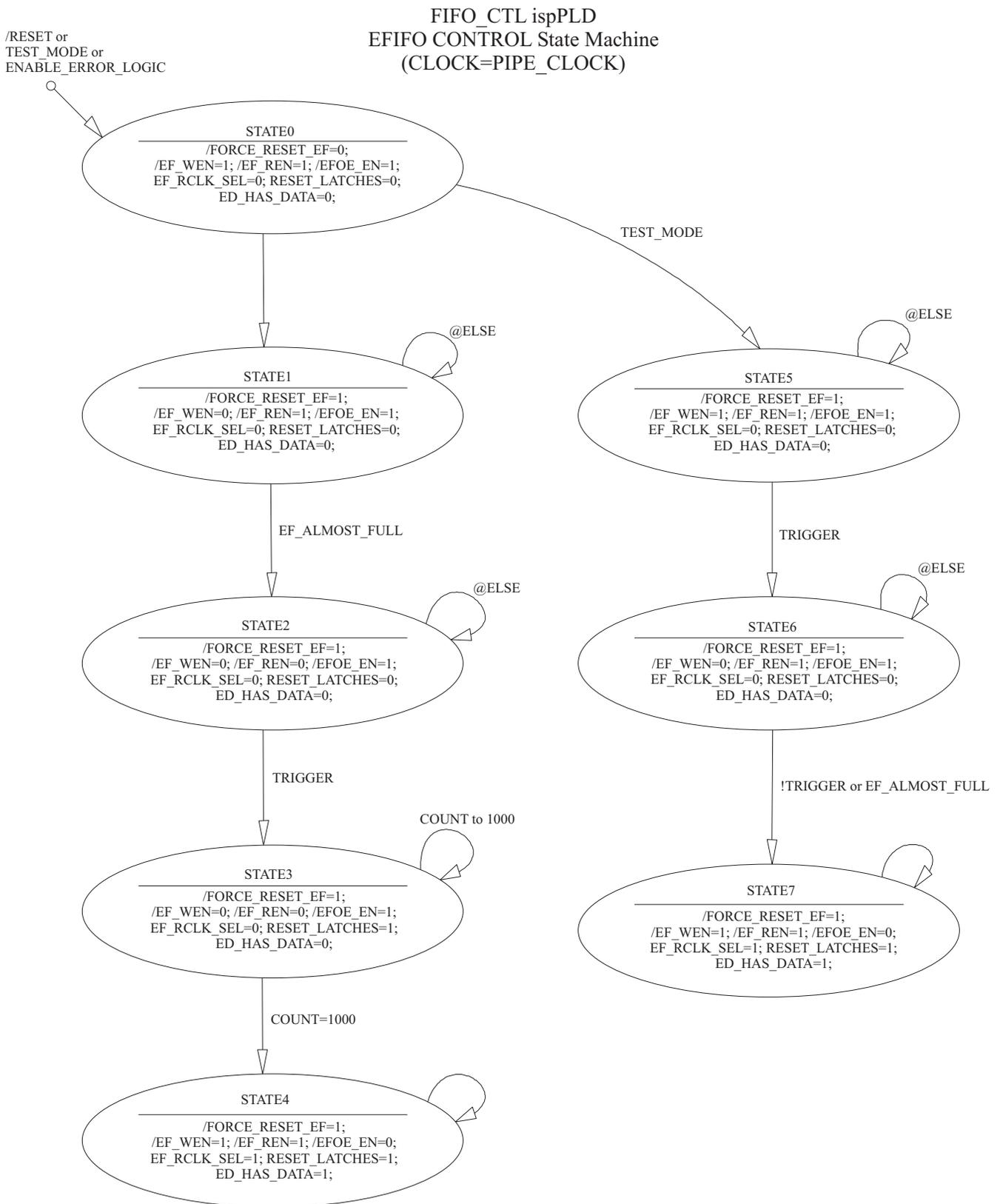


Figure 6.9, Error FIFO State Machine

FIFO\_CTL ispPLD  
TFIFO State Machine  
(CLOCK=LOCAL CLOCK)

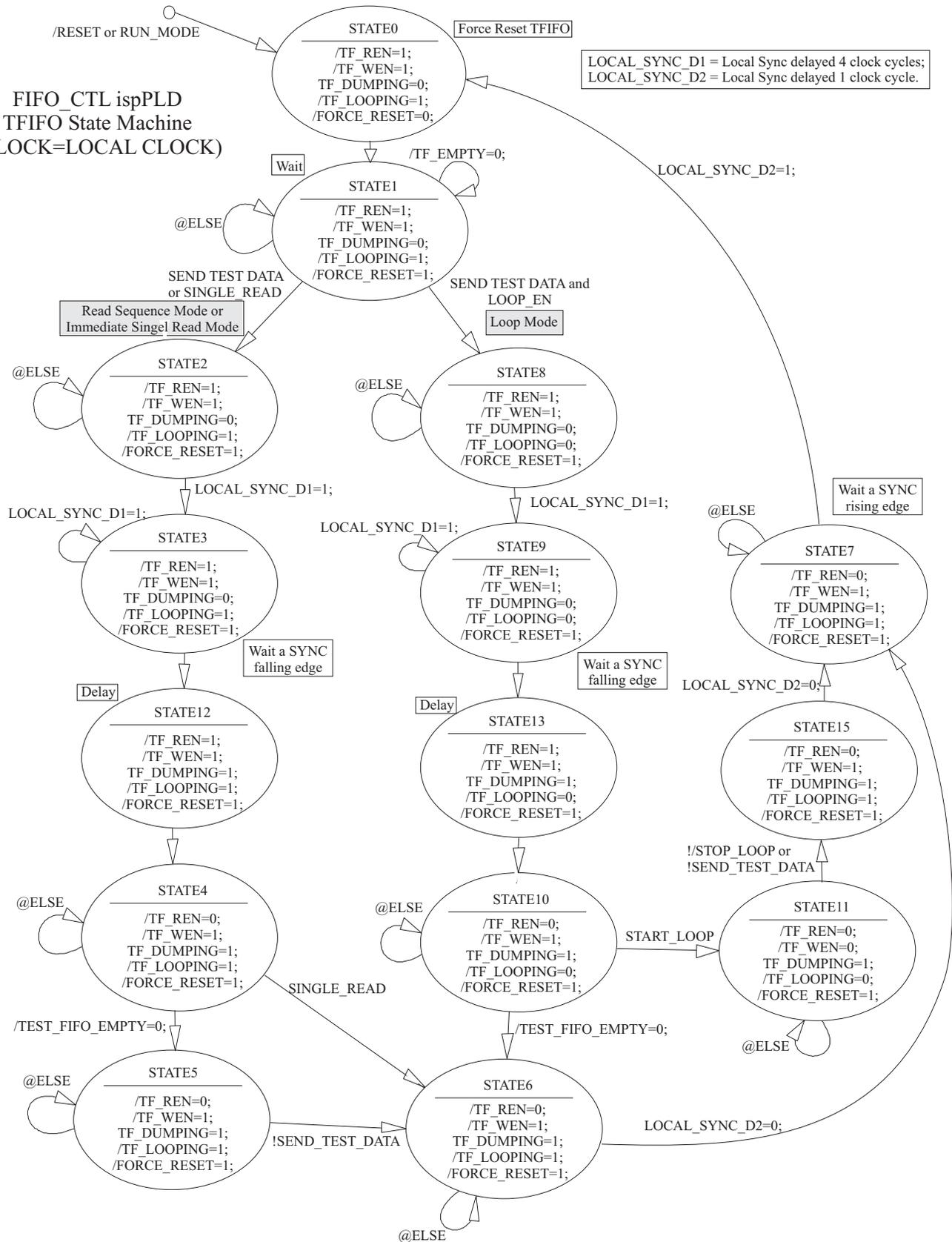


Figure 6.10, Test FIFO State Machine



Figure 6.11, Master State Machine.

CLK\_CTL ispPLD RUN State Machine  
(CLOCK=LOCAL CLOCK)

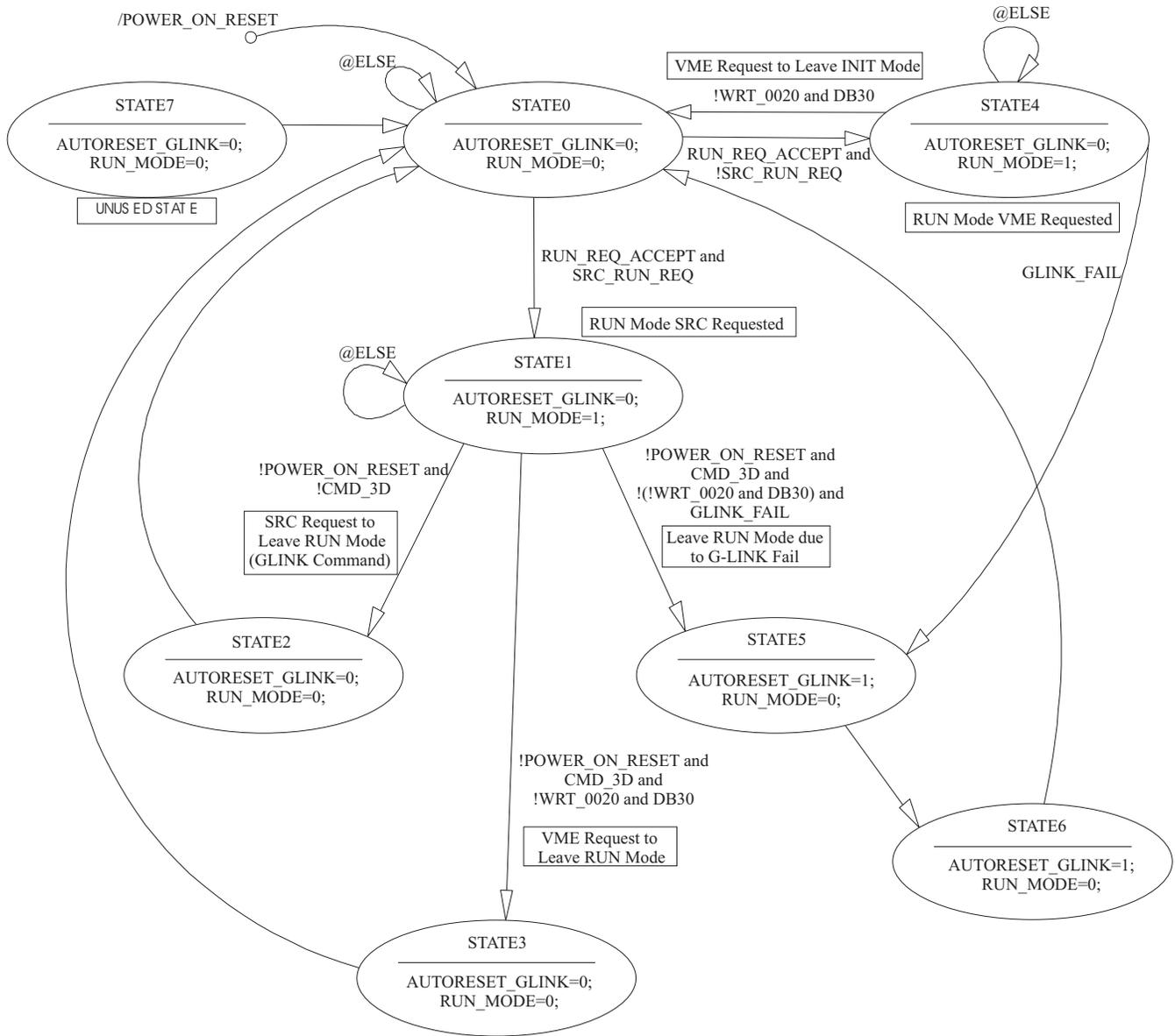


Figure 6.12, RUN Mode State Machine.

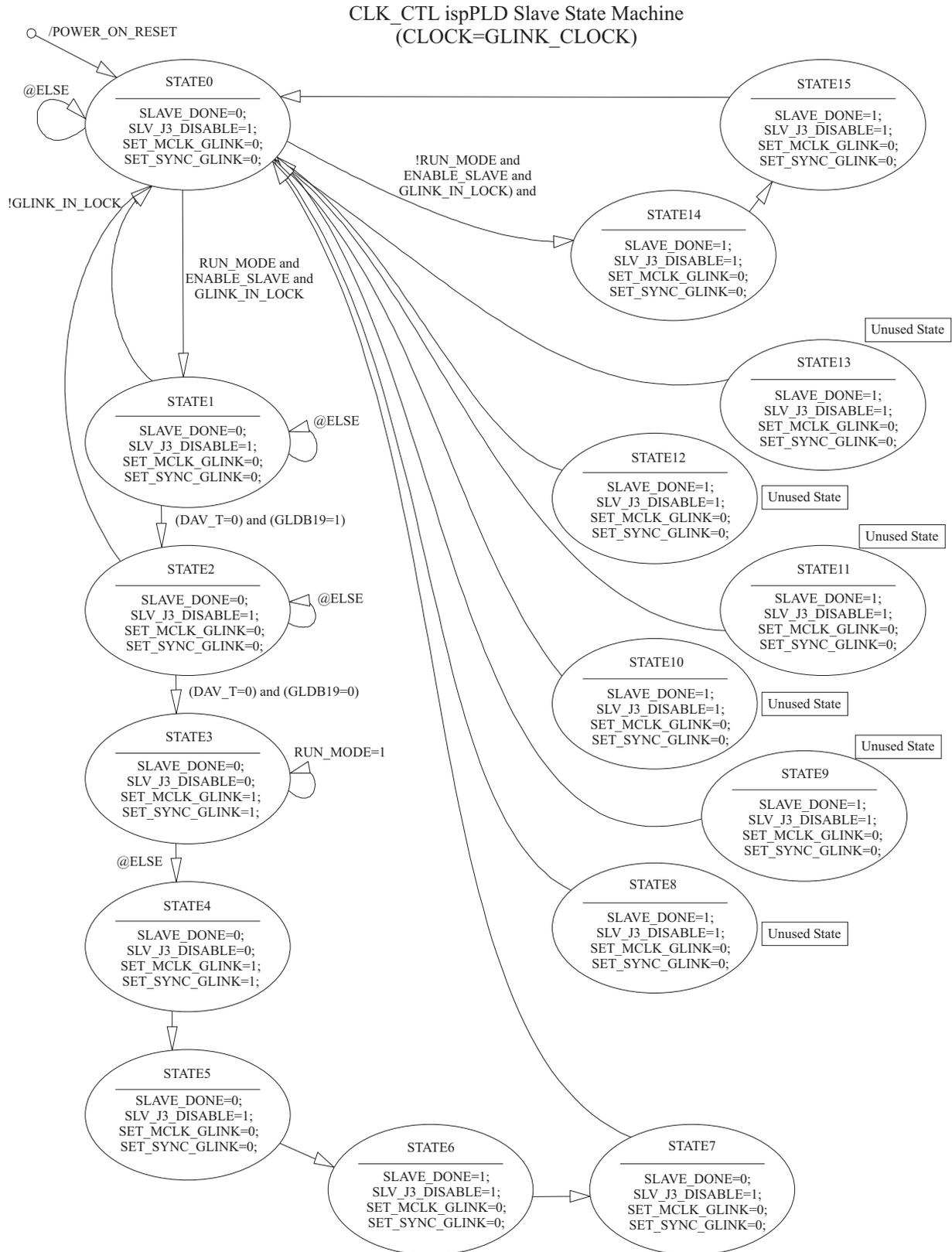


Figure 6.13, Slave State Machine.

### 6.6 Making changes to the programmable logic

The software used to design/produce the programmable logic is the ISP Synario Software KIT Version 5.0 and the ispGDX Version 1.5.1 (only for the GDX part) from Lattice Semiconductor Co. [Ref.15, 16, 17]. The programmable logic design is organized in directories, one for each programmable logic chip on the FIB Fanout. After the desired modification is applied to the programmable logic code/schematic the design should be recompiled. The FIB Fanout programmable logic chips affected by the modifications can be reprogrammed as described in section 6.7. The programmable logic schematics and ABEL Files are provided in a separate document [Ref.35].

### 6.7 Reprogramming the In-System Programmable logic.

Software: ISP Daisy Chain Download Version 5.1 from Lattice Semiconductor Co [Ref.15, 16, 17].

Hardware: IBM compatible Personal Computer (486 or greater) and a parallel port cable.

Data: Download configuration file (extension .DLD), a JEDEC file (extension .JED) for each of the 10 programmable chip on the FIB Fanout.

The Lattice Semiconductor ISP Daisy Chain Download (ispDCD) software provides a tool for downloading (programming) designs onto programmable logic devices (PLDs) singly or in a daisy chain. The FIB Fanout has ten Lattice programmable chips which can be reprogrammed using the ispDCD software, a PC and a parallel port cable connected to the PC and to the front panel ISP connector of the Fanout. For further instruction see the ispDCD software help file.

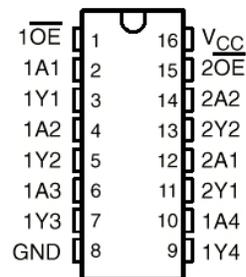
Index #	Lattice Device [Ref.16, 17]	Orcad schematic chip identifier	Programmable logic name	Jedec file
1	1032E	U28	FIFO controller	FIFO_CTL.JED
2	1032E	U42	Clock controller	CLK_CTL.JED
3	1032E	U56	VME interface	VME_INT.JED
4	1032E	U26	Error latch	ERRLATCH.JED
5	1032E	U36	Error decoder 1	ERRDEC1.JED
6	2032	U7	LED controller 1	LEDCTL1.JED
7	2032	U8	LED controller 2	LEDCTL2.JED
8	1032E	U14	Error decoder 2	ERRDEC2.JED
9	1032E	U43	Error pipe	ERR_PIPE.JED
10	GDX160	U37	GDX	FAN_GDX.JED

Table 6.2, Programmable logic daisy chain information.

## 6.8 Parts List

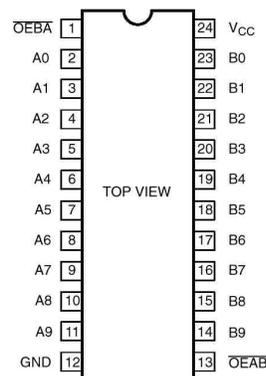
### 6.8.1 74HC367N - Hex Bus Driver with Tri-State Outputs

<i>Part Number</i> 74HC367N	<i>Package</i> 16-Pin 300 mil Dip
<i>PC Board Reference</i> U6 [Ref.36].	<i>Quantity</i> 1
<i>Data Sheet file</i> slcs309b.pdf	<i>Manufacturer</i> Texas Instruments [Ref.19]



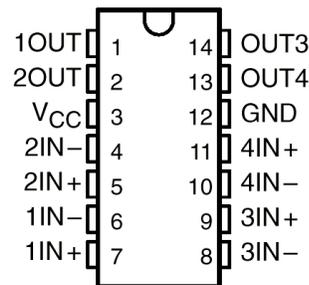
### 6.8.2 74ABT861PW-DH - 10-Bit BUS Transceiver

<i>Part Number</i> 74ABT861PW-DH	<i>Package</i> 24-Pin TSSOP
<i>PC Board Reference</i> U60, U61 [Ref.36].	<i>Quantity</i> 2
<i>Data Sheet file</i> 74ABT861_2.pdf	<i>Manufacturer</i> Philips [Ref.27]



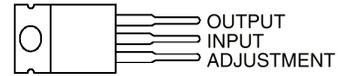
### 6.8.3 LM339AN - Quad Differential Comparator

<i>Part Number</i> LM339AN	<i>Package</i> 14-Pin 300 mil Dip
<i>PC Board Reference</i> U13, U29 [Ref.36].	<i>Quantity</i> 2
<i>Data Sheet file</i> slcs006c.pdf	<i>Manufacturer</i> Texas Instruments [Ref.19]



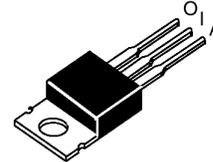
**6.8.4 LM337 - 3-Terminal Adjustable Negative Regulator**

<i>Part Number</i> LM337	<i>Package</i> TO-220AB
<i>PC Board Reference</i> U23, U41 [Ref.36].	<i>Quantity</i> 2
<i>Data Sheet file</i> LM137.pdf, slvs047b.pdf	<i>Manufacturer</i> National Semiconductor [Ref.18], Texas Instruments [Ref.19].



The input terminal is in electrical contact with the mounting base.

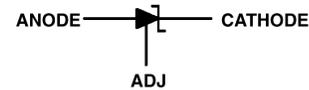
TO-220AB



**6.8.5 LM336BZ-2.5 - 2.5V Integrated Reference Circuit**

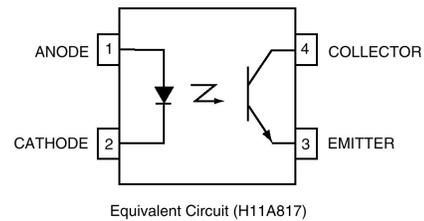
<i>Part Number</i> LM336BZ-2.5	<i>Package</i> LP (Plastic Cylindrical)
<i>PC Board Reference</i> REF1, REF2 [Ref.36].	<i>Quantity</i> 2
<i>Data Sheet file</i> slvs063a.pdf	<i>Manufacturer</i> Texas Instruments [Ref.19].

LP PACKAGE (TOP VIEW)



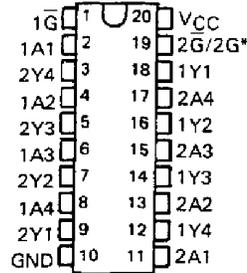
**6.8.6 H11A817B – 4-pin Phototransistor Optocoupler**

<i>Part Number</i> H11A817BQT	<i>Package</i> 4-Pin Dip
<i>PC Board Reference</i> U5 [Ref.36].	<i>Quantity</i> 1
<i>Data Sheet file</i> h11A817.pdf	<i>Manufacturer</i> QT Optoelectronics [Ref.21].



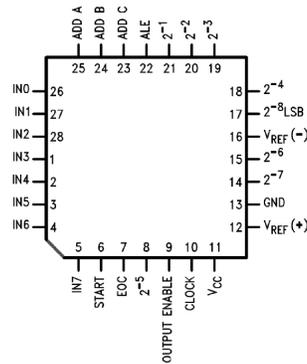
**6.8.7 74ALS244 – Octal Buffer and Line Driver with 3-State Outputs**

<i>Part Number</i> 74ALS244AN	<i>Package</i> 20-Pin 300 mil Dip
<i>PC Board Reference</i> U23, U4 [Ref.36].	<i>Quantity</i> 2
<i>Data Sheet file</i> sdl144.pdf	<i>Manufacturer</i> Texas Instruments [Ref.19].



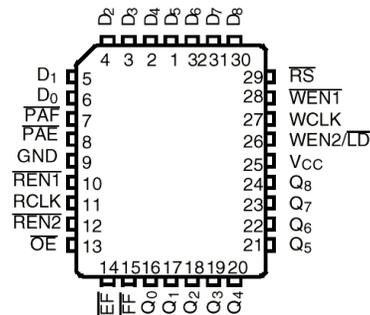
**6.8.8 ADC0808 – 8-bit  $\mu$ P compatible A/D Converter with 8-Channel Analog Multiplexer**

<i>Part Number</i> ADC0808CCV	<i>Package</i> 28-Pin PLCC
<i>PC Board Reference</i> U30 [Ref.36].	<i>Quantity</i> 1
<i>Data Sheet file</i> ADC0808.pdf	<i>Manufacturer</i> National Semiconductor [Ref.18].



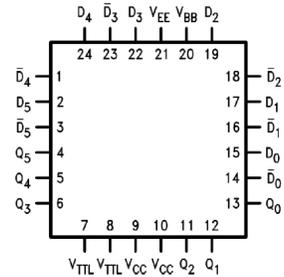
**6.8.9 CY7C4251 – 8K x 9 Synchronous FIFO**

<i>Part Number</i> CY7C4251-15JC	<i>Package</i> 32-Pin PLCC
<i>PC Board Reference</i> U31,U32,U33, U34, U38, U39, U40 [Ref.36].	<i>Quantity</i> 7
<i>Data Sheet file</i> cy7c42x1.pdf	<i>Manufacturer</i> Cypress Semiconductor [Ref.25].



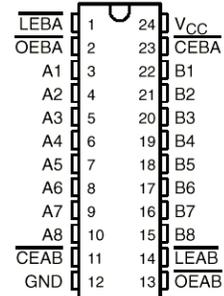
**6.8.10 SY100S325JC - Low-Power Hex ECL-to-TTL Translator**

<i>Part Number</i> SY100S325JC		<i>Package</i> 28-Pin PLCC	
<i>PC Board Reference</i> U20, U22 [Ref.36].		<i>Quantity</i> 2	
<i>Data Sheet file</i> 100325.pdf	<i>Manufacturer</i> National Semiconductor [Ref.18], Synergy Semiconductor [Ref.28].		



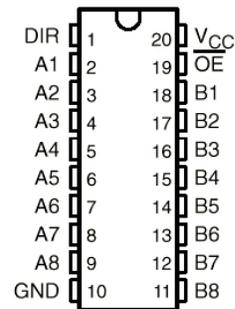
**6.8.11 74F543 – Octal Registered Transceiver with 3-State Outputs**

<i>Part Number</i> 74F543SPC		<i>Package</i> 24-Pin 300 mil Dip	
<i>PC Board Reference</i> U54, U55, U58, U59 [Ref.36].		<i>Quantity</i> 4	
<i>Data Sheet file</i> sdfs025b.pdf	<i>Manufacturer</i> Texas Instruments [Ref.19].		



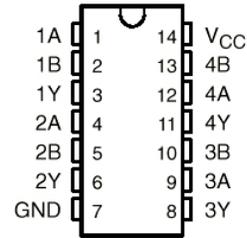
**6.8.12 74F245 - Octal Bus Transceiver**

<i>Part Number</i> 74F245PC		<i>Package</i> 20-Pin 300 mil Dip	
<i>PC Board Reference</i> U57 [Ref.36].		<i>Quantity</i> 1	
<i>Data Sheet file</i> sdfs010a.pdf	<i>Manufacturer</i> Texas Instruments [Ref.19].		



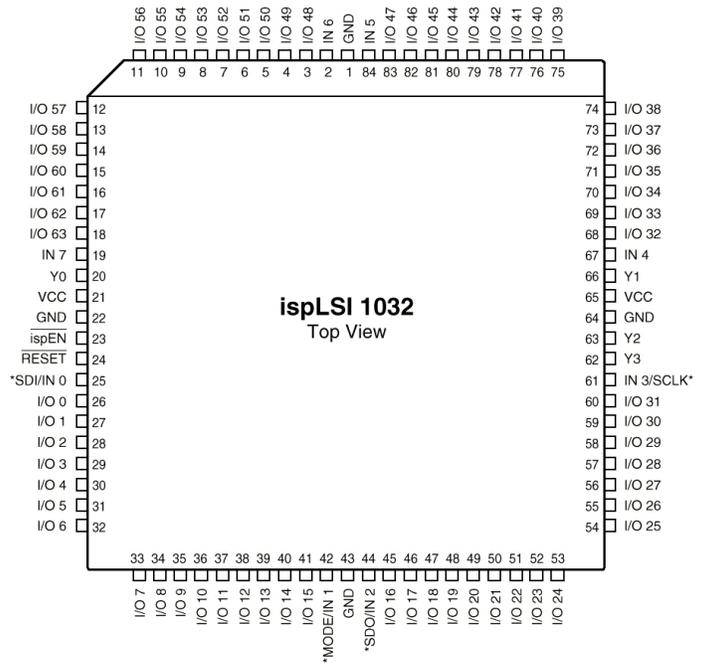
**6.8.13 74AS00N - Quadruple 2-Input Positive NAND Gates**

<i>Part Number</i> 74AS00N	<i>Package</i> 14-Pin 300 mil Dip
<i>PC Board Reference</i> U27 [Ref.36].	<i>Quantity</i> 1
<i>Data Sheet file</i> sdas187a.pdf	<i>Manufacturer</i> Texas Instruments [Ref.19].



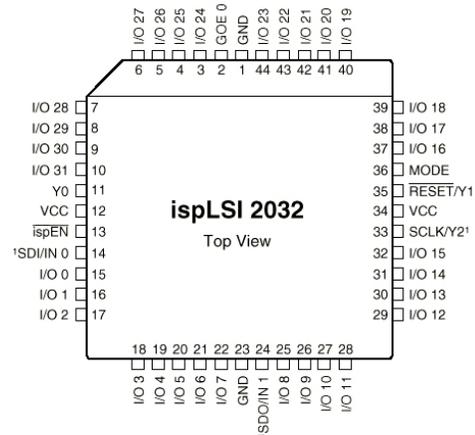
**6.8.14 ispLSI1032 – In-System programmable High Density PLD**

<i>Part Number</i> ispLSI1032-100LJ	<i>Package</i> 84-Pin PLCC
<i>PC Board Reference</i> U14,U26, U28 U36, U42, U43, U56 [Ref.36].	<i>Quantity</i> 7
<i>Data Sheet file</i> 1032.pdf, 1032e.pdf	<i>Manufacturer</i> Lattice Semiconductor [Ref.16]



**6.8.15 ispLSI2032 - In-System programmable High Density PLD**

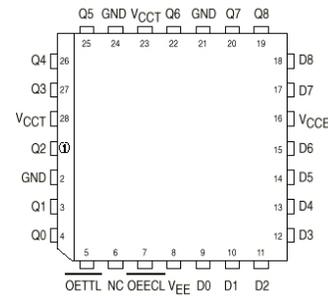
<i>Part Number</i> ispLSI2032-80LJ	<i>Package</i> 44-Pin PLCC
<i>PC Board Reference</i> U7, U8 [Ref.36].	<i>Quantity</i> 2
<i>Data Sheet file</i> 2032e.pdf, 2032e.pdf	<i>Manufacturer</i> Lattice Semiconductor [Ref.16].



1. Pins have dual function capability.

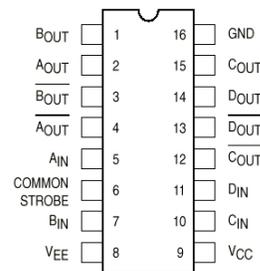
**6.8.16 MC10H601 – 9-bit ECL/TTL Translator**

<i>Part Number</i> MC10H601FN	<i>Package</i> 28-Pin PLCC
<i>PC Board Reference</i> U46, U47, U48 [Ref.36].	<i>Quantity</i> 3
<i>Data Sheet file</i> mc10h601rev7.pdf	<i>Manufacturer</i> Motorola [Ref.26].



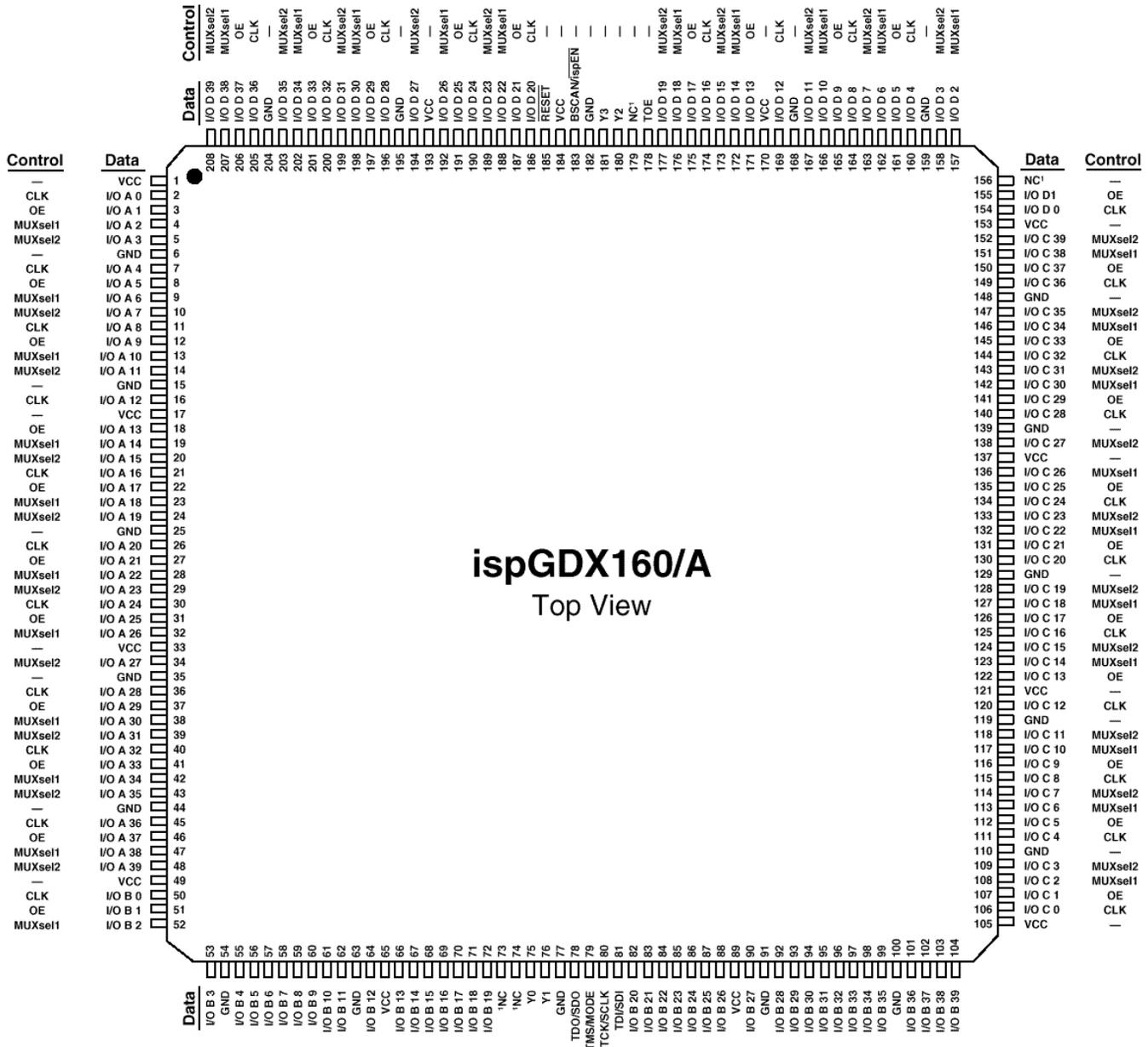
**6.8.17 MC10H124 – QUAD TTL to MECL Translator with TTL Strobe Input**

<i>Part Number</i> MC10H124P	<i>Package</i> 16-Pin 300 mil Dip
<i>PC Board Reference</i> U49 [Ref.36].	<i>Quantity</i> 1
<i>Data Sheet file</i> mc10h124rev6.pdf	<i>Manufacturer</i> Motorola [Ref.26].



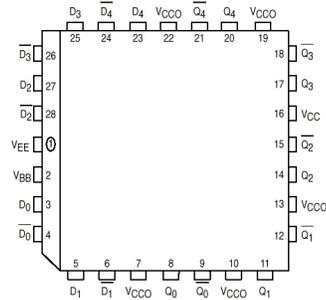
6.8.18 ispGDX160 - Generic Digital Crosspoint Device

<i>Part Number</i> ispGDX160-7Q208	<i>Package</i> 208-Pin SOIC	<i>PC Board Reference</i> U37 [Ref.36].	<i>Quantity</i> 1
<i>Data Sheet file</i> gdxarch.pdf, gdxarch.pdf, introgdx.pdf, ispgdx.pdf	<i>Manufacturer</i> Lattice Semiconductor [Ref.17]		



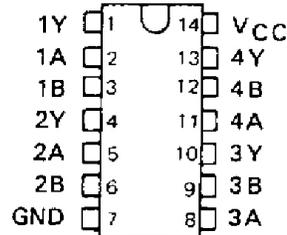
**6.8.19 MC10E116 – Quint Differential Line Receiver**

<i>Part Number</i> MC10E116FN	<i>Package</i> 28-Pin PLCC	
<i>PC Board Reference</i> U15, U16, U17, U19, U21 [Ref.36].		<i>Quantity</i> 5
<i>Data Sheet file</i> mc10e116rev3a.pdf	<i>Manufacturer</i> Motorola [Ref.26].	



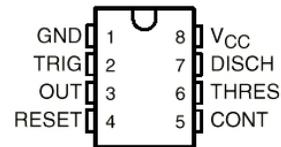
**6.8.20 SN74LS01 - QUAD 2-Input Positive-NAND Gates with Open Collector Outputs**

<i>Part Number</i> SN74LS01N	<i>Package</i> 14-Pin 300 mil Dip	
<i>PC Board Reference</i> U10 [Ref.36].		<i>Quantity</i> 1
<i>Data Sheet file</i> sdl026.pdf	<i>Manufacturer</i> Texas Instruments [Ref.19].	



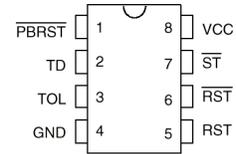
**6.8.21 NE555 – Precision Timer**

<i>Part Number</i> NE555P	<i>Package</i> 8-Pin 300 mil Dip	
<i>PC Board Reference</i> U3, U9 [Ref.36].		<i>Quantity</i> 2
<i>Data Sheet file</i> slfs022.pdf	<i>Manufacturer</i> Texas Instruments [Ref.19].	



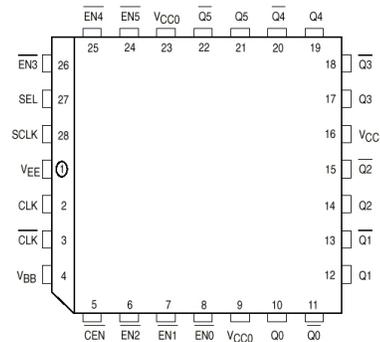
**6.8.22 DS1232 – Micro Monitor**

<i>Part Number</i> DS1232	<i>Package</i> 8-Pin 300 mil Dip	
<i>PC Board Reference</i> U11 [Ref.36].		<i>Quantity</i> 1
<i>Data Sheet file</i> 1232.pdf	<i>Manufacturer</i> Dallas Semiconductor [Ref.24]	



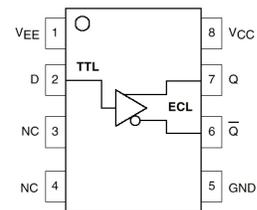
**6.8.23 MC10E211 - 1:6 Differential Clock Distribution Chip**

<i>Part Number</i> MC10E211FN	<i>Package</i> 28-Pin PLCC	
<i>PC Board Reference</i> U50, U51, U52, U53 [Ref.36].		<i>Quantity</i> 4
<i>Data Sheet file</i> mc10e211rev3a.pdf	<i>Manufacturer</i> Motorola [Ref.26].	



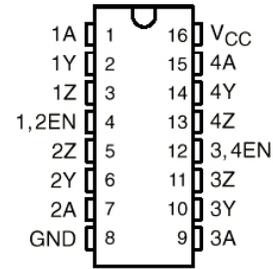
**6.8.24 MC10ELT24 - TTL to Differential ECL Translator**

<i>Part Number</i> MC10ELT24FN	<i>Package</i> 8-Pin SOIC	
<i>PC Board Reference</i> U12, U18, U44 [Ref.36].		<i>Quantity</i> 3
<i>Data Sheet file</i> mc10elt24rev2b.pdf	<i>Manufacturer</i> Motorola [Ref.26].	



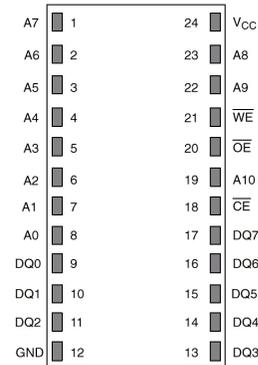
**6.8.25 SN75174 – Quadruple Differential Line Driver**

<i>Part Number</i> SN75174N	<i>Package</i> 16-Pin 300 mil Dip
<i>PC Board Reference</i> U1 [Ref.36].	<i>Quantity</i> 1
<i>Data Sheet file</i> slls039b.pdf	<i>Manufacturer</i> Texas Instruments [Ref.19]



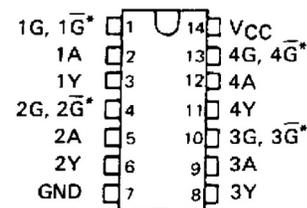
**6.8.26 DS1220 - 16K Nonvolatile SRAM**

<i>Part Number</i> DS1220AB-150	<i>Package</i> 24-Pin 600 mil Dip
<i>PC Board Reference</i> U45 [Ref.36].	<i>Quantity</i> 1
<i>Data Sheet file</i> 1220abad.pdf	<i>Manufacturer</i> Dallas Semiconductor [Ref.24].



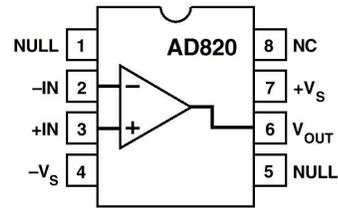
**6.8.27 74LS125- Quadruple Bus Buffers with 3-State Outputs**

<i>Part Number</i> 74125	<i>Package</i> 14-Pin 300 mil Dip
<i>PC Board Reference</i> U35 [Ref.36].	<i>Quantity</i> 1
<i>Data Sheet file</i> sdls044.pdf	<i>Manufacturer</i> Texas Instruments [Ref.19].



**6.8.28 AD820 – Single Supply, Rail to Rail Low Power FET-Input Op Amp**

<i>Part Number</i> AD820AN	<i>Package</i> 8-Pin 300 mil Dip
<i>PC Board Reference</i> U24 [Ref.36].	<i>Quantity</i> 1
<i>Data Sheet file</i> AD820.pdf	<i>Manufacturer</i> Analog Devices [Ref.20].



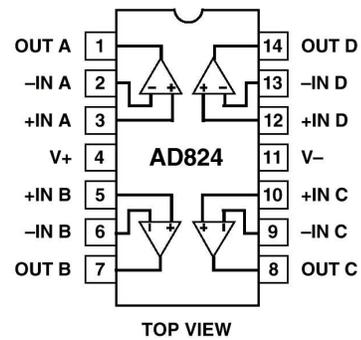
**6.8.29 LM35 - Precision Centigrade Temperature Sensor**

<i>Part Number</i> LM35CA	<i>Package</i> TO- 92
<i>PC Board Reference</i> LM35CA [Ref.36].	<i>Quantity</i> TO- 92
<i>Data Sheet file</i> LM35A.pdf	<i>Manufacturer</i> National Semiconductor [Ref.18]



**6.8.30 AD824 – Single Supply, Rail to Rail Low Power FET-Input Op Amp**

<i>Part Number</i> AD824AN	<i>Package</i> 14-Pin 300 mil Dip
<i>PC Board Reference</i> U25 [Ref.36].	<i>Quantity</i> 1
<i>Data Sheet file</i> 1810a.pdf	<i>Manufacturer</i> Analog Devices [Ref.20].



## 6.9 List of the hardware modifications to the original FIB Fanout Rev.B Design

The following is a list of the hardware modifications that have been done to the Fanout Rev.B original design. The modifications which involve changes in the schematic are reported in it.

### 1. Front Panel Modifications

- a) Enlarge (drill) the “Fiber Input” hole to 0.375 inches.
  - b) Enlarge (drill) the “Reset Out” hole to 0.344 inches.
  - c) Enlarge (drill) the “Scope Trig Out” hole to 0.344 inches.
  - d) Enlarge the hole for the “RS-485 Status” by filing the side near the solder-side of the board.
  - e) Enlarge the hole for the “Isp Loader” by filing it out so the mating connector will fit into the front panel.
2. Change surface mount resistors R107 and R108 (on solder-side of board) to 100 ohms
  3. Add a wire from U39-15 (Test Fifo) to jumper hole J72 which is connected to U28-58 (Fifo\_Ctl).
  4. Remove Zero ohm resistor R1.
  5. Add clear shrink wrap tubing over the barrels of the two Lemo connectors (Lemo1 and Lemo2) at the front panel of the board.
  6. Unsolder and remove U8 from the PC Board, cut the trace from U8-1 to the via it connects to, replace U8 on the PC Board and add a wire from U8-1 to the ground side (-) of C7.
  7. None
  8. None
  9. Carefully scratch off the G-Link Jumper labels on the PC Board silkscreen as they are opposite of what they really are.
  10. Unsolder pin #14 of U39 and U40 and then cut it so there is no longer a connection.
  11. Remove pin #1 of logic analyzer connector J139.
  12. Install a jumper wire (resistor lead) at position J54 between “Common” and “/Ispen”.
  13. Remove solder from holes at locations JP1 and JP2 along with row in between.
  14. Install jumper wire (resistor lead) at location JP2 Pin #2 to hole just above and at location JP2 Pin #3 to hole just above.
  15. Remove the fuse at location F3 (J3 Power) and replace it with a 2-Amp fuse. Carefully scratch the “5” off the silkscreen under the fuse.
  16. Install a 53Mhz oscillator at location Y1.
  17. Add modified front panel mount with bottom screw only.
  18. Remove resistor at location R45 and install a Zero ohm resistor.
  19. Remove resistor at location R42 and install a 430 ohm resistor.
  20. Remove potentiometer R44 and install a 10 ohm 10-turn potentiometer.
  21. Install a 75 ohm resistor at location R43.
  22. Remove capacitor at location C7, remove capacitor at location C6 and install the capacitor from location C7 (2.2uF). Leave location C7 open.
  23. Remove solder from holes at locations J137 and J138 and install a jumper wire (resistor lead) at this location.
  24. Add G-Link guide rails and RTV them to the board.
  25. Add a wire from U17-9 to U20-20 and add a wire from U20-23 to J50 (of U28).
  26. Place kapton tape on the edges of the top and bottom trace layers of the FINISAR G-LINK Receiver card to cover any traces that could possibly short to the aluminum guide rails on FFO if the soldermask got scratched off.

27. Solder the tabs of the 2 voltage regulators (U23, U41) to the copper area under them on the circuit board.
28. None.
29. Adjust R44 so that VBB is equal to  $-1.28\text{V}$ .
30. None.
31. Remove R24 (100K ohm) and replace with a 250K ohm.
32. Remove U24 and install an AD820AN.
33. Adjust R46 to give  $0.640\text{V}$  at U29-6. (5/21/99)
34. Install "capacitor boards" at locations U46, U47 and U48.
35. Install sip termination for ECL clock lines at locations RN6, RN7, RN8, RN9, RN10 and RN11.
36. Install module stiffener at rear of board over connectors.
37. Add a piece of 26 gauge wire to J3 connector to add the additional grounds to match the new Fib subrack J3 Backplane.
38. Place PREP serial number tag for front panel.
39. Tack wires to board using Loctite adhesive.
40. Install front panel.
41. ---Optional---Remove silk screen "do not install" below R43.
42. Remove U27 (74F08 or 74AS1008) and replace with a socket and a 74AS00. (6/16/99)
43. Remove U30, cut the trace (DB21) between Pin-6 and the via that it connects to and then resolder U30 back on the board. Add a wire between U30 Pin-6 and U56-14. Reprogram the VME Interface with code dated 06/16/99 or later.
44. Remove U25 and replace with a socket and an AD824AN.
45. Add module keying to front panel.
46. Add J3 connector solder-side shields.
47. Remove U60 and U61 and replace with 74ABT861PWDH (Phillips)
48. Add a wire from U31-7 (Error FIFO, Almost full flag) to J67 (connected to U28-70, FIFO Control)
49. Add a wire from U32-23 (Error FIFO, DB23) to J59 (connected to U28-47, FIFO Control)
50. Cut trace going to U34-21 (Error FIFO, DB29) near the via by GND test point J60.
51. Cut trace to U34-6 (Error FIFO) and add a wire from Pin-6 of U34 to J62 (connected to U26-69, Error Latch, FIB Error)
52. Cut trace to U34-5 (Error FIFO) and add a wire from Pin-5 of U34 to U26-37 (Error Latch, Optical Power Low)
53. Cut the following pins: U31-14, U32-14 and U33-14 (EFEF)
54. Cut the following pins: U31-15, U32-15 and U33-15 (EFFF)
55. Unsolder and remove U39 from the PC Board, cut the trace from U39-19 to the via it connects to, replace U39 on the PC Board. (need ISP code of August 27 or later).
56. Short J90 and J91 (needs ISP code of September 2 1999 or later).
56. Short J93 and J104 (needs ISP code of September 3 1999 or later).
57. To change the "VEE too low" and "VEE too high" error levels to more reasonable levels 3 resistors need to be changed.  $R27 = 78.7$  ohms,  $R30 = 95.3$  ohms and  $R31 = 10$  ohms (Note that the resistors have a 1% tolerance). This will set the error set levels equal to: "VEE too low" =  $-5.43\text{V}$  and "VEE too high" =  $-4.89\text{V}$  (Reference MISC page of schematic).
58. To tie the Shielded Data Link shield to the front panel follow this procedure: Carefully remove the serial number sticker covering center mount hole (with an Exacto knife) and center punch the mount. Remove the center mount and drill a  $0.070$ " hole (#50 drill) completely through it at the center punch marked spot and then tap it (both sides of center hole) with a 2-56 tap. Reinstall the center mount onto

- 
- the board and install a 2-56 x 0.250" taper head screw through the front panel. Install a solder lug with a star washer and screw to rear side of the mount. Solder a 26-gauge wire to the lug and to the mounting hole of "J1". Reinstall the serial number sticker (after removing existing adhesive) near the bottom of the front panel (Just above the "FFO" lettering) with "Permabond 910" or similar glue.
59. Trim any through hole component leads that are excessively long on back (solder-side) of the module.
  60. None.
  61. None.
  62. Lift U27-6, cut the pin. Connect a wire from the pad U27-6 to test point J55 (it goes to U28-7).
  63. Add a wire from U28-20 (FIFO Controller PLD, SAVE\_ERROR) to J48 (connected to U28-19, FIFO Controller PLD) (Reference FIFOS page of schematic).
  64. None.
  65. Check (using an ohm meter) that the signal /WRT\_MAP2 is not shorted to any other signal on the board. (For reference see MODULE HISTORY for boards numbered 108 & 110). November 04 1999.
  66. ~~Reprogram with ISP code dated November 11, 1999.~~  
Reprogram with ISP code dated November 10<sup>th</sup>, 2000.
  67. October 22 1999: Verify the board functionality referring the document "FIB Fanout Module Tests" document.

## Glossary

### **Fiber-Optic Interface Board (FIB) [Ref. 3]:**

Receive (through the FIB Transition Module) and process the data from 10 HDI links.

On an HDI the data rate is 26.5 Mbyte/sec.

The FIB is a 9U x 400 VME card that interfaces to a custom J3 Backplane and the J1 VMEbus Backplane. It is one of the modules designed to control and readout the SVX-III chips. The FIB interfaces with FIB Subrack Fanout Module over the custom J3 Backplane. The FIB Subrack Fanout Module receives timing and command information from the Silicon Readout Controller (SRC) from a dedicated Gigabit fiber-optic data link (G-Link). The FIB will be used to both control the SVX-III chips and to transfer data to the Level 2 data collection buffers known as VRB's (VMEbus Readout Buffers).

### **Command Flow:**

The following is the flow of commands and clocks from the SRC to the SVX-III chips.

- The SRC sends a 53 MHz clock (Master Clock), timing signals, and commands to the FIB Subrack Fanout Module via a dedicated G-Link fiber.
- The FIB Subrack Fanout Module distributes the 53 MHz clock and SRC commands through the J3 Backplane to the FIB modules.
- The FIB interprets the commands from the SRC and sends the SVX-III clocks (FE\_CLK, BE\_CLK, L1A), the Control Clock (C\_CLK) and the encoded control information (C [3:0]) to the PC (Portcard) using low voltage differential signal levels. Note these drivers are on the FIB/PC transition module.
- The PC controller interprets the encoded control information using the Control Clock (C\_CLK) and delivers the proper CMOS logical levels to the SVX-III chips through the HDI.

The clock sequences for the SVX-III chips are generated directly by the FIB. These clocks are fanned out by the PC to the five HDIs.

### **Data Flow:**

The data flow from the SVX-III chips travels via the following path:

- SVX-III chips transmit the data to the PC through the HDI using CMOS levels (single ended).
- The PC converts these signals, places them on a parallel optical link, and transmits the data to the FIB through five 9-bit parallel optical links (8 bits of data and a Data Valid signal). Note: these receivers are on the FIB/PC transition module.
- The FIB module accepts data from ten of these HDI links.
- Data from the HDI is processed (header frames and End Of Records added) and then transferred to the Level 2 buffers (VMEbus Readout Buffer (VRB) modules) and Silicon Vertex Trigger (SVT) system buffers (FIFO).

**FIB Subrack [Ref. 3, 14]:**

Vipa Subrack that houses the FIBs.

There is a special J3 Backplane used by the System Controller to drive the buffer number for event readout and scan, and to monitor operational status.

**FIB Subrack Fanout Module:**

The FIB Fanout Module is a 9Ux400 VME card that resides in a Fiber Interface Board (FIB) subrack. The FIB Fanout interfaces to a custom J3 Backplane, the Silicon Readout Controller (SRC) module and the VMEbus Backplane. There is a single FIB Fanout module in slot 14 of each FIB subrack. The FIB Fanout module receives commands and timing signals from the SRC module on a G-Link and places them on the J3 Backplane for use by the FIBs. The VME master in the FIB subrack configures the FIB Fanout.

**G-Link (High Speed Optical Serial Connection) [Ref. 8, 9, 10, 11, 12]:****Master clock signals:**

The CDF Master Clock provides the Master clock signals to the SRC module. Four signals are used by the SRC to provide synchronization between the Tevatron accelerator and the SVX data acquisition system:

- **CDF Clock:** The CDF Master system clock (approximately 53.104 MHz) is synchronized to the Tevatron clock. The clock frequency will vary over a small range depending on the beam energy. The clock has a 50% duty cycle.
- **SYNC:** This clock is one seventh of the CDF clock or approximately 7.6 MHz. and has a 132 ns. period and 18.8 ns. duration. It indicates the possible presence of a proton-antiproton bunch crossing as only one out of seven cycles of the CDF clock is defined to contain particles. This clock is active high.
- **BX:** The bunch crossing clock has a 132 ns. or 396 ns. period depending on accelerator operating mode and position of bunch gaps. It tags the presence of a proton-antiproton bunch crossing. This clock is active high with a 18.8 ns. duration.
- **BZ:** The bunch zero clock has a duration of 18.8 ns. and occurs once every revolution of the beam in the ring or at almost a 21 microsecond period. This clock is active high.

**Silicon Read-out Controller module (SRC) [Ref. 1]:**

The Silicon Read-out Controller is the controller for SVX. It is a D32 VME (9U x 400 mm VME card format) slave module that mediates upper level commands from the Trigger Supervisor Interface (TSI) to the Fiber Interface Board and VRB, compiles and reports readout status from the VRB to the TSI and passes the timing signals from the Master Clock to the FIB and VRB modules.

SRC to TS Commands (on a copper link):

- **DONE** (LVDS active high ): indicates that a level 2 accepted buffer transfer has completed.
- **Wait** (LVDS active high): indicates the SRC cannot accept any more "accepts" because it is out of scan buffers in the VRB.
- **ERROR** (LVDS active high): indicates a catastrophic error condition in or sensed by the SRC.
- **RACK** (LVDS active high): indicates acknowledgment of a L2 reject.

**TAXI:**

Transparent Asynchronous Xmitter-Receiver Interface. This is the name of the communication protocol used by the Advanced Micro Devices (AMD) chip (am7968) used in the communication link between the Silicon Readout Controller (SRC) and the Trigger Supervisor (TS). Further information could be found at the AMD web site: <http://www.amd.com/>.

**Trigger Supervisor**

The Trigger Supervisor is the master of the readout controllers within the data acquisition system. It issues commands and analyzes the status of all the readout controllers and makes system level decisions.

TS to SRC Commands (on a fiber link):

The trigger supervisor sends two (9-bit) words every 132 ns. The control link between the TS and the SRC is implemented by means of the AMD Am7968-175 TAXI (Transparent Asynchronous Xmitter-Receiver Interface) chip set. TAXI chips provide a simple parallel interface through a high-speed (up to 175MHz) serial link while maintaining the data bandwidth required by the system.

**VME Bus ReadOut Buffer (VRB) [Ref. 2]:**

The VRB is a single-width 9U VME module that includes VME64 slave capability. The VME interface is used for module initialization, diagnostics and readout of accepted events. The VRB receives data via transition module data links, which are typically serial optical connections and communicates with the System Controller through the J3 Backplane. The VRB can accept input data at a combined rate of up to 600 Mbytes/sec on multiple channels. The output rate is limited by VME transfer speeds and by the number of VRB modules sharing the VME bus. To make optimum use of the module, a significant trigger rejection factor between input and output event rates is assumed. The VRB memory is partitionable allowing a trade-off between buffer size and number of buffers. The VRB module normally does not implement its own buffer management, this is delegated to the System Controller module. The main function of the VRB module is to provide Level 2 buffering for the SVX silicon readout system. A set of VRB modules resides in a VIPA subrack along with one System Controller or Controller Fanout Module. They communicate via a custom J3 Backplane used by the System Controller to drive the buffer number for event readout/scan and to monitor operational status. Data received on each link is stored in the buffer pointed to by the readout buffer number supplied by the System Controller.

For the SVX system, the events stored by the VRB are events that have been accepted by the Level 1 trigger and are waiting for a Level 2 accept or reject. For a reject, the buffer is re-used when the System Controller requests an over-write (i.e. re-uses the buffer number). Events that are accepted by the Level 2 trigger are accessed via the VME interface with the System Controller supplying the scan buffer number. Either of the VRB ports may be programmed to operate in FIFO mode. In this mode the readout and/or scan buffer numbers are incremented automatically. Buffer numbers supplied by the System Controller are ignored. Information normally supplied by the System Controller can also be provided through VME if the control traffic will not interfere with data transfer.

**VRB Subrack [Ref. 2, 14]:**

Vipa Subrack that houses the VRBs and SRCs. There is a special J3 Backplane used by the System Controller to drive the buffer number for event readout/scan and to monitor operational status.

**VRB Fanout Module [Ref. 2, 14]:**

The VRB Fanout Module is a single-width 9U VME module. It resides in slot 14 of an SVX VRB subrack and translates differential PECL signals on the cable to TTL signals on the J3 Backplane. There are three groups of signals: a control bus that is used by the System Controller to send commands to the VRBs, a status bus used by the VRBs to signal completion of event readout and various error conditions.

### 6.10 Block Diagram of the SVX Data Acquisition System

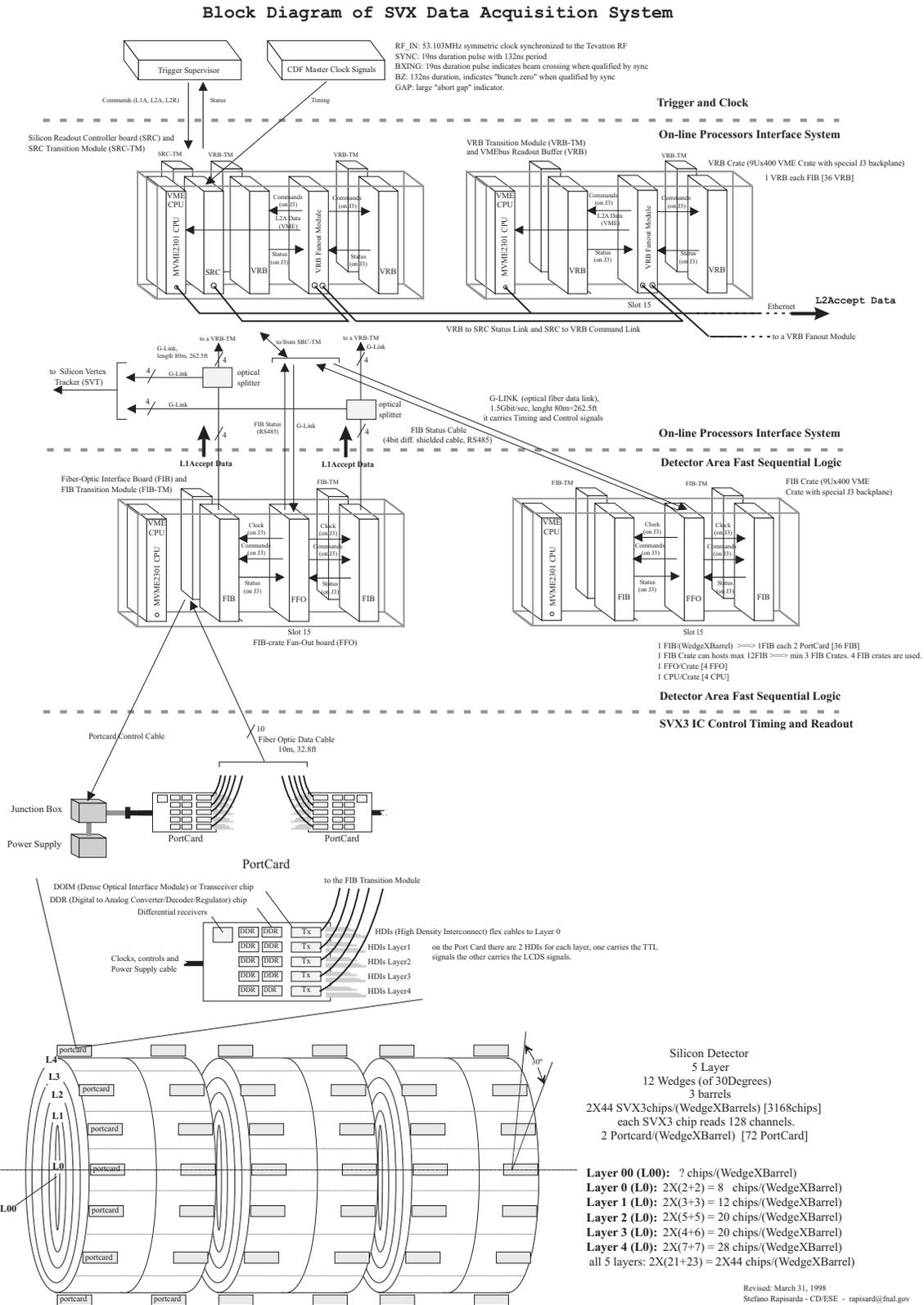


Figure 6.14, Block diagram of SVX DAQ system.

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