

**Fermi National Accelerator Laboratory**

## **SVX II Silicon Strip Detector Upgrade Project**

### **Transition Module for the Fiber Interface Board**

**4 March, 1998**

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**Document # ESE-SVX-960624**

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## 1 GENERAL INFORMATION

### 1.1 Introduction to the FIB\_TM

This document describes the Transition Module for the Fiber Optic Interface Board, hereafter referred as the FIB\_TM. This module is an interface adapter between the Port Card and the Fiber Optic Interface Board (FIB). The FIB controls and reads out SVX3 chips in the SVX II Upgrade Readout Electronics System. Multiple SVX3 chips are controlled by a Port Card. Each FIB transition module provides data signal reception from and control transmission to two Port Cards mounted on the Silicon Vertex (SVX) detector. The Silicon Vertex detector is a subsystem within the Collider Detector at Fermilab (CDF) project.

### 1.2 Description of the FIB\_TM and how it fits into the System

The FIB\_TM card is designed to operate mechanically as a VME transition card in a card slot directly behind the FIB and to electrically translate signal levels for the FIB. The FIB is a 9U X 400mm VME board that receives and process system commands from the Silicon Readout Controller (SRC) and passes encoded control information to the port cards within the SVX detector. The FIB also takes data from the Port Cards and transfers the data to the level two data collection buffers or VME Readout Buffers (VRB). There the data can be further processed over the VME bus as part of the data acquisition system. The FIB\_TM performs electrical signal translation for the FIB board of both received and transmitted signals. An additional benefit of this separation of circuitry is that the FIB can adapt to different versions of Port Cards as the development of the SVX chips and Port Cards continues. The FIB<sup>1</sup>, Port Card<sup>2</sup> and VRB<sup>3</sup> specifications are available as separate documents.

At this time, two versions of the FIB transition module exist. The first one was built while the DOIM fiber optic links were still under design. Early test stands were using copper cables to carry the data from the port card to the FIB subrack. Therefore, the first FIB\_TM is called the copper version or FIB\_TM\_CU. The production version is called the fiber optic module or FIB\_TM\_FO. The differences between these two versions will be highlighted as necessary through this document.

#### 1.2.1 Transmitter Functions

The FIB normally executes commands from the Silicon Readout Controller. It can also execute commands previously stored by the local VMEbus CPU inside the FIB Command FIFO or, also, some limited functions are available via selected bits of the FIB Control Register. Commands executed in the FIB are synchronous with the Port Cards (PCs) and SVX chips because the clocks for those devices come from the FIB. Two Port Cards are controlled by each FIB. The SVX-3 clock and command signals are: Front End clock (**FE\_CLK**), Back End clock

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<sup>1</sup> Fiber Interface Board Specification, Kerry Woodbury, Document #ESE-SVX-951010SVX

<sup>2</sup> Port Card for the SVX3 Chip, Andresen, Treptow & Zimmerman, Document #ESE\_SVX-950820

<sup>3</sup> VME Recording Buffer Specifications, Gonzalez, Mendoza, Bowden, Zmuda, Johnson & Barsotti, Document # ESE-SVX-950719

(**BE\_CLK**), Level 1 accept (**L1A**), Control clock (**C\_CLK**), the pipe read command (**PIPE\_RD2**) and the encoded control information (**C[5:0]**). One diagnostic clock called **T\_Clk** comes from the FIB to the transition module. There are also three buffered signals left over from the Intermediate Fiber Tracking (IFT) system design; **B\_MCLK**, **B\_AD\_PIPE** and **B\_SYNC**. All of these clock and control signals will pass from the FIB to the FIB\_TM board through the backplane P3 (P5/P6) connector. On the FIB\_TM board, the signals will be electrically translated to match the receivers of the current version of the Port Card.

### 1.2.2 Receiver Functions

The detector data will flow from the SVX-3 chips on the detector through the High Density Interconnect to the Port Card. Each Port Card takes data from five ladders, each containing from four to fourteen SVX-3 chips. The Port Card will place the data on five nine bit parallel optical links. These links will carry the data approximately 10 meters to the FIB racks where they will be received by fiber optic receivers on the FIB\_TM card. Each FIB\_TM board will take data from two Port Cards. Early versions of Port Cards will use copper data links until the high-density fiber links are available. The copper data links will be LVDS signals on small-pitch ribbon cable.

The data signals go through several layers of translation and buffers between the port card and the FIB. The signals were found to have too much skew to allow the FIB input circuitry to reliably extract the data from the data stream. The FIB\_TM now has circuitry to register the data right out of the fiber optic receivers. This logic creates a clock from the edges from the Odd Byte Data Valid (OBDV) signal and uses that to clock the data bits in the FIB\_TM latches. Only after that are the data converted from ECL to TTL signal levels and passed to the FIB.

## 1.3 Description of Component Requirements

The FIB\_TM module must mount in the transition card cage of an SVX VME chassis. It will be a 9U by 120-mm board. The FIB\_TM module is a signal level translator and is not concerned with signal content. Power is supplied through the VME P0 connector.

### 1.3.1 Requirements for the Transmitter Section

The signals from the FIB into the FIB\_TM will be TTL. The FIB\_TM must translate these signals into Low Current Differential Signaling (LCDS<sup>4</sup>) for the Port Card. The delays added to the signals must be consistent between signals and over time to avoid phase errors in the transmitted information. Development versions of the Port Cards will require translation to Low Voltage Differential Signaling (LVDS) output signals.

### 1.3.2 Requirements for the Receiver Section

The data from the Port Cards will be carried on five nine-bit fiber optic links utilizing Dense Optical Interface Modules (DOIM). The DOIM receiver outputs will be PECL signals.

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<sup>4</sup> Low Current Differential Signals, Barsotti & Zimmerman, Document #ESE\_SVX-950605.

These will be translated to TTL on the FIB\_TM and passed to the FIB through P3 (P5/P6). Development versions of the Port Cards will transmit data at LVDS or LCDS signal levels.

## 2 THEORY OF OPERATION

### 2.1 Basic Features and Operation

The FIB Transition Module is a component of the detector system for the CDF SVX II upgrade. The FIB transition module will be the signal translator for the Fiber Interface Board and its connections to the Port Cards. Different versions of Port Cards with different signal protocols will require the FIB\_TM to have a flexible interface design at the connections to the Port Card. This will allow one version of the much more complicated FIB module to interface to many versions of Port Cards. The FIB to FIB\_TM to Port Card module connectivity relationships is represented in Figure 1. The signals are described in detail in the next two sections.

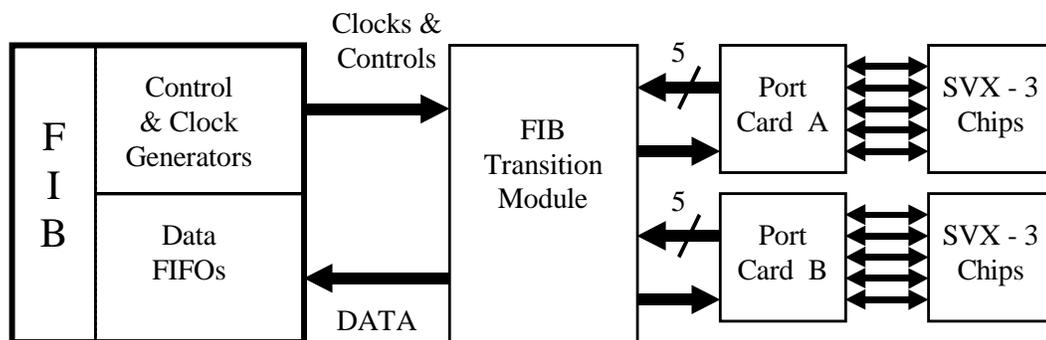


Figure 1 FIB\_TM connections.

#### 2.1.1 The Transmitted signals.

The transmitted clock and control signals are: **FE\_CLK**, **BE\_CLK**, **C\_CLK**, **C[5:0]**, **C\_Data**, **L1A**, and **PIPE\_RD2**. The generation of these signals is described in the FIB specifications. The signals will be TTL into the FIB\_TM and they will connect through the P3 (P5/P6) connectors. The following signal descriptions are summaries. The detail specifications of these signals can be found in the device specifications for the SVX3 chips<sup>5</sup> and the Port Card..

- The front end clock **FE\_CLK**. This 7.5 MHz (132-ns.) clock drives the analog front-end chip of the SVX3 readout chip set.
- The back end clock, **BE\_CLK**. This 53 MHz (19-ns.) clock drives the digital back-end chip of the SVX3 readout chip set.

<sup>5</sup> Device Specifications for the SVX3 Readout Chip Set, Strohmmer and Knopf, Document #ESE-SVX-950703.

- The command clock, **C\_CLK**. This 26.5 MHz (38-ns.) signal will clock the command bits **C[5:0]** into the DAC/Decoder/Regulator (DDR) chip on the Port Card to provide control of the SVX3 chips.
- The command bits **C[5:0]**. These bits are decoded by the DDR chip to produce the signals that control the SVX chips. These bits can change at a 26.5 MHz (38-ns.) rate. Details are in the Port Card specifications. The **C[5] bit** is only used by the prototype Discrete Port Card and not the production Compact Port Card.
- The control line **C\_Data** is the data bit containing the action that will be applied to the command decoded by **C[5:0]** in the DDR. The state of this bit controls changes of state or activity in the SVX3 chips. This is an input to DDR register bits addressed with **C** bits.
- The control line **L1A**, signals the trigger systems desire to keep the data cell from an event that is stored temporarily in the SVX3 chips set pipeline. The rate varies with the number of qualifying events.
- The control line **PIPE\_RD2** is a control line that put the most recently processed data cell back in to the pipeline so it is available for re-use.
- The diagnostic signal **T\_Clk** is a gated clock line that replaces the **OBDV** signal on the transition module during diagnostic tests of the **DDR**. This allows the registers on the transition module to appear transparent so that data bits from the **DDR** can be examined..
- There are three signals available on the P3 (P5/P6) backplane that were provided for use in the Intermediate Fiber Tracking system. These are **B\_MCLK**, **B\_AD\_PIPE** and **B\_SYNC**. Use of these signals would require a different version of transition module than the one described in this document.

### 2.1.2 The Received Signals.

The data from the Port Card will arrive on five high-density fiber optic ribbons as nine bit parallel data. The nine bits represent eight data bits and a data valid signal. There is an optical link for each of the five layers of silicon strip detectors. Layers will contain four, six, ten or fourteen SVX-3 chip sets because the layers are narrow near the beam pipe and wider away from it. One port card controls one wedge of five layers. A transition board is connected to two Port Cards so there will be ten optical link receivers on the FIB\_TM. The optical receiver outputs are PECL signal levels so the transition board will translate from PECL to TTL signal levels before passing the data to the FIB.

The copper versions of the FIB\_TM board will take in LVDS differential signals and translate these to TTL for the FIB. The connectors will be the high-density insulation displacement styles that allow 0.025-inch ribbon cable to replace the DOIM fiber optic ribbons.

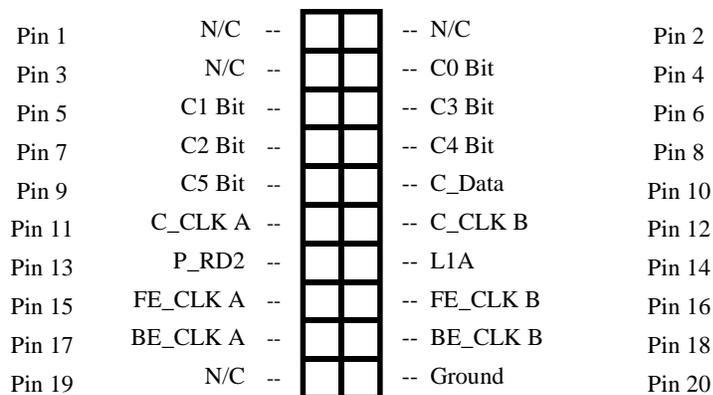
From the FIB and FIB\_TM module, the Port Cards are identified as port A or B. From the port card, the High Density Interconnect (HDI) from a layer into the port card are identified as HDI1 through 5. The port card data links (optical or copper) carry data bits D0-D7 and a data valid bit called Odd Byte Data Valid (OBDV). The data signals going into the FIB on P3 (P5/P6) are identified as HDI [A through J]. The mapping of signals follows from the following examples

- FIB HDI-A-D0 is Port Card A HDI1-D0
- FIB HDI-A-D1 is Port Card A HDI1-D1
- FIB HDI-B-D7 is Port Card A HDI2-D7
- FIB HDI-F-D0 is Port Card B HDI1-D0
- FIB HDI-J-OBDV is Port Card B HDI5-OBDV.

## 2.2 Diagnostic Features

There will not be any diagnostic displays on the FIB\_TM board beyond the LED indicating module power. Normal operation of the FIB\_TM module can not be determined other than by operation in a system or in a test stand. This board is most useful and easiest to test when it is plugged into a FIB. The diagnostic testing for the FIB should also test the FIB\_TM.

The FIB\_TM has a diagnostic connector accessible near the backplane on the board. Signals on the connector are diagrammed in **Figure 2**. The connector pin-out matches a standard Hewlett Packard logic analyzer pod connector.



**Figure 2 FIB\_TM\_FO Diagnostic Connector**

### **3 DIAGNOSTIC/DEVELOPMENT SOFTWARE**

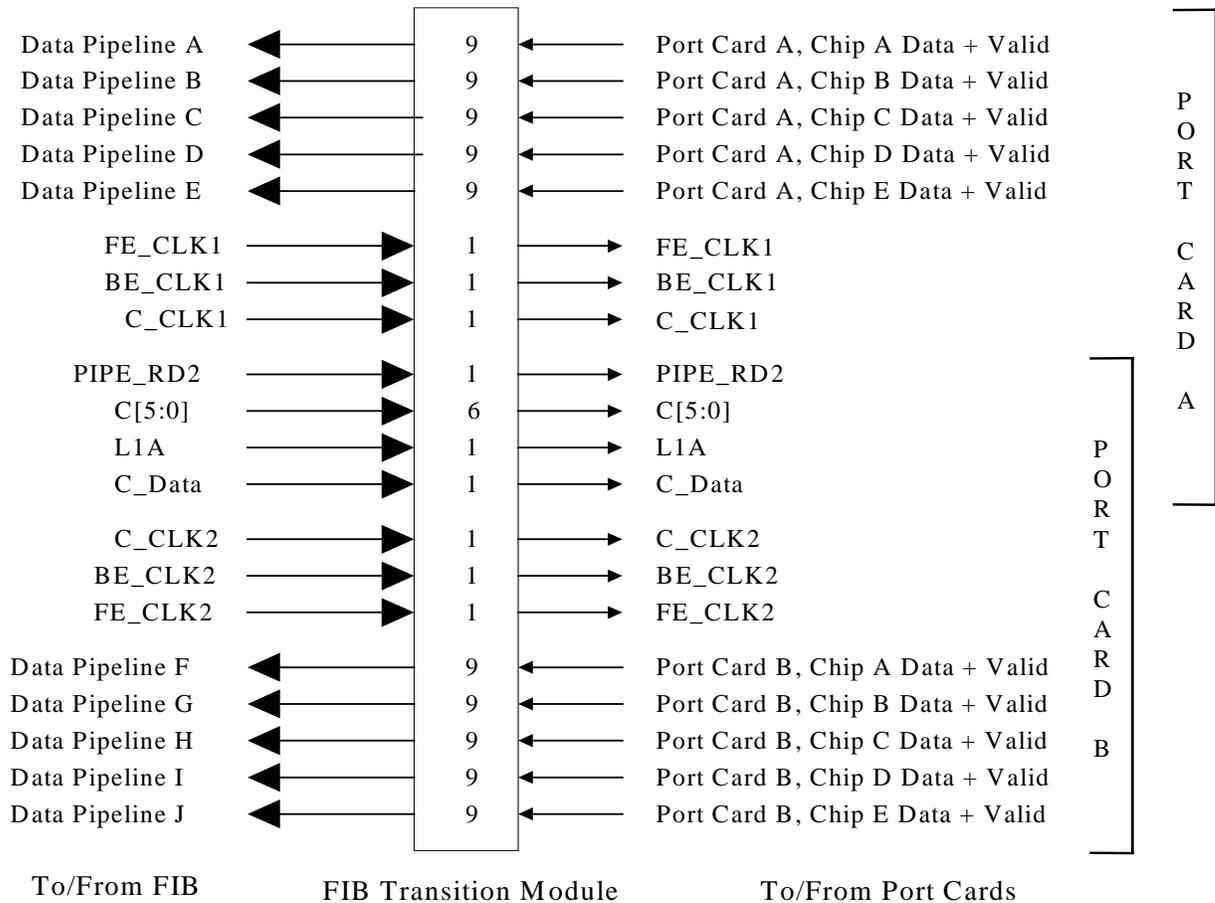
This board is most easily tested when it is plugged into a FIB so the diagnostic software for the FIB will also test the FIB\_TM. See the FIB manual for the description of this software.

## 4 INTERFACE SPECIFICATIONS

The FIB\_TM card occupies the transition module site behind a FIB board in a FIB subrack. There is a FIB\_TM for each FIB in the system. The two boards will exchange signals through the P3 (P5/P6) connector. The transition board will have VME-P hard metric seven row connectors mounted at sites P0 and P3 (P5/P6). The transition board will also have a VME64X seven row DIN connector mounted at site P2 to assist with vertical alignment during insertion and extraction. This should be a pinless shell.

### 4.1 FIB\_TM to FIB Interface - P3 (P5/P6)

The Fiber Interface Board communicates with the Port Cards through the FIB\_TM board. The signals pass through the VME backplane P3 (P5/P6) connectors. This is a 235-pin 2-mm hard metric connector. The block diagram, figure 2, shows the connections between the FIB and the FIB\_TM card for two Port Cards. The numbers shown within the transition module block are the quantity of bits for each signal. Note that nine control signals are shared.



**Figure 3 FIB to FIB\_TM to Port Card Signals**

**4.1.1 P3 (P5/P6) Connector Signal Descriptions**

The pin-out of the P3 (P5/P6) connector is shown below. The center row of pins is used as a custom backplane within the FIB chassis allowing communication between a module called a FIB Fanout Board and the FIBs in the subrack. There can be up to 12 FIBs in a subrack. The FIB\_TM board will not connect to any of these center-row pins. The outer four rows of pins are only straight-through pins at each card slot and are available for FIB to FIB\_TM communication. All of the connections that are used by the FIB\_TM are described in section 2.1.

## 4.1.2 P3 (P5/P6) Connector Pin Configuration

Table 1. P3 (P5/P6) Connector Pin Assignments

Pin #	Row 'a'	Row 'b'	Row 'c'	Row 'd'	Row 'e'
1	GND	GND	BUS1	GND	GND
2	B_MCLK	HDI-A-D0	BUS2	NC	HDI-B-D0
3	GND	HDI-A-D1	BUS3	GND	HDI-B-D1
4	B_AD_PIPE	HDI-A-D2	BUS4	NC	HDI-B-D2
5	GND	HDI-A-D3	BUS5	GND	HDI-B-D3
6	B_SYNC	HDI-A-D4	BUS6	NC	HDI-B-D4
7	GND	HDI-A-D5	BUS7	GND	HDI-B-D5
8	T_Clk	HDI-A-D6	BUS8	NC	HDI-B-D6
9	GND	HDI-A-D7	BUS9	GND	HDI-B-D7
10	NC	HDI-A-OB DV	BUS10	NC	HDI-B-OB DV
11	GND	HDI-C-D0	BUS11	GND	HDI-D-D0
12	NC	HDI-C-D1	BUS12	NC	HDI-D-D1
13	GND	HDI-C-D2	BUS13	GND	HDI-D-D2
14	NC	HDI-C-D3	BUS14	NC	HDI-D-D3
15	GND	HDI-C-D4	BUS15	GND	HDI-D-D4
16	NC	HDI-C-D5	BUS16	NC	HDI-D-D5
17	GND	HDI-C-D6	BUS17	GND	HDI-D-D6
18	C0	HDI-C-D7	BUS18	NC	HDI-D-D7
19	GND	HDI-C-OB DV	BUS19	GND	HDI-D-OB DV
20	C1	HDI-E-D0	BUS20	NC	HDI-F-D0
21	GND	HDI-E-D1	BUS21	GND	HDI-F-D1
22	C2	HDI-E-D2	BUS22	NC	HDI-F-D2
23	GND	HDI-E-D3	BUS23	GND	HDI-F-D3
24	C3	HDI-E-D4	BUS24	NC	HDI-F-D4
25	GND	HDI-E-D5	BUS25	GND	HDI-F-D5
26	C4	HDI-E-D6	RESERVED	NC	HDI-F-D6
27	GND	HDI-E-D7	SYNC(n)	GND	HDI-F-D7
28	C5	HDI-E-OB DV	/SYNC(n)	NC	HDI-F-OB DV
29	GND	HDI-G-D0	RESERVED	GND	HDI-H-D0
30	L_1/0	HDI-G-D1	MCLK(n)	NC	HDI-H-D1
31	GND	HDI-G-D2	/MCLK(n)	GND	HDI-H-D2
32	C_CLK1	HDI-G-D3	RESERVED	NC	HDI-H-D3
33	GND	HDI-G-D4	NC	GND	HDI-H-D4
34	C_CLK2	HDI-G-D5	NC	NC	HDI-H-D5
35	GND	HDI-G-D6	NC	GND	HDI-H-D6
36	PIPE_RD2	HDI-G-D7	NC	NC	HDI-H-D7
37	GND	HDI-G-OB DV	NC	GND	HDI-H-OB DV
38	L1A	HDI-I-D0	NC	NC	HDI-J-D0
39	GND	HDI-I-D1	NC	GND	HDI-J-D1
40	FE_CLK1	HDI-I-D2	NC	NC	HDI-J-D2
41	GND	HDI-I-D3	NC	GND	HDI-J-D3
42	FE_CLK2	HDI-I-D4	NC	NC	HDI-J-D4
43	GND	HDI-I-D5	NC	GND	HDI-J-D5
44	BE_CLK1	HDI-I-D6	NC	NC	HDI-J-D6
45	GND	HDI-I-D7	NC	GND	HDI-J-D7
46	BE_CLK2	HDI-I-OB DV	NC	NC	HDI-J-OB DV
47	GND	GND	NC	GND	GND

## 4.2 P0 Power Connector

The power for the FIB transition module will be supplied through the 96-pin 2-mm hard metric connector at P0. It is a female style to mate with the male style on the VME backplane. Only power connections will be made at this connector. Additional P0 details and specifications can be found in the FIB and VME-P specifications.

### 4.2.1 Power Connector Signal Descriptions

The power available to transition modules will come from assigned backplane pins. The FIB\_TM board needs only + 5 volts from the P0 backplane connector as the digital supply voltage. The total power dissipation should be approximately 14.5 watts. The total power dissipation on the FIB\_TM card is limited to 21 watts by the transition module specifications.

### 4.2.2 Power Connector Pin Configuration

List of P0 pin numbers for each voltage.

+5.0 volt pins - C1, D1, E1, C19, D19, E19.

Ground reference - all of row z and row f. (1-19)

## 4.3 Front Panel Area I/O

The front panel area will be at the back of the FIB subrack because this card is in the transition card area of the subrack. The bottom of the production (FIB\_TM\_FO) front panel will have a single SCSI II connector containing the control signals for both port cards. The cable will be split on the way to the port cards. The rest of the production front panel will have the ten fiber optic connectors. There will be one LED to indicate +5 volt power on the board. The front panel and front of the module are shown in Fig. 5.

The copper version (FIB\_TM\_CU) of the front panel will have board mount connectors for the copper data cables in approximately the same positions as the fiber optic data connectors. The order of the inputs will be the same as on the FIB\_TM\_FO module. The FIB\_TM\_CU control signal outputs are on a pair of sanded IDC style connectors in approximately the same position as the control connector on the FIB\_TM\_FO module.

### 4.3.1 Front Panel

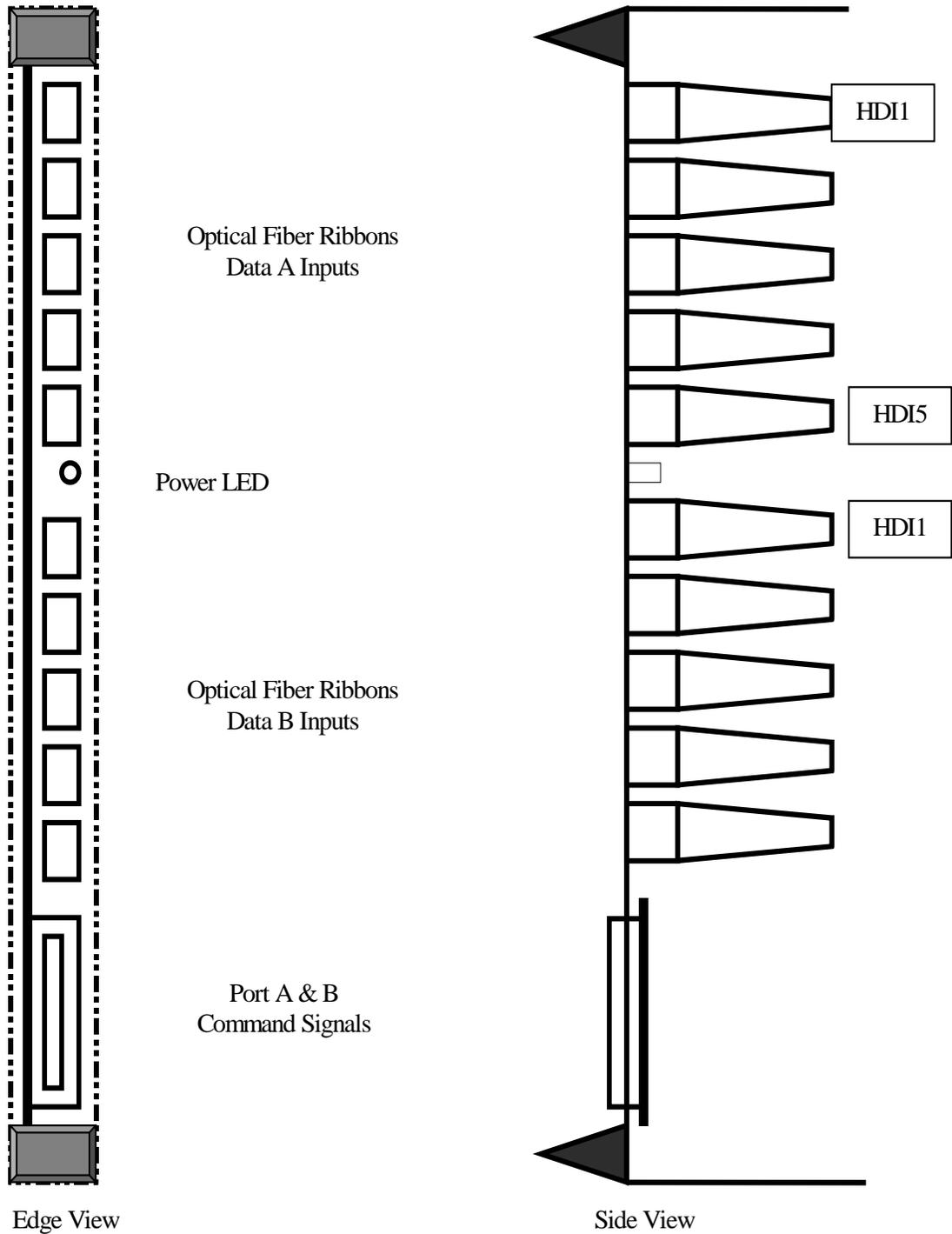


Figure 4 FIB\_TM Front Panel

### 4.3.2 Port Card Control Outputs

The Port Card output connector will be a 50-pin SCSI II style right-angle connector that is mounted to the transition card and accessible from the front. The part is an Amplimite .050 series subminiature D connector that uses 25 mil ribbon cables. The signal levels will be LCDS to match the Port Card.

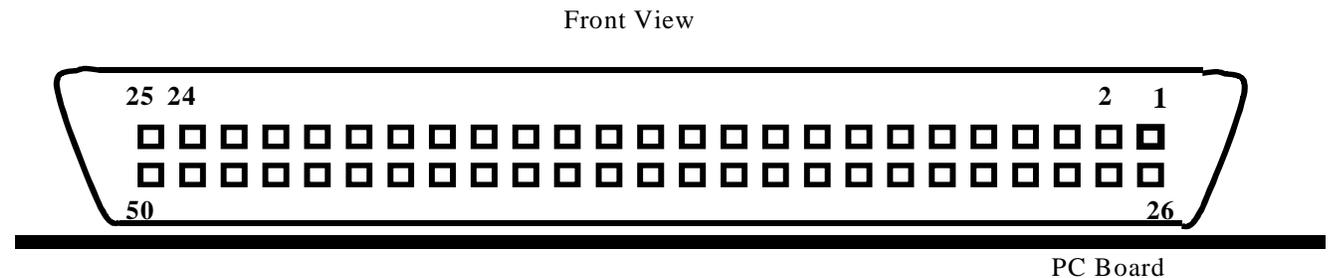
The copper version of this module has control cable connectors that are a pair of standard IDC style parts for 50 mil ribbon cables. A layout revision of the copper version of this module should update this part to the SCSI style connector that is on the fiber optic version of the board. The signal levels will be either LCDS or LVDS to match the version of the Port Card.

#### 4.3.2.1 Output Signal Descriptions

The outputs from the FIB\_TM\_FO board will control the SVX chips through the Port Card. The signals are described in Section 2.1.1. The signal level is LCDS.

#### 4.3.2.2 Output Connector Pin Configuration

For each Port Card, there are twelve signals transmitted differentially or twenty-four wires per port card. There is also a spare wire per card that can optionally be used for a reference ground connection. The total number of control wires out of the transition module equals fifty for the FIB\_TM\_FO. The connector pin-out is shown in **Figure 5**.



**Figure 5 FIB\_TM Control Signal Connector**

Signal pin assignments are detailed in the following table with the common abbreviations. The starred pins are the inverted outputs. The signals are arranged so that the signals for one port card are on the left and the signals for the other port card are on the right. Ground option pins separate the signal groups. In this way the cable can be split and provide the two identical cables necessary for the two port cards. One cable must be physically inverted before connecting to the junction box. Despite the odd numbering, the differential pairs are adjacent to each other in the cable and the signal order matches the signal order on the port card connector.

**Table 2 Control Pin Assignments – FIB\_TM\_FO**

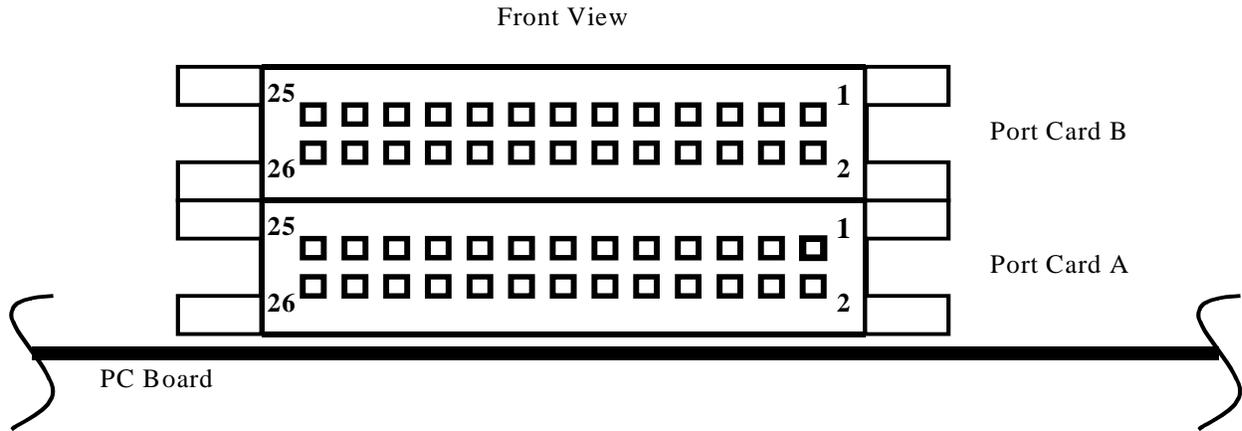
SIGNAL NAME	Port Card A	Port Card B
Front End Clock (FE_CLK)	1	50
Front End Clock* (FE_CLK*)	26	25
Command Clock (C_CLK)	2	49
Command Clock* (C_CLK*)	27	24
Command Data (C_Data)	3	48
Command Data* (C_Data*)	28	23
Command Bit #0 (C0)	4	47
Command Bit #0* (C0*)	29	22
Command Bit #1 (C1)	5	46
Command Bit #1* (C1*)	30	21
Command Bit #2 (C2)	6	45
Command Bit #2* (C2*)	31	20
Command Bit #3 (C3)	7	44
Command Bit #3* (C3*)	32	19
Command Bit #4 (C4)	8	43
Command Bit #4* (C4*)	33	18
Back End Clock (BE_CLK)	9	42
Back End Clock* (BE_CLK*)	34	17
Level 1 Accept (L1A)	10	41
Level 1 Accept* (L1A*)	35	16
Pipe_RD2	11	40
Pipe_RD2*	36	15
Command Bit #5 (C5)	12	39
Command Bit #5* (C5*)	37	14
Spare – Ground reference.	13	38

#### 4.3.2.3 Output Signal Descriptions

The outputs from the FIB\_TM\_CU board will control the SVX chips through the Port Card. The signals are described in Section 2.1.1. The signal levels are LVDS.

#### 4.3.2.4 Output Connector Pin Configuration

For each Port Card, there are twelve signals transmitted differentially or twenty-four wires per port card. There are also two spare wires per card that can optionally be used for a reference ground connection. The total number of control wires out of the transition module equals fifty-two for the FIB\_TM\_CU. The connector pin-out is shown in **Figure 6**.



**Figure 6. FIB\_TM Copper Control Signal Connector**

Signal pin assignments are detailed in the following **Table 3** with the common abbreviations. The starred pins are the inverted outputs. Despite the odd numbering, the differential pairs are adjacent to each other in the cable and the signal order matches the signal order on the port card connector.

**Table 3 Control Pin Assignments – FIB\_TM\_CU**

SIGNAL NAME	Port Card A or B
Front End Clock (FE_CLK)	2
Front End Clock* (FE_CLK*)	1
Command Clock (C_CLK)	4
Command Clock* (C_CLK*)	3
Command Data (C_Data)	6
Command Data* (C_Data*)	5
Command Bit #0 (C0)	8
Command Bit #0* (C0*)	7
Command Bit #1 (C1)	10
Command Bit #1* (C1*)	9
Command Bit #2 (C2)	12
Command Bit #2* (C2*)	11
Command Bit #3 (C3)	14
Command Bit #3* (C3*)	13
Command Bit #4 (C4)	16
Command Bit #4* (C4*)	15
Back End Clock (BE_CLK)	18

Back End Clock* (BE_CLK*)	17
Level 1 Accept (L1A)	20
Level 1 Accept* (L1A*)	19
Pipe_RD2	22
Pipe_RD2*	21
Command Bit #5 (C5)	24
Command Bit #5* (C5*)	23
Spare – Ground reference	26
Spare – Ground reference.	25

### 4.3.3 Port Card Data Inputs

There will be eight data bits, D0-D7, and a data valid line, OBDV, to be used to latch the data. These will be optical signals in the production system but the prototype system will need to use copper cables carrying LVDS signals. Both are described below.

#### 4.3.3.1 Fiber Optic Data Input Signal Description

The DOIM receiver parts will have 30-centimeter fiber optic pigtailed that are ribbons of 10 fibers. These will be terminated by panel mount optical fiber ribbon connectors inserted into the front panel adapters.

#### 4.3.3.2 Fiber Optic Input Connector Configuration

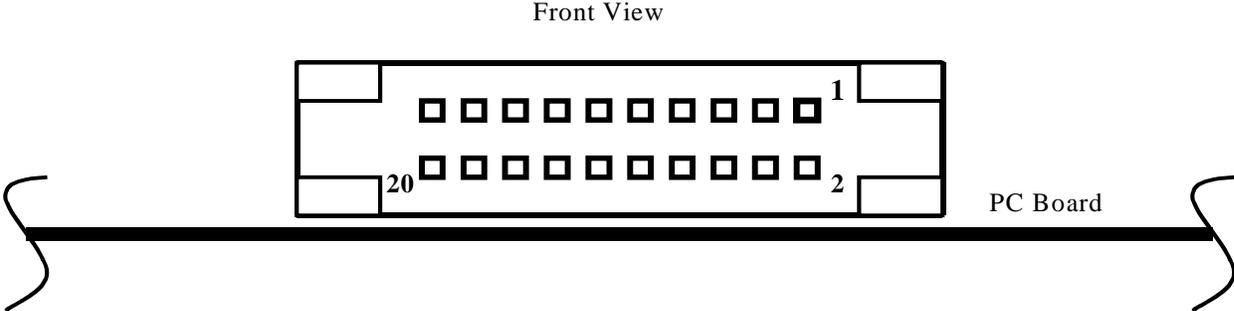
The data connector is a bulkhead version of an MTP optical fiber ribbon connector. The connectors are keyed by the front panel adapter so the orientation is correct. Molex and USConec make versions of this connector.

#### 4.3.3.3 Copper Cable Data Input Signal Description

For the copper version of the FIB\_TM, the data signals will be differential and either LVDS or LCDS depending on the port card.

#### 4.3.3.1 Copper Cable Data Input Connector Pin Configuration

The connector is a 3M Tripolarized header used with wiremount insulation-displacement sockets and 0.025-inch ribbon cable. The ten data input connectors are accessible at the front panel. Channel number one from port card A is at the top. The sixth connector down is channel number one from port card B. The pin out for each connector is shown in **Figure 7**.



**Figure 7. FIB\_TM Copper Data Signal Connector**

## **5 ELECTRICAL, MECHANICAL and SAFETY SPECIFICATIONS**

### **5.1 Packaging & Physical Size**

The board is a transition module that plugs into the transition card cage of a detector area FIB VME subrack. The dimensions of the card are 120-mm wide and 367-mm (9U) high. The electrical connections to the VME backplane are DIN style VME64X and 2-mm Hard Metric connectors as described in the VME-P specifications. Connections to interface cables are right angle mounted on the circuit board edge away from the backplane and accessible through the front panel when the board is inserted into a chassis.

Modules should conform to the VME64 Extensions Specification (VITA 1.1-199X) and VME64 Extensions for Physics (VITA 23-199X) in most areas including:

- This module will have front panel ESD gaskets and extractor/injector handles.
- This will be an inline module with no connection to VME bus signals.
- Mechanical and electrical connections will use P0, P2 and P3 (P5/P6). Transition modules are not allowed to connect to P1. The FIB subrack has a standard VME64X backplane covering the P0, P1 and P2 positions. The P3 (P5/P6) position is provided by a custom backplane with no power pins. Each P3 (P5/P6) position will have 235 pins. The P0 connection is used for power only.

### **5.2 PC Board Construction**

PC board construction techniques for high-speed logic should be used on this board. The fiber receiver to latch/translator chip connections should be as short as possible. On a per-channel basis, all the data signals should route through equal length traces. All chip power connections should be filtered and sufficient bulk filter capacitors distributed around the board.

### **5.3 Power Requirements**

The board requires +5 volts at four amps. The transition module should operate comfortably below the maximum allowed power dissipation of 21 watts. Major sources of heat, such as the termination voltage regulators, will have heat sinks applied.

### **5.4 Cooling Requirements**

The cooling requirements will be supplied by the VME chassis within which the board will normally operate. Test stands will have ambient forced-air cooling and the FIB detector racks will have heat exchangers with forced air cooling between the subracks. There is more information in the VME-P documents.

### **5.5 Connector Requirements**

The fiber optic receivers must be mounted on the transition module such that the optical ribbon makes an unimpaird 180-degree turn within the module with a straight exit from the board. The ribbon should be constrained so that the fiber is not repeatedly flexed, both on the module and within the rack. The Port Card command cable connectors should have a locking mechanism to secure the cable connector from unintended disconnection.

## **5.6 Module Fusing & Transient Suppression**

The +5 volt 'VCC' power supply connections will be fused at the transition board connector P0 such that all the board power passes through the fuses. On the transition board, all the power supply lines are protected with transient protection (transorb diodes) close to the fuses. Following that there will be high frequency ferrite in-line filters and the bulk capacitor filters. There will be low ESR filter capacitors at each digital integrated circuit and distributed around the printed circuit board.