

Fermi National Accelerator Laboratory

**SVX II Silicon Strip Detector Upgrade Project
Readout Electronics**

FIB CRATE FANOUT MODULE

--PRELIMINARY--

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Revision History

August, 1996

- Significant rewrite from original version.

September 4, 1996

1. Changed date and author list on title page.
2. Removed “Generate a VME crate reset on command from the SRC” from section 1.3, List of Component Requirements. Note that logic on the board allows for future re-inclusion of this feature at a later date.
3. Fixed missing arrow on Figure 2, block diagram.
4. Removed SYNC signal from bit 19 of TTL bus.
5. Re-ordered TTL bus such that only three bits of STAT_DATA are returned, on bits 23..21, as opposed to original four bits on bits 23..20 to allow use of only one 74F38 package on FIB as opposed to two. Bits 19 and 20, now unused, declared as RESERVED with option to tie to ground on Fanout. Tables 1 and 2 changed.
6. Added specific reference to GLINK as being source of STAT0 and STAT1 in section 2.2.1.
7. Rewrite of section 2.4.1 to provide more detail for reader, essentially pointing out where ancillary information needed for understanding is to be found. Highlighted ability of Fanout to provide individual control on a per-error basis of whether an error condition is Fatal or Non-Fatal.
8. Processor watchdog timer enable added to section 2.4.3 such that watchdog is disabled upon power up and must be explicitly enabled by VME write. Bit added to Fanout Configuration Register to accomplish this.
9. Pinout of J3 backplane connection changed as per request from George Wolf to simplify J3 backplane traces.
10. RC filtering network added to section 2.4.5 to filter out short-duration power glitches from POWER_OK sense line.
11. Section 4.1.1 changed to delete CR/CSR response and to delete block transfer response.
12. Section 4.1.2 changed, CR/CSR response deleted.
13. Section 4.1.3 deleted, save for description of derivation of module base address.
14. Section 4.1.4 rewritten. Relative address 0x0 changed to be Fanout Configuration Register and SVX module ID; all other registers shifted four bytes lower.
15. Section 4.2 deleted.
16. Section 4.3, with exception of Fanout Configuration Register, deleted. Fanout Configuration Register table moved to Section 4.1.4.
17. Figure 4 modified to put ST connector and LVDS link in middle of board.
18. J3 pinout table changed to remove GRT notation and to match new J3 backplane layout.

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2. THEORY OF OPERATION AND OPERATING MODES

The following sections describe in detail the operation of the FIB Fanout board.

2.1 Basic Features & Operation (Including Block Diagram)

The block diagram of the FIB Fanout is shown in Figure 2.

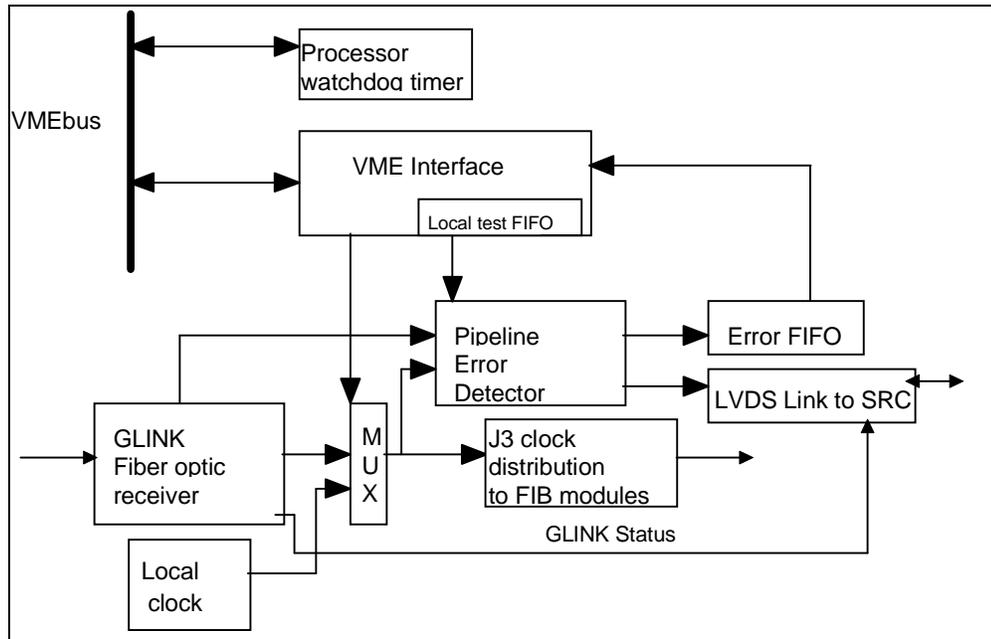


Figure 2

The FIB Fanout receives timing and control information from the SRC through an optical link. SRC timing information is conveyed by the optical link word clock itself, which runs at 53 Mhz and is the source of the MCLK signal. The rest of the SRC data is presented as a 20-bit word which is placed on the J3 backplane TTL bus for the FIB modules. In addition, the SYNC bit is extracted and driven over a separate differential ECL low-skew path to each FIB. Table 1 details the data format for the SRC data and how it maps to the TTL bus.

Bit #	Signal Name	Distribution Method
19	SYNC	Individual Differential ECL line per FIB
18	Pipe_RD2	TTL bus bit 18.
17..16	RDQ (<u>R</u> ead- <u>D</u> igitize- <u>Q</u> uirescent)	TTL bus bits 17..16
15..8	Bunch Crossing Number	TTL bus bits 15..8
7	Level 1 Accept	TTL bus bit 7
6	Advance_Pipeline	TTL bus bit 6
5	FIB XQT signal	TTL bus bit 5
4..0	FIB Command	TTL bus bits 4..0

Table 1 - SRC Signals

The FIB Fanout does not interpret any of the command bits in any way. All data is passed unchanged to the FIB as received. Determination of whether a command sequence is legitimate or rational is left to the FIB. Bits 24..20 of the TTL bus which connects the Fanout to the FIB are reserved for future use by the FIB to send acknowledgement or error information back to the Fanout. The Fanout assumes that the data presented upon these lines shall follow the format given in Table 2.

Bit #	Signal Name	Interpretation by Fanout
24	FIB_ERROR	Open-collector TTL signal indicating that one or more FIB modules have an error condition. Normally biased high, driven low by FIB upon error.
23..21	STAT_DATA	Three-bit status code from FIB, meaning TBD. Receivers on Fanout are biased such that data bits, if undriven, read 111 binary.
20..19	RESERVED	Unused TTL data bits. Optionally grounded by Fanout.

Table 2
Status Bits from FIB to Fanout

2.2 Initialization Sequence

The Fanout has two modes of operation, **Run** and **Initialize**. The device powers up in **Initialize** mode. In this mode, the user may, through software, read and write test patterns to the board, initiate a temperature conversion or probe the board for status information. While the board is in the **Initialize** mode, clocks to the FIB may be enabled or disabled in software, and if enabled, are derived from an internal oscillator. To use the Fanout, software must explicitly place

the board in to the **Run** mode by writing to a control register, or the Fanout must receive the RUN signal from the SRC over the LVDS link.

2.2.1 Initialization via the SRC

1. The SRC drives the RUN/INIT* line to INIT. The Fanout is driving MCLK and SYNC to the FIB via the internal oscillator.
2. The SRC starts sending fill frames to the GLINK. The Fanout returns the GLINK's STAT0 and STAT1 lines back to the SRC via the LVDS link.
3. The SRC determines that lock is achieved and starts sending data. The RUN/INIT* line is driven to RUN.
4. The Fanout receives the RUN signal, and uses this to initiate switching from the internal oscillator to the GLINK output. The Fanout first checks to insure that the GLINK is locked, then waits for the falling edge of the SYNC as seen on the local oscillator, at which time the internal oscillator is synchronously stopped.
5. The Fanout waits for the falling edge of the SYNC signal as received from the GLINK, and uses this to enable data from the GLINK synchronous with the GLINK clock. Commands, SYNC and MCLK resume to the FIB.

2.2.2 Initialization via other GLINK sources such as the GSTM

1. The Fanout powers up in INIT mode. MCLK and SYNC are driven from the internal oscillator.
2. The RUN signal is provided by software over the VMEbus.
3. The Fanout waits for the GLINK to indicate lock, then waits for the falling edge of SYNC as in step 3 in section 2.2.1 above. It is assumed the external device issues fill frames long enough for lock to be achieved; while this is occurring software may poll the GLINK's STAT0 and STAT1 lines via the Fanout's control registers.
4. Once lock is achieved, the Fanout automatically shifts over to the GLINK as described in steps 4 and 5 of Section 2.2.1.

2.3 Interface Descriptions

2.3.1 Physical interface from SRC to FIB Fanout

The SRC transmits all data to the FIB Fanout using a single optical fiber terminated in an ST connector. The FIB Fanout receives this data via a panel-mounted ST connector on the front panel of the Fanout, which is connected to a Finisar optical receiver module. The optical receiver drives a GLINK serial-to-parallel converter.

2.3.2 Physical interface from FIB Fanout back to SRC

Status data is returned from the FIB Fanout to the SRC via means of a four-bit cable. LVDS signals are sent differentially from the FIB Fanout to the SRC, with the meaning of the three bits of Fanout status controlled by the state of the bit driven from SRC to Fanout. A bias and termination scheme is assumed to exist within the SRC which allows the SRC to detect the presence or absence of the cable. Section 2.4.5 details the bias and termination scheme.

2.3.3 Physical interface from FIB Fanout to FIB

The FIB Fanout drives clock signals and commands to the FIB over a custom J3 backplane described in document #ESE-SVX-960130. Clock signals are driven via differential 10K ECLips lines, while commands and other information are carried on a terminated TTL bus. Power for the terminations of the TTL bus is provided by reserved pins and traces in the FIB Fanout. 10K ECLips pulldown and termination resistances are located within the FIB modules.

2.3.4 Physical interface from FIB back to FIB Fanout

No status or diagnostic information is sent from the FIB back to the FIB Fanout. Provision for later implementation of such a feature is present as the four-bit feedback bus described in Section 2.1 above. The Fanout samples the five bits described in Section 2.1 once every FIB command cycle (that is, once every seven GLINK frames) and saves the current state in a register which is accessible via VME. A control register in the Fanout allows the FIB_ERROR line to be optionally included in the generation of error status fed back to the SRC over the LVDS link.

2.4 Diagnostic Features

The Fanout provides diagnostic information regarding the validity of data transferred over the GLINK but does not duplicate protocol integrity checking already present in the FIB itself. The Fanout is capable of detecting the following error conditions:

- 1) Bit errors in any of the 20 data bits within an SRC frame. With the exception of the SYNC bit, all data bits should be repeated seven times. The Fanout uses a pipeline comparator to detect transitions within a frame.
- 2) Bit errors within the SYNC signal. In an SRC frame of seven GLINK data words, the SYNC is defined to be a '0' for the first five words, and a '1' in the last two. If this pattern is not found within an SRC frame, an error is detected.
- 3) Power failure of the -5.2 volt or +5.0 volt power supplies within the VME subrack. Failure of the -5.2 volt supply will result in an error trace available via VME data access and a direct indication to the SRC via cable; +5.0 volt supply failure may only be sensed via a direct indication to the SRC via cable, as failure of the +5.0 volt supply will disable the Fanout.
- 4) Out-of-range errors in the -5.2 volt and +5.0 volt power supplies. Voltage comparators and LEDs on the front panel of the Fanout provide visual indication of the power supply status.

2.4.1 Optical Link Data Error Detection

All 20 bits of GLINK data, previously described in section 2.1, enter a pipeline implemented in a Lattice in-system-programmable CPLD. The pipeline shifts with each GLINK clock (53 MHz), and a comparator is used to detect bit errors in the various bit fields of SRC data. Each of the eight bit field groups defined in Table 1 is sampled multiple times within a single SRC frame. Bit errors in any group create either Fatal or Non-Fatal error conditions. Each bit field group may be individually controlled as to whether a transmission error in the group is Fatal or Non-Fatal. The pipeline comparator is designed around a seven-word frame which is given in Figure 3:

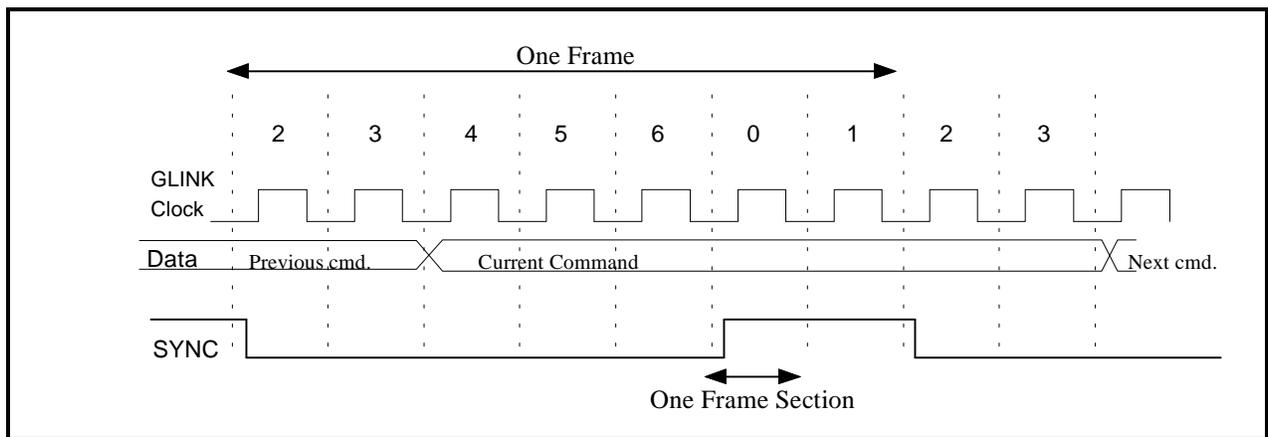


Figure 3

SRC GLINK Frame Structure

Data is entered in to the pipeline with every GLINK clock. The SYNC pulse (bit 19 of the data) is used to clock the output comparator. The second clock in which the SYNC is asserted (frame section 1) is used as the comparator result clock, resulting in the pipeline test looking backward at the data which was presented in frame sections 5, 6 & 0. The FIB latches the command in frame section 0, so the Fanout is sampling not only the data at the time the FIB uses it, but also in the frames immediately preceding.

Each group of data bits given in Table 1 is individually compared, allowing the Fanout to assign different levels of error severity to bit mismatches in different fields. The Fanout provides two different levels of error for data transmission:

- 1) Fatal Error. A Fatal Error is one which demands a Halt-Reset-Run sequence, as data is certain to be corrupt. Examples of Fatal Errors include SYNC errors or CMD errors. A Fatal Error is transmitted directly to the SRC over the FIB Fanout status cable so that appropriate action may be taken immediately.
- 2) Non-Fatal Error. A Non-Fatal Error is one which may create a Halt-Reset-Run sequence, but the decision of whether to do so may be deferred. An error has been saved to the Error FIFO, but the bit(s) in which the error has occurred are not critical

to FIB operation. An example of a Non-Fatal error is an error in the Bunch Crossing Number. Non-Fatal Errors are also transmitted directly to the SRC over the FIB Fanout status cable, allowing the SRC to determine whether a Halt-Reset-Run is required or whether simple tagging is sufficient.

The user programs the FIB Fanout Configuration Register to select which SRC fields create Fatal Errors and which create Non-Fatal errors. In addition to bit mismatches, other conditions such as power supply failure or receipt of the FIB_ERROR signal create Fatal Errors. Bits 0-7 of the Fanout Configuration Register, described later in Table 10, allow individual selection for each error condition of whether the error is deemed Fatal or Non-Fatal.

2.4.2 Sync Pulse Error Detection

A secondary pipeline is used to detect errors in the SYNC signal itself. A seven-bit shift register is implemented, which saves the state of the SYNC at every GLINK output clock. For any set of seven GLINK words, two and only two of the bits in the register may be asserted. Any other combination is indicative of a SYNC error, which is always a Fatal Error.

2.4.3 Processor Watchdog Timer

The Fanout implements a retriggerable monostable with a timeout period of 1 minute. The AS* signal on the VMEbus retriggers the monostable, whether the cycle is destined for the Fanout or any other board in the system. Should no VME activity occur for a full minute, the Fanout has the optional capability to assert SYSRESET*. Upon power-up the watchdog timer is disabled. To enable the watchdog timer, a bit in the Fanout Configuration Register must be set.

2.4.4 Internal Clock Generator for FIB testing

The General System Test Module (GSTM) is designed to provide test data inputs for all other SVX modules. However, some small facility within the Fanout that provides clocks for the FIB for in-situ testing is appropriate. To that end, the Fanout contains a Clock Generator that creates MCLK and SYNC signals at 53 MHz which may be enabled via a VME write cycle. A delay line is used to insure that the edges of the SYNC signal lead the edges of the MCLK signal to properly emulate the GLINK data output.

2.4.5 LVDS Error Feedback to SRC

A four-bit connector provides DC feedback from the Fanout to the SRC. This connector may be used by the SRC to directly monitor the state of the FIB subrack. The four bits provided are as follows:

- 1) RUN/INIT*. This bit is driven by the SRC and read by the Fanout. During system initialization, the SRC drives this line to a '0', indicating that the SRC is attempting to establish the fiber optic lock. Once the lock is established, the SRC then drives this line to a '1', informing the Fanout that data is now present on the GLINK and that the clocks and data should now be forwarded to the FIB. The Fanout biases the RUN/INIT* line to '0' such that a disconnected cable leaves the device in the **Initialize** mode.
- 2) POWER_OK. This bit is driven by the Fanout and received by the SRC. The Fanout drives this bit to a '1' if the power is OK. In the event of a power failure of the -5.2

- Volt supply, this bit is actively driven to a '0'. The SRC biases this line to a '1' at its receiver so that in the event of a +5.0 Volt failure, an error is also recorded.
- 3) STAT0/FATAL_ERROR. When the RUN/INIT* is a '0', this bit reflects the STAT0 status line of the GLINK. When RUN/INIT* is a '1', this bit is set to a '1' if the Fanout detects a Fatal Error condition. The SRC biases this line to a '1' in order to detect a disconnected cable.
 - 4) STAT1/NON-FATAL ERROR. When RUN/INIT* is a '0', this bit reflects the STAT1 status line of the GLINK. When RUN/INIT* is a '1', this bit is set to a '1' if a Non-fatal Error condition exists and no Fatal Error condition exists. The SRC biases this line to a '1' in order to detect a disconnected cable.

The bits of the LVDS link may be interpreted according to this table:

RUN/INIT*	POWER_OK	STAT0/ FATAL_ERROR	STAT1/ NON_FATAL_ERROR	Interpretation
0	0	X	X	Power failure in Fanout
0	1	GLINK STAT0	GLINK STAT1	GLINK initialization in progress
1	0	x	x	Power failure in Fanout
1	1	1	1	Cable disconnected
1	1	1	0	Fatal Error
1	1	0	1	Non-Fatal Error
1	1	0	0	Normal operation

The POWER_OK bit is heavily filtered on the Fanout such that momentary power surges or dropouts are not transmitted to the SRC. A power fail condition must be present for a minimum of 10 usec before the POWER_OK line will indicate the error.

2.4.6 Error Trace FIFO

A FIFO embedded within the programmable logic of the Fanout continually monitor the output data from the GLINK. Whenever the error detection circuitry detects that any form of data transfer error has occurred, a flag is set which will stop the FIFO after another 128 writes. This will leave a data trace in the FIFO where the error is in the middle with 128 words of history both prior to and following the error is recorded.

Once an error has been trapped by the FIFO, the FIFO is disabled until it is explicitly reset by a VME write. The entire error trace may be read out over VME at any time after the error has occurred. A bit in the Fanout Configuration Register allows software to force an error, causing the Error FIFO to act as a simple transaction capture memory.

Fanout errors are priority encoded such that higher value errors override lower value errors in the error FIFO. Thus, the highest priority error is a failure in the -5.2 volt supply, and the lowest priority error is a bit error in the bunch crossing number. Should multiple errors occur in the same frame, only the highest priority error is recorded for each word. The priority-encoded error code is stored for every word in the Error FIFO.

The FIB Fanout does not provide statistical analysis of errors detected, and does not in general have the ability to store information about more than one error. Should multiple errors occur within the sampling period of the Error FIFO they will all be recorded, but the FIFO is only guaranteed to hold information pertinent to the first error encountered.

2.4.7 Power Supply Monitoring Hardware

A dual voltage comparator circuit monitors the -5.2 volt and +5.0 volt power supplies in the subrack. A voltage reference diode is used as the basis for comparison. In the event that the +5.0 volt supply fails, the voltage comparator will cease to function. So long as the +5.0 volt supply is at least +3.0 volts, two window comparators are used to measure the -5.2 volt and +5.0 volt supplies. Each supply is allowed a $\pm 10\%$ variation before it is flagged as being in error.

The FIB Fanout assumes that -5.2 volts is presented to modules in the VIPA compatible subrack via the Vw, Vx and Vy pins of the J0 connector. The test of the -5.2 volt supply requires that current be drawn from all three pins such that if voltage is not present on any one of them the -5.2 volt supply is deemed to be in error. The FIB Fanout performs no tests of the Vz voltage, the +3.3 volt supply, the +12 volt supply, the -12 volt supply, $\pm V1$ or $\pm V2$.

2.4.8 Temperature Monitoring

An on-board temperature sensor allows software to remotely monitor the temperature in the FIB Fanout. The sensor automatically measures the temperature at fixed time intervals and histograms the temperatures seen in to an eight-bin histogram. Additionally, the same component provides a small amount of NVRAM which may be used for device tracking purposes.

2.4.8.1 On-board identification

A unique serial number is programmed in to each FIB Fanout along with a small non-volatile memory which allows software to uniquely identify each device for inventory tracking and update tracking purposes. 24 bytes of NVRAM are allocated for storage of update history data. These bytes are assigned as 12 16-bit words with the following format:

D[15..9]	D8	D[7..0]
date code	change code	modification number, in binary

Table 3
Format of NVRAM repair history memory

The seven-bit date code is an index value indicating the month during which the modification was applied. It is the number of months after January, 1997; thus, a module which is

returned for update in July of 1998 will have a date code of 18. The 128 values of the date code allow for recordkeeping over more than 10 years.

The change code provides an indicator of the type of function which has been performed on the device. The defined values are:

D7	Interpretation
0	Engineering Change Applied. Value in modification number field indicates change which has been applied.
1	Device cycled for repair. Value in modification number field is last two digits of Repair form serial number, for correlation with repair records.

Table 4
Interpretation of bit seven in NVRAM repair history memory

The user obtains access to this data by writing a bit to a control register which causes the Fanout to copy all identification data to a FIFO. A status bit indicates when all data has been downloaded. Identification data may only be read out of the Fanout when it is in the **Initialize** mode.

2.5 FIB Fanout response to error conditions during RUN mode

The FIB Fanout will, in addition to asserting the error condition on the LVDS link to the SRC and storing the error trace in the Error FIFO, halt the clock to the FIB upon the detection of any Fatal Error. The clock will be stopped at the end of a FIB command frame to insure a clean stop. Having halted the clock to the FIB, the Fanout is left in the **Initialize** mode and must be put back in to the **Run** mode either by VME write or a low-to-high transition on the RUN/INIT* line from the SRC. The status bits fed back from Fanout to SRC will continue to assert their RUN mode values until such time as the SRC drops the RUN/INIT* to '0'. At this point the lines monitor the GLINK status allowing the SRC to re-establish lock prior to restarting in RUN mode.

In the event of catastrophic failure, where the VME processor stops functioning, the Fanout's VME watchdog timer will at the end of one minute assert the SYSRESET* signal on the VMEbus, which should have the effect of reinitializing the FIB modules and rebooting the local processor. To insure that the VME processor may be restarted without requiring physical access to the processor board, a copy of the SYSRESET* generated by the Fanout is provided on the front panel as an optically isolated open-collector TTL signal. This reset pulse may be connected by a wire to the front panel reset input of the processor board.

3. DIAGNOSTIC/DEVELOPMENT SOFTWARE

This section is still quite draft. Software needs will be more formally analyzed as the design matures.

3.1 Development & Diagnostic Software

Diagnostic software for the FIB Fanout is minimal. The device implements few memory locations. The majority of tests may be accomplished using the VME Master's resident debug program plus an oscilloscope and/or logic analyzer.

3.1.1 Description Of Hardware Test Platform

To test the FIB Fanout, the following hardware is required:

- 1) VIPA subrack with power supplies
- 2) Any VMEbus processor plus a dumb terminal
- 3) Oscilloscope and/or logic analyzer
- 4) A FIB (to receive the signals sent by the Fanout)
- 5) A SRC and/or GSTM (to send optical data to the Fanout)

3.1.2 Description Of Software Test Platform

No new software test platform is required to test the FIB Fanout.

3.1.3 Software Tools & Methodologies

Minimal C software written under VxWorks will be used to test the FIB Fanout. It is expected that FIB test software will also access the Fanout.

3.1.4 Test Features

Basic I/O to the registers of the modules will be provided. In addition, the user may enable and disable the various error trap conditions within the Fanout.

4. VME INTERFACE SPECIFICATIONS

The FIB Fanout has a A32:D32 VMEbus slave interface. The FIB Fanout does not generate VMEbus errors or interrupts.

4.1.1 Addressing Modes

The FIB Fanout is an A32 VMEbus slave and responds to the following Address Modifiers:

AM Code	Function
0x0A	A32 Supervisory Data Access
0x09	A32 Non-Priviledged Data Access

Table 5 - VME Address Modifiers

4.1.2 Data Cycle Types

The FIB Fanout is an A32/D32 VME Slave. In accordance with SVX specifications no support of A24/Dxx, A32/D16 or A32/D08 transactions is provided.

4.1.3 CR/CSR Register Descriptions

The FIB Fanout has no CR or CSR locations.

4.1.4 Addressing

The FIB Fanout derives its base VME address from the Geographic Address pins of the subrack, if provided. If not Geographic Address pins are available, as determined by hardware in the Fanout, the base VME address is derived from DIP switches on the board.

4.1.5 Data Space Register Descriptions

The FIB Fanout provides five 32-bit wide register locations in Data Space as described in the following subsections.

4.1.5.1 Fanout Configuration Register: relative address 0x0000

Relative address 0x0 is the Fanout Configuration Register. In addition, this location provides module identification as per SVX system specifications. The entire bitmap of the Fanout Configuration Register is given in Table 7.

Bit #	Name	Read/Write interpretation
31..24	MODULE_ID	Upon read, the SVX ID of the Fanout. No effect upon write.
23	FORCE_RESET	Writing a 1 to this bit forces the FIB Fanout to create a SYSRESET* pulse. Needless to say, reading this bit after writing to it is impossible.
22	RUN_MODE	Writing a 1 to this bit sets the Fanout in to Run mode, identical to having received the RUN signal from the SRC.
21	CLOCK_SOURCE	When the module is in the Initialize mode, writing this bit to a 1 sets the clock source to the GLINK and writing a zero sets the clock source to the internal oscillator. Reading this bit at any time indicates where the clock is sourced. The power-up default is the internal oscillator.
20	RESET_EFIFO	Writing a 1 to this bit clears the Error FIFO.
19	RESET_GLINK	Writing a 1 to this bit resets the GLINK receiver.
18	SEND_FAKE_DATA	Writing a 1 to this bit causes the fake GLINK data previously loaded from VME to be issued through the system at full system speed. Once the FIFO of fake data is exhausted, the Fanout will continue to send MCLK and SYNC pulses, but all other data bits will be forced to zero. Reading this bit returns the status of the fake data FIFO empty flag.
17	FORCE_FATAL_ERR	Writing a 1 to this bit forces the FATAL_ERROR signal to be sent out the LVDS link, for test purposes.
16	FORCE_NONFATAL_ERR	Writing a 1 to this bit forces the NONFATAL_ERROR signal to be sent out the LVDS link, for test purposes
15	DALLAS_BUSY	This bit is 1 when data is being transferred into or out of the SPFIFO. When this bit is set the SPFIFO is not available to VME.
14..10	RESERVED	These bits are reserved for future use.
08	ENABLE_WATCHDOG	Writing a 1 to this bit enables the AS* watchdog timer.
07	Bunch Xing error map	Writing a 1 to each bit maps the error to a FATAL ERROR.
06	RDQ error map	Writing a 0 to each bit maps the error to a NON_FATAL ERROR.
05	CMD/XQT error map	Upon read, these bits are '1' if that error is currently present and '0' if the error is not present.
04	ADV_PIPE error map	
03	L1A error map	
02	PIPE_RD2 error map	
01	SYNC error map	
00	-5.2 volt fail error map	

Table 6
Configuration Register in FIB Fanout

4.1.5.2 GLINK/FIB Status Register: relative address 0x0004

Relative address 0x4 provides read access to the current GLINK data. It is intended for system commissioning purposes, where data is sent very slowly, allowing the processor to see each word as it is sent. As the GLINK data is only 20 bits wide, the remaining 12 bits are used to display FIB and GLINK status as given in Table 8. Writing to relative address 0x4 will allow VMEbus to enter fake GLINK data to a FIFO. The FIFO is filled by VME and then emptied at full speed by a write to a different control register at a later time. This FIFO may be tested by placing a fake data pattern into the FIFO, then sending it through the system and verifying that the same data appears in the Error Trace FIFO.

Bit	Meaning
31	FIB ERROR bit from FIBs
30,29,28	3-bit FIB STATUS from FIBs
27	CAV* status from GLINK
26	DAV* status from GLINK
25	LINKRDY* status from GLINK
24	FLAG status from GLINK
23	FF status from GLINK
22	ACTIVE status from GLINK
20,21	STAT1, STAT0 status from GLINK
19..0	20-bit data from GLINK

Table 7

GLINK/FIB Status Register bitmap (read cycles only)

Bit(s)	Meaning
31..24	Unimplemented for write
23..20	Writable, but have no function
19..0	Fake GLINK data

Table 8

GLINK/FIB Status Register bitmap (write cycles only)

4.1.5.3 Error Trace FIFO: Relative address 0x0008

Relative address 0x08 provides access to the Error FIFO, which provides a record of words preceding and following any data transmission error. The FIFO can only be read. It cannot be directly written from VME. To test the Error FIFO, a test data pattern must be placed within the Test FIFO and clocked through the system. Table 10 shows the format of data read from the Error FIFO.

Bits 31..24		Bits 23..20		Bits 19..0
GLINK Status Bits		Fanout Error Status (binary)		GLINK Data
bit 31	STAT0	0XXX	No error	
bit 30	STAT1	1000	Bunch Xing bit error	
bit 29	LINKRDY*	1001	RDQ bit error	
bit 28	FLAG	1010	CMD/XQT error	
bit 27	FF	1011	ADV_PIPE bit error	
bit 26	ERROR	1100	L1A bit error	
bit 25	DAV*	1101	PIPE_RD2 bit error	
bit 24	CAV*	1110	SYNC bit error	
		1111	-5.2 volt supply failed	

Table 9
Error Trace FIFO Data Format

4.1.6 Dallas Command Register: relative address 0x000C

Relative address 0x0C is the Dallas Command Register, where software loads the temperature/board signature access commands as described in section 3.1.5. When a command is written to this register, data transfer to or from the temperature/board signature device is initiated. The format of this register is given in Table 8. The lower 24 bits of this register are implemented as a shift register such that the commands loaded within are directly sent over the one-wire Dallas interface.

Bit #	Name	Read/Write interpretation
31..29	RESERVED	Not implemented.
28	READ/WRITE	1: Data transfer is from Dallas to SPFIFO. 0: Data transfer is from SPFIFO to Dallas.
27..26	FIFO_CTRL	When in sequence of commands data is transferred between Dallas 2435 and FIFO 0: FIFO first, then commands 1: After Command 1 2: After Command 2 3: After Command 3
25..24	NUM_CMD	number of commands in this sequence (0 not valid)
23..16	Command1	First Command given to Dallas 2435 part.
15..8	Command2	Second Command given to Dallas 2435 part (optional)
7..0	Command3	Third Command given to Dallas 2435 part. (optional)

Table 10

Dallas Command Register Bitmap

4.1.6.1 Serial/Parallel FIFO: relative address 0x0010

Relative address 0x10 provides access to the Serial/Parallel FIFO (SPFIFO) used for communication with the temperature/board signature device. When a write command is stored in the Dallas Command Register, data previously stored in this FIFO is transferred to the temperature/board signature module in locations controlled by the command. A write command transfers data until the SPFIFO is empty. When a read command is stored in the Dallas Command Register, data in one of the banks of Dallas 2435 registers is transferred to the SPFIFO. A read always transfers exactly 32 bytes of data from the Dallas to the SPFIFO. Not all locations read may be valid; the amount of valid data is dependent upon the command used.

Various commands may be stored within the Dallas Command Register in order to automate the access to the various data fields within the Dallas 2435.

4.1.6.2 Software notes on Dallas time/temperature interface

Table XXX below lists some of the more common interactions between the SPFIFO and the Dallas Command Register, to accomplish different system monitoring tasks.

Desired Action	Sequence of operations required
Read Board History Data	<ol style="list-style-type: none"> 1) Reset SPFIFO via write to Fanout Configuration Register. 2) Write 0x7111 to Dallas Command Register. 3) Poll DALLAS_BUSY bit in Fanout Configuration Register. 4) Read data from SPFIFO.
Write Board History Data	<ol style="list-style-type: none"> 1) Reset SPFIFO via write to Fanout Configuration Register. 2) Load SPFIFO with history data from VME. 3) Write 0x1722 to Dallas Command Register. 4) Wait for DALLAS_BUSY bit to clear before attempting any further access to Dallas 2435.
Read Temperature Data	<ol style="list-style-type: none"> 1) Reset SPFIFO via write to Fanout Configuration Register. 2) Write 0x1722 to Dallas Command Register. 3) Poll DALLAS_BUSY bit in Fanout Configuration Register. 4) Read data from SPFIFO.
Change Histogram Bins	Preload Histogram control data
	What to write to the Dallas Command Register
	0x1722

	0x00B2
	0x00EF

4.2 Front Panel I/O, Test & Monitoring

The FIB Fanout has one ST connector to receive G-Link data from the SRC and one ST connector to return the ERROR bit of the G-Link to the SRC.

The FIB Fanout has front panel LEDs to indicate when it is attached as a VMEbus slave, when the G-Link is ready, and a G-Link ERROR signal is active. Additional LEDs indicate the state of subrack +5.0 volt power, subrack -5.2 volt power and J3 backplane power.

A single LEMO connector provides a copy of the SYSRESET* pulse as an open-collector TTL signal for interface to the local subrack CPU board. An auxiliary 25-pin type 'D' connector allows front panel access to the internal ISP programming chain.

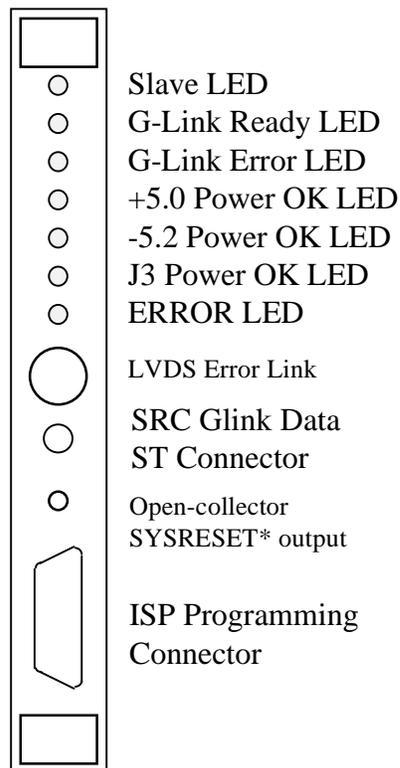


Figure 4 - FIB Fanout Front Panel

4.3 J3 Backplane Connector

The J3 connector is used to fanout clocks and commands received from the SRC to the FIBs. The J3 backplane has 13 slots with the FIB Fanout in the middle slot.

4.3.1 J3 Connector Pin Assignments

The pinout for the J3 connector is shown on the following page. The Fanout makes no connection to User I/O or RESERVED signals.

Pin #	Row 'z'	Row 'a'	Row 'b'	Row 'c'	Row 'd'	Row 'e'	Row 'f'
1	GND	USER I/O	MCLK9	BUS 1	SYNC9	USER I/O	GND
2	GND	USER I/O	/MCLK9	BUS 2	/SYNC9	USER I/O	GND
3	GND	USER I/O	MCLK10	BUS 3	SYNC10	USER I/O	GND
4	GND	USER I/O	/MCLK10	BUS 4	/SYNC10	USER I/O	GND
5	GND	USER I/O	MCLK11	BUS 5	SYNC11	USER I/O	GND
6	GND	USER I/O	/MCLK11	BUS 6	/SYNC11	USER I/O	GND
7	GND	USER I/O	MCLK12	BUS 7	SYNC12	USER I/O	GND
8	GND	USER I/O	/MCLK12	BUS 8	/SYNC12	USER I/O	GND
9	GND	USER I/O	MCLK13	BUS 9	SYNC13	USER I/O	GND
10	GND	USER I/O	/MCLK13	BUS 10	/SYNC13	USER I/O	GND
11	GND	USER I/O	MCLK14	BUS 11	SYNC14	USER I/O	GND
12	GND	USER I/O	/MCLK14	BUS 12	/SYNC14	USER I/O	GND
13	GND	USER I/O	MCLK21	BUS 13	SYNC21	USER I/O	GND
14	GND	USER I/O	/MCLK21	BUS 14	/SYNC21	USER I/O	GND
15	GND	USER I/O	MCLK20	BUS 15	SYNC20	USER I/O	GND
16	GND	USER I/O	/MCLK20	BUS 16	/SYNC20	USER I/O	GND
17	GND	USER I/O	MCLK19	BUS 17	SYNC19	USER I/O	GND
18	GND	USER I/O	/MCLK19	BUS 18	/SYNC19	USER I/O	GND
19	GND	USER I/O	MCLK18	BUS 19	SYNC18	USER I/O	GND
20	GND	USER I/O	/MCLK18	BUS 20	/SYNC18	USER I/O	GND
21	GND	USER I/O	MCLK17	BUS 21	SYNC17	USER I/O	GND
22	GND	USER I/O	/MCLK17	BUS 22	/SYNC17	USER I/O	GND
23	GND	USER I/O	MCLK16	BUS 23	SYNC16	USER I/O	GND
24	GND	USER I/O	/MCLK16	BUS 24	/SYNC16	USER I/O	GND
25	GND	USER I/O	USER I/O	BUS 25	USER I/O	USER I/O	GND
26	GND	USER I/O	USER I/O	GND	USER I/O	USER I/O	GND
27	GND	USER I/O	USER I/O	GND	USER I/O	USER I/O	GND
28	GND	USER I/O	USER I/O	GND	USER I/O	USER I/O	GND
29	GND	USER I/O	USER I/O	GND	USER I/O	USER I/O	GND
30	GND	USER I/O	USER I/O	GND	USER I/O	USER I/O	GND
31	GND	USER I/O	USER I/O	GND	USER I/O	USER I/O	GND
32	GND	USER I/O	USER I/O	+3.3 V	USER I/O	USER I/O	GND
33	GND	USER I/O	GND				
34	GND	USER I/O	GND				
35	GND	USER I/O	GND				
36	GND	USER I/O	GND				
37	GND	USER I/O	GND				
38	GND	USER I/O	GND				
39	GND	USER I/O	GND				
40	GND	USER I/O	GND				
41	GND	USER I/O	GND				
42	GND	USER I/O	GND				
43	GND	USER I/O	GND				
44	GND	USER I/O	GND				
45	GND	USER I/O	GND				
46	GND	USER I/O	GND				
47	GND	USER I/O	GND				

Table 11 - J3 Backplane pin assignments

4.4 G-Link RX Daughter Card Connector

The G-Link RX card connector is implemented on a 60 conductor 50 mil pitch connector with the pin out shown in Table 12. See document # ESE-SVX-951018 for detailed information on the G-Link daughter card.

4.4.1 G-Link RX Connector Pin Assignments

Pin Number	Signal	Pin Number	Signal
1	DVCC	31	DGND2
2	DIV0	32	DIV1
3	VCC1	33	ERR
4	D0	34	D1
5	D2	35	D3
6	D4	36	D5
7	D6	37	D7
8	D8	38	VCC4
9	D9	39	D10
10	D11	40	D12
11	D13	41	D14
12	D15	42	D16
13	D17	43	D18
14	VCC2	44	VCC5
15	D19	45	CAV*
16	FLAG	46	LINKRDY*
17	FF	47	LOOPEN
18	DAV*	48	ACTIVE
19	RX_SIG_DET*	49	FDIS
20	STRBOUT-	50	VCC6
21	STRBOUT+	51	EQEN
22	SIMCLK-	52	RX_OPT_PWR
23	SIMCLK+	53	RX_SYS2
24	STAT1	54	RX_SYS1
25	VCC3	55	FLAGSEL
26	STAT0	56	VEE1
27	M20SEL	57	VEE2
28	VTT1	58	SMC1*
29	VTT2	59	SMC0*
30	DGND1	60	VCC7

Table 12 - G-Link RX Connector Pin Assignments

4.5 Fanout to SRC Feedback Connector

This four-bit cable utilizes the AMP Shielded Data Link Connector, 8 conductor, side entry panel and PCB ground, part number 3-520459-3. The eight wires in the cable carry four LVDS signals as shown in Table 12:

Pin	Signal
1	RUN/INIT* (true side)
2	RUN/INIT* (invert side)
3	POWER_OK (true side)
4	POWER_OK (invert side)
5	STAT0/NONFATAL_ERROR (true side)
6	STAT0/NONFATAL_ERROR (invert side)
7	STAT1/FATAL_ERROR (true side)
8	STAT1/FATAL_ERROR (invert side)

Table 13

Pinout of LVDS status/error link to SRC

5. ELECTRICAL & MECHANICAL SPECIFICATIONS

5.1 Packaging & Physical Size

The FIB Fanout is a 9U x 400mm VME card in accordance with the VME 9U X 400 mm draft format standard.

5.2 PC Board Construction

The printed circuit board will be 0.093 +/-0.008 in thick. The PC board will be six layers: power, gnd, and four signal layers.

5.3 Power Requirements

The FIB Fanout requires 5.0v @ 5 amps (estimated) and -5.2v @ 1.5 amps (estimated).

5.4 Cooling Requirements

Cooling will be provided by fans mounted on the VME crate.

6. SAFETY FEATURES & QUALITY ASSURANCE PROCEDURES

6.1 Module Fusing & Transient Supression

The FIB Fanout will include fusing and transient suppression for all incoming voltages. Fuses and transient suppression diodes will be placed as close as possible to the voltage entry point on the board. The fuses will be sized such that the board is protected against a power short on the board.

6.2 Other Safety & Quality Assurance features

Termination power supplied to the J3 backplane by the Fanout is separately fused and transient suppressed. Power for the J3 backplane comes from pins which are not used to provide module power. A temperature monitor is available on-board which may be read over VME.

7. A APPENDICES

7.1 A1 List Of Component Documentation

7.2 A2 Schematics

7.3 A3 PAL, FPGA Equations

7.4 A4 Timing Diagrams

7.5 A5 Parts List