



**Fermi National Accelerator Laboratory**

**SVX II Silicon Strip Detector Upgrade Project  
Readout Electronics**

**GSTM G-Link Receiver Adapter and  
GSTM SRC Commands Status Adapter Daughter Cards  
for Silicon Readout Controller (SRC) testing**

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## 1. GENERAL INFORMATION

This document describes and specifies two General System Test Module (GSTM) [Ref. 2,8] daughter cards named the GSTM G-Link Receiver Adapter (G-Link-RA) and the GSTM SRC Command Status Adapter (GSTM SRC CSA). These daughter cards are two of the three adapters that will be used for the Silicon Readout Controller (SRC) [Ref. 1] stand alone testing and debugging. The G-Link RA emulates the behavior of the FIB Crate Fanout Module. The GSTM SRC CSA emulates the behavior of the VME Readout Buffer Fanout Module (VRB Fanout) [Ref. 6]. A diagram of the SVX data acquisition system can be found in section 5.7.

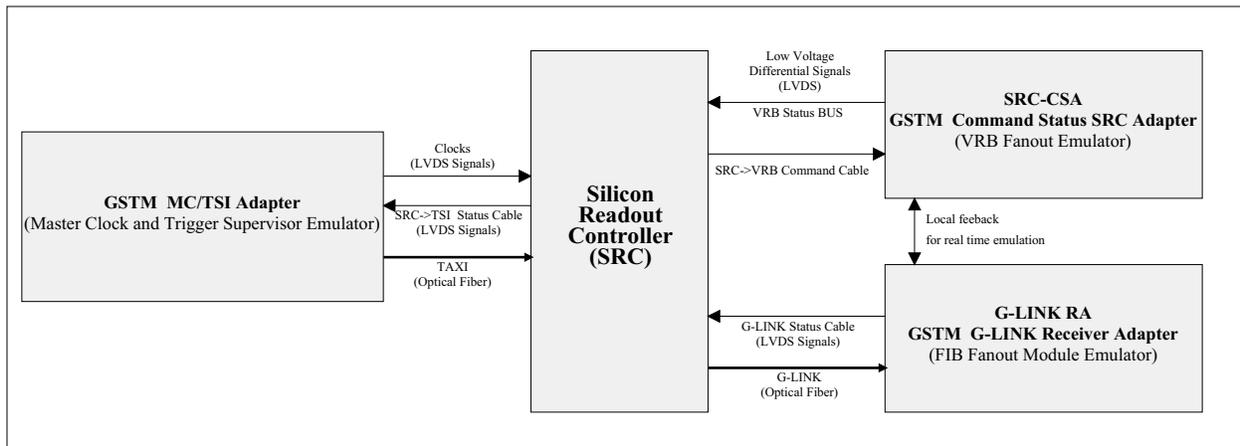


Figure 1: SRC and daughter cards block diagram

### 1.1 System Introduction

Figure 1 shows the three daughter cards needed to test the SRC: a Master Clock/Trigger Supervisor daughter card [Ref. 7], a Command Status SRC Adapter daughter card, and a G-Link Receiver Adapter daughter card.

The Master Clock/Trigger Supervisor card will generate the five differential timing signals needed by the SRC and will receive a data stream from the GSTM and re-transmit the data stream via a TAXI optical link [Ref. 7, 15]. It will also receive three coax control signal signals originating from the SRC via coax cables.

The SRC-CSA Adapter card will receive commands from the SRC (VRB Command Cable), translate, and send them as single ended TTL to the GSTM. This card will also receive data from the GSTM, translate, and transmit status and data back to the SRC (VRB Status Bus).

The G-Link-RA card will receive a data stream from the SRC via a G-Link optical link [Ref. 10, 12], convert it to single ended TTL, and send it to the GSTM. This card also implements the LVDS link that carries the G-Link handshake signals.

State machines on G-Link -RA and SRC-CSA interpret the data and commands from the SRC streams and provide a real time emulation of the FIB Fanout [Ref. 5] and VRB fanout [Ref. 3, 6] modules.

## 1.2 Description

The General System Test Module (GSTM) is a 9U x 400mm double-width VME module capable of receiving and transmitting multiple streams of data. The GSTM provides two FIFO-sourced transmit ports (T-Ports) and two receive ports (R-Ports) feeding into FIFOs for later read-back. The GSTM provides control, status, and mode signals for user-defined manipulation of custom daughter cards [Ref. 2]. Figure 2 shows a crate containing two GSTMs configured for SRC testing. Figure 3 is a block diagram of the GSTM.

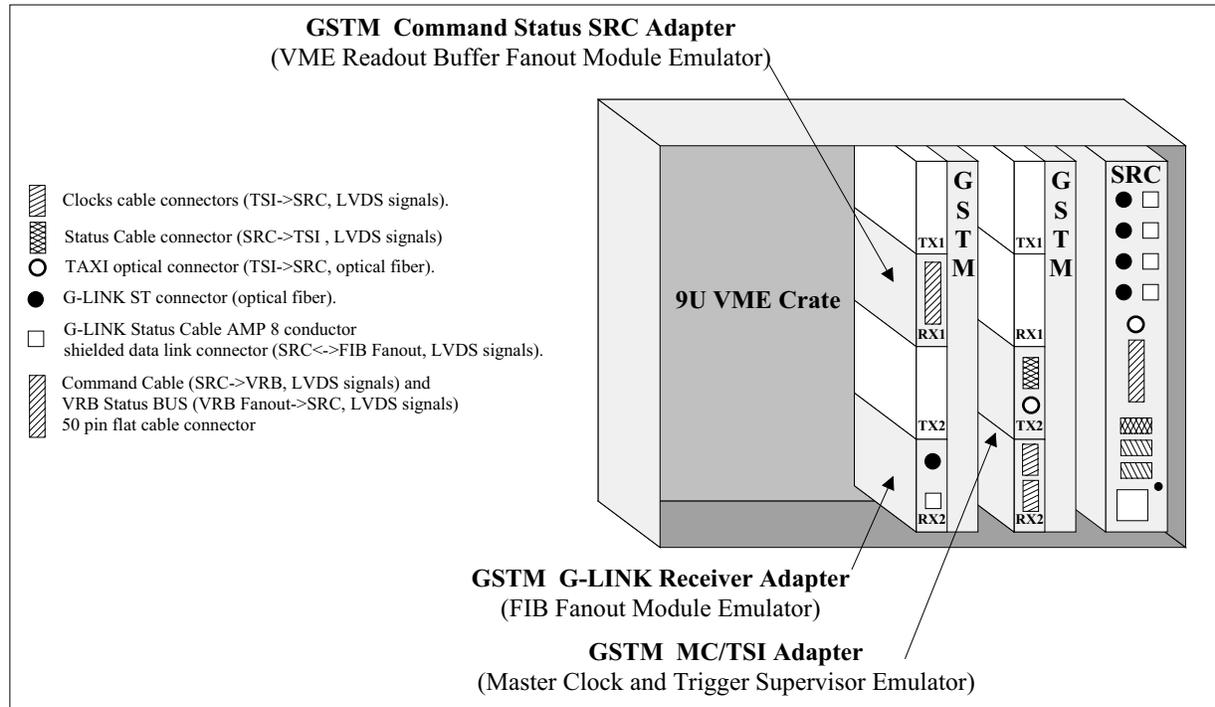


Figure 2: View of SRC test crate

The G-Link RA specified in this document will enable the GSTM to be interfaced with Silicon Readout Controller (SRC) via a G-Link optical fiber and the G-Link Status Cable. A Finisar G-Link Receiver Board FRC-1101-1 [Ref. 11] is used to receive the data transmitted by the SRC. The G-Link RA will feed the GSTM R2 port's FIFO with the data stream received from the SRC on the G-Link, but it will also interpret the commands and the data received to mimic the behavior of the FIB Crate Fanout Module [Ref. 5].

The G-Link RA can also be used in a stand-alone mode for general-purpose G-Link testing. In this mode, the state machines that emulate the FIB are not used. The PLD that implements these state machines can be re-programmed for other tasks.

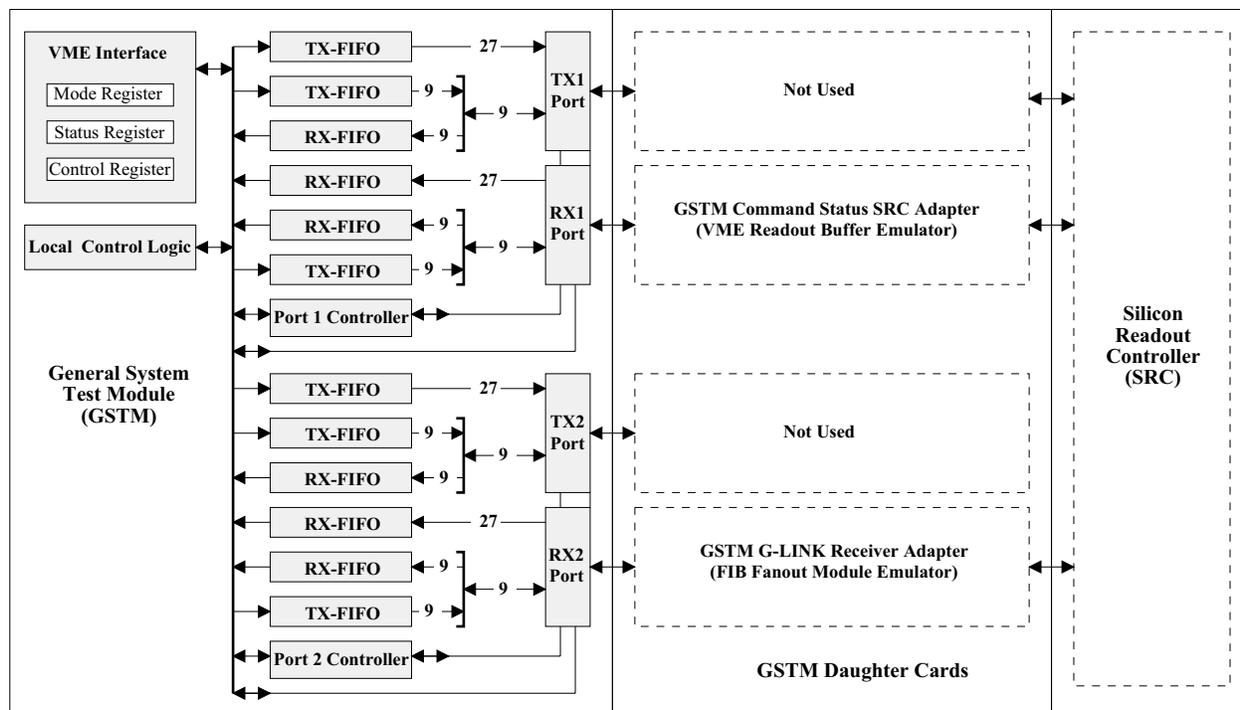


Figure 3: General System Test Module (GSTM) Block Diagram

The SRC CSA will enable the GSTM to be interfaced with the Silicon Readout Controller (SRC) [Ref. 1] via the VME Readout Buffer (VRB) Command Cable and Status Bus. The SRC CSA will interpret the commands and the data received from the SRC on VRB Command Cable and mimic the behavior of the VME Readout Buffer (VRB). It will feed the GSTM R1 port's FIFO with the data stream received from the VRB Command Cable and with the data sent to the SRC on the VRB Status Cable.

Physically, the GSTM G-Link Receiver Adapter (G-Link RA) will mount on a GSTM R2 receiving port connector. The G-Link RA will also connect to the GSTM mezzanine power connector associated with the R2 receive port. The GSTM SRC Command Status Adapter will mount a GSTM R1 receiving port connector. The SRC CSA will also connect to the GSTM mezzanine power connector associated with the R1 receive port. The two adapters will communicate via a 20 bit wide bus (40 wire wide flat cable).

### 1.3 Requirements

This is the set of requirements for the VRB/FIB emulator needed to test the SRC.

**I/O Ports:** The emulator will require four ports:

- G-Link. The emulator will receive the G-Link sourced by the SRC.
- G-Link return status. The emulator will source the “G-Link Status Cable” to the SRC. This cable contains four differential signals and is the same cable as that used by the CDF Master Clock. The signals have been defined in the specifications of the FIB Crate Fanout Module [Ref. 5]. Generally they are used to report both fatal and non-fatal G-Link errors back to the SRC.
- VRB Command Cable. The emulator will receive the VRB Command cable sourced by the SRC. This is a differential LVDS bus containing signals described in the SRC [Ref. 1] and VRB [Ref. 3, 6] documents. The signals are a 4-bit CMD bus, which specifies a command code, an 8-bit data bus, and a strobe, which validate the commands and data.
- VRB Status bus. The emulator will source the 10-bit differential LVDS status bus to the SRC. The signals are described in the SRC and VRB documents. The first two signals are the most important for the emulator, which are READ\_BUSY and SCAN\_BUSY. The remainders are error flags.

#### Emulator responses:

In the following, the FIB and VRB commands will be referred to by name. The actual codes are in the system documents.

##### 1) READOUT

READOUT refers to the movement of data from the SVXIII chip to the VRB. There are six commands and one handshake line involved. In order to effect the data transfer, the SRC does the following:

- a) Send READ and a buffer address (4-bit) to the VRB.
- b) Send PIPE\_CAP address to VRB.
- c) Send Bunch Crossing to VRB.
- d) Send DIGITIZE to the FIB.
- e) Send READOUT to the FIB.

Upon the receipt of READ, the VRB asserts READ\_BUSY within two clocks cycles ( $1\text{clk} = 132\text{ns}$ ). Assuming that the rest of the commands b, c, d, e have arrived, the emulator must wait for a time period (DIG/READ TIME) which is programmable in 132ns increments from 2usec to 10usec to emulate both digitize and readout and then deassert READ\_BUSY.

The Readout may be aborted by the SRC sending the ABORT command to the FIB. If the emulator receives this ABORT before the DIG/READ TIMER has timed out, it clears this timer and starts a much shorter programmable ABORT TIMER (3-bits will suffice) after which it deasserts READ\_BUSY.

## 2) SCAN

SCAN refers to the transfer of data from the VRB into its VME backplane and must be associated with a programmable SCAN TIME in the range of 100us to 1000us. A SCAN cycle is as follows:

- a) SRC sends the SCAN code along with a buffer address (4-bit).
- b) SRC sends EVENT ID code along with a 4-bit Event ID.

The VRB responds by asserting SCAN\_BUSY within 2 clock cycles of a). Assuming it has received the EVENT ID as well, the emulator starts its SCAN TIMER. Upon timeout, it deasserts SCAN\_BUSY. There are no FIB commands involved with the SCAN nor is there any provision for an abort.

The above fulfills the minimal requirement for the SRC to run continuously. The FIB lines, which need to be monitored for this, are the FIB Command lines and SYNC. Error checking could be considered for the presence and consistency of other bits in the 20-bit field of the FIB/G-Link word.

## 2. THEORY OF OPERATION AND OPERATING MODES

This section contains the following block diagrams, signal descriptions, tables, and state-machine diagrams:

Figure 4: G-Link-RA block diagram.  
 Figure 5: SRC-CSA block diagram.  
 Figure 6: G-Link-RA and SRC-CSA Layout.

Figure 7: G-Link Receiver Board FRC-1101-1 connector.  
 Table 1: Signals from G-Link receiver on G-Link-RA.

Figure 8: G-Link Status Cable connector.  
 Table 2: G-Link Status Cable on G-Link-RA.

Figure 9: VRB Status Bus and Command Cable connector.  
 Table 3: VRB Command Cable on SRC-CSA.  
 Table 4: VRB Status Bus on SRC-CSA.

Figure 10: GSTM R1 Port and R2 Port connectors.  
 Table 5: GSTM R2-Port Connector on G-Link-RA.  
 Table 6: GSTM R1-Port Connector on SRC-CSA.

Figure 11: Board to Board connectors.  
 Table 7: Board to Board connectors on SRC G-Link-RA and SRC-RCA.

Figure 12: GSTM Power ID connectors.

Figure 13: Readout FIB State Machine.  
 Figure 14: Readout VRB State Machine.  
 Figure 15: Scan state machine.  
 Figure 16: LEDs meaning on G-Link-RA.  
 Figure 17: LEDs meaning on SRC-CSA.

Table 8: Jumpers on the G-Link RA.  
 Table 9: Jumpers on the SRC CSA.

Table 10: Micro-switches on the G-Link RA.  
 Table 11: Micro-switches on the SRC CSA.

Table 12: Test Points on the G-Link RA.  
 Table 13: Test Points on the SRC CSA.





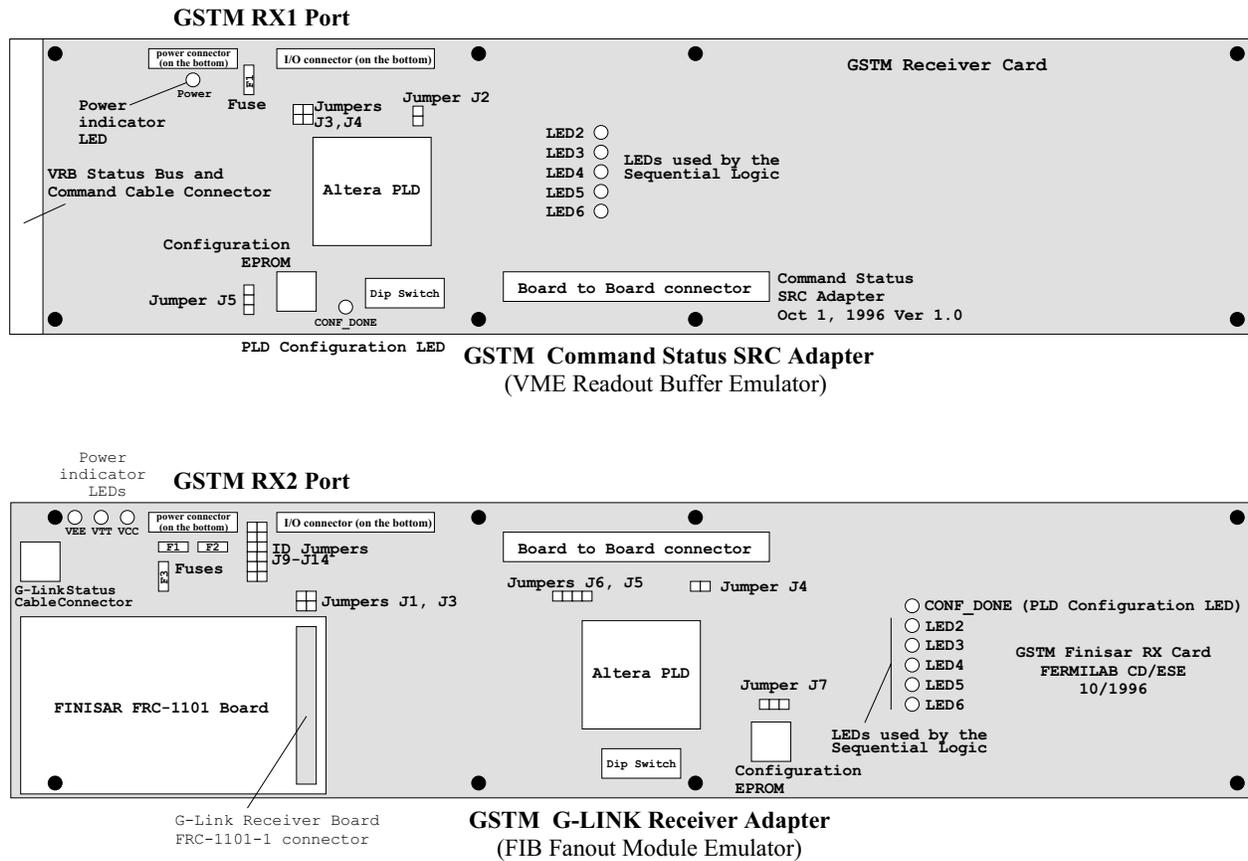


Figure 6: G-Link-RA and SRC-CSA Layout

## 2.1 INTERFACE SPECIFICATIONS

### 2.1.1 G-Link Receiver Board FRC-1101-1 Connector

Input and Output signals are defined referring to the GSTM G-Link Receiver Adapter daughter card. The names of the signals correspond to those used in the FINISAR FRC-1101Board documentation. The names of the parts (between square brackets) correspond to those used on the GSTM G-Link Receiver Adapter daughter card.

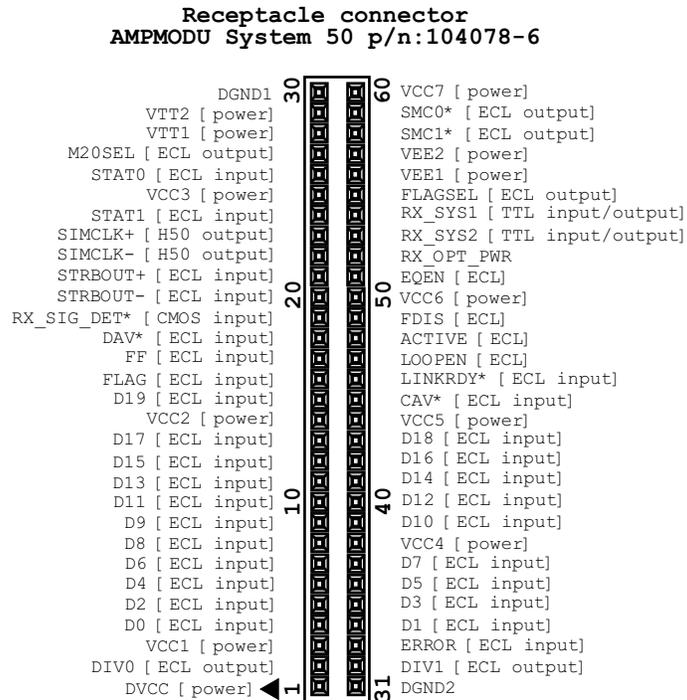


Figure 7: G-Link Receiver Board FRC-1101-1 connector

Table 1 shows the emulation of FIB Fanout Board as seen by SRC. [\[Ref. 1\]](#)

<b>Signal</b>	<b>Description</b>	<b>use in the G-Link Receiver Adapter</b>
MCLK	53 MHz Clock	Is used as clock for the sequential logic implemented on the Altera PLD. Is also forwarded to the GSTM on which is used as system clock. The GSTM provide a copy of this clock to the GSTM SRC CSA using the SYS_CLK signal (Receive port 1).
CMD	5 bit Command	Forwarded to the GSTM. Interpreted by the sequential logic implemented in the Altera PLD.
XQT	Execute Immediate	Forwarded to the GSTM.
ADV_PIPE	Advance Pipeline	Forwarded to the GSTM.
L1A	L1 Accept	Forwarded to the GSTM.
BUNCH	Bunch Crossing Number	Forwarded to the GSTM.
RDQ	Read Digitize Quiescent	Forwarded to the GSTM.
PIPE_RD2	Return Capacitor to pipe	Forwarded to the GSTM.
SYNC	SYNC signal (1/7 of MCLK frequency)	Forwarded to the GSTM. Used by the sequential logic implemented in the Altera PLD.

Table 1: Signals from G-Link receiver on G-Link-RA

Table 1A shows the emulation of FIB Fanout Board as seen by SRC. [\[Ref. 1\]](#)

<b>Command Code binary (decimal)</b>	<b>Description</b>	<b>use in the G-Link Receiver Adapter</b>
00000 (0)	No Operation	No operations performed.
00001 (1)	Abort Readout	Affect the behavior of the sequential logic.
00010 (2)	Preamp Stop Reset	No operations performed.
00100 (4)	Preamp Start Reset	No operations performed.
00101 (5)	Readout	Affect the behavior of the sequential logic.
00110 (6)	Return Cap. to pipe	Affect the behavior of the sequential logic.
00111 (7)	Digitize	Affect the behavior of the sequential logic.
01001 (9)	Calibration Inject	No operations performed.
10001 (17)	Latch Status	No operations performed.
10010 (18)	Reset SVXIII chip	No operations performed.
10011 (19)	Reset FIB	No operations performed.
10100 (20)	Reset PortCard	No operations performed.
10101 (21)	G-Link send fill frames	No operations performed.

Table 1A: Coding of CMD bits as interpreted by PLD state machine (see Figure 6)

**2.1.2 G-Link Status Cable Connector**

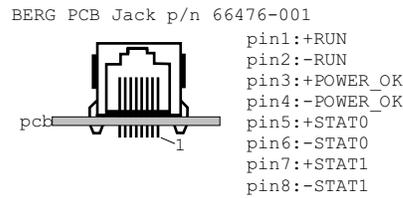


Figure 8: G-Link Status Cable connector

Table 2 shows the emulation of FIB Fanout Board as seen by SRC. [\[Ref. 5\]](#)

Signal	Description and use in the G-Link Receiver Adapter
RUN/INIT*	During system initialization the SRC drive this signal to '0', indicating that the SRC is attempting to establish the fiber optic lock. Once the lock is established, the SRC then drives this signal to '1', informing the FIB Crate Fanout Board that the data is now present on the G-Link. The Fanout biases the RUN/INIT* line to '0' such that a disconnected cable leaves the devices in the Initialize mode. Forwarded as signal "P-Status1" to the GSTM Port R2. Is used also to control the select signal of a multiplexer on the Altera PLD.
STAT0/ FATAL	When RUN/INIT is low (Init) this sends the STAT0 signal from the G-Link phase-locked loop. When RUN/INIT is high, this indicates a fatal error has occurred. The SRC biases this line to a '1' in order to detect a disconnected cable. Is controlled by the logic on the Altera PLD. Is a copy of "STAT0" if "RUN/INIT*" is "0". Is a copy of "TEST_BIT0" if RUN/INIT* is "1".
STAT1/ Non-Fatal	During initialization, this sends the STAT1 signal from the G-Link. At other times, this indicates that a non-fatal error has occurred. Is controlled by the logic on the Altera PLD. Is a copy of "!LINKRDY*" if "RUN/INIT*" is "0". Is a copy of "TEST_BIT1" if RUN/INIT* is "1".
Power_OK	This bit is driven to 1 if the power is OK. In the event of a power failure of the -5.2 Volt supply, this bit is actively driven to a '0'. The SRC biases this line to a '1' at its receiver so that in the event of a +5.0 Volt failure an error is also recorded. Is controlled by the logic on the Altera PLD. Is "1" if "RUN/INIT*" is "0". Is a copy of "P-CNTRL1" if RUN/INIT* is "1".

Table 2: G-Link Status Cable on G-Link-RA

### 2.1.3 VRB Status Bus and Command Cable Connector

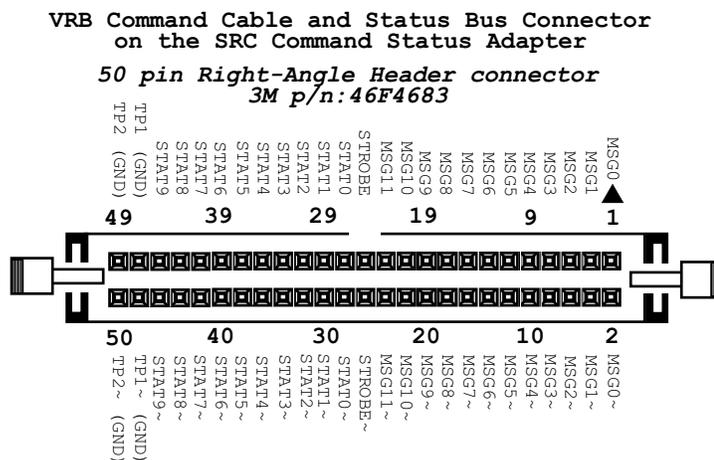


Figure 9: VRB Status Bus and Command Cable connector

Table 3 shows the emulation of VRB Fanout Board as seen by SRC [\[Ref. 3, 6\]](#)

Signal	Description	use in the SRC Command Status Adapter
Data Strobe	data validation signal	Forwarded to the GSTM as “DAT_R12”. Used by the sequential logic as validation signal for the commands (CMD) and data.
CMD	4 bit commands	Forwarded to the GSTM. Interpreted by the sequential logic implemented in the Altera PLD.
DATA	8 bit of data	Forwarded to the GSTM. Interpreted by the sequential logic implemented in the Altera PLD.

Table 3: VRB Command Cable on SRC-CSA

Table 3A shows the emulation of VRB Fanout Board as seen by SRC [\[Ref. 3, 6\]](#)

Command Code binary (decimal)	Description	use in the SRC Command Status Adapter
0000 (0)	No Operation	No operations performed.
0001 (1)	Readout Buffer	Affect the behavior of the sequential logic.
0010 (2)	Pipeline Capacitor Number	Affect the behavior of the sequential logic.
0011 (3)	Bunch Crossing Number	Affect the behavior of the sequential logic.
0100 (4)	Scan Buffer	Affect the behavior of the sequential logic.
0101 (5)	Event Buffer	Affect the behavior of the sequential logic.
0110 (6)	Reset	No operations performed.

Table 3A: Interpretation of CMD bits by PLD state machines (see Figures 7 and 8)

Table 4 shows the emulation of VRB Fanout Board signals as seen by SRC [Ref. 3, 6]

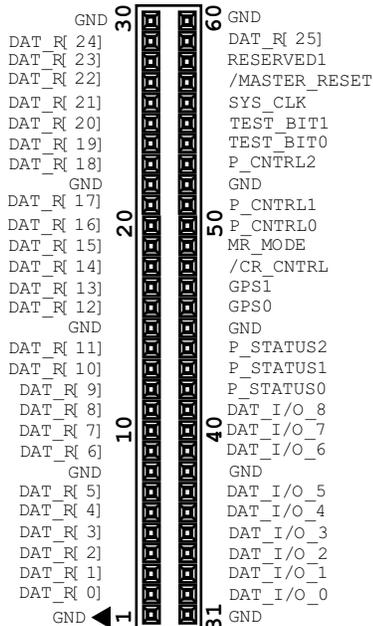
Signal	Description and use in the SRC Command Status Adapter
READOUT_BUSY	Is driven low when a READOUT BUFFER message is received by the VRB and is released when all active channels on the VRB have received the event data. Controlled by the sequential logic on the Altera PLD.
SCAN_BUSY	Is driven low when a SCAN BUFFER message is received by the VRB and is released when the VRB has been read out through VME. Controlled by the sequential logic on the Altera PLD.
SYNC_ERROR	Error Flag. Used by the VRB to flag a link synchronization error on one of the data links. Is a copy of DAT_I/O_0 from GSTM..
FRAME_ERROR	Error Flag. Used by the VRB to flag a non-valid data word on one of the data links. Is a copy of DAT_I/O_1 from GSTM..
IDENTIFIER_ERROR	Error Flag. Used by the VRB to flag an invalid event identifier (crossing number, capacitor number, etc.) in the data stream. Is a copy of DAT_I/O_2 from GSTM..
FORMAT_ERROR	Error Flag. Used by the VRB to flag that a data format error has occurred. Data format errors indicate markers (channel numbers, chip IDs, etc.) which are outside the valid range or not in the expected location in the data stream. Is a copy of DAT_I/O_3 from GSTM..
CONTROLLER_ERROR	Error Flag. Used by the VRB to flag unrecognizable or invalid SRC messages. Is a copy of DAT_I/O_4 from GSTM..
VRB_ERROR	Error Flag. Used by the VRB to flag all other errors, including buffer overflow. Is a copy of DAT_I/O_5 from GSTM.
RESERVED	Error Flag. Is a copy of DAT_I/O_6 from GSTM.
RESERVED	Error Flag. Is a copy of DAT_I/O_7 from GSTM.

Table 4: VRB Status Bus on SRC-CSA

### 2.1.4 GSTM Receiver Connectors

**GSTM R1 Port Connector  
on the SRC Command Status Adapter**

**Receptacle connector  
AMPMODU System 50 p/n:104078-6**



**GSTM R2 Port Connector  
on the G-Link Receiver Adapter**

**Receptacle connector  
AMPMODU System 50 p/n:104078-6**

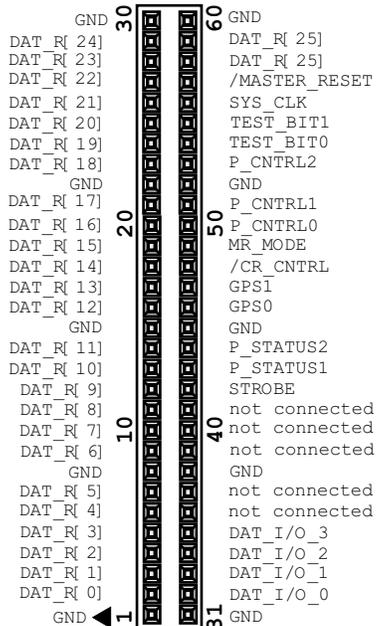


Figure 10: GSTM R1 Port and R2 Port connectors

Signal	use in the G-Link Receiver Adapter
SYS CLK	Not used.
P-CNTRL 0	Used to reset the state machines on the Altera PLD.
P-CNTRL 1	Used as input of a multiplexer. Control the signal "POWER_OK" when "RUN/INIT*" is "1".
P-CNTRL 2	Used to control the signal "FLAGSEL" of the G-Link Receiver.
TEST BIT 0	Used as input of a multiplexer. Control the signal "STAT0/ FATAL_ERROR" when "RUN/INIT*" is "1".
TEST BIT 1	Used as input of a multiplexer. Control the signal "STAT1/NON_FATAL_ERROR" when "RUN/INIT*" is "1".
/CR_CNTRL	Used to reset the G-Link Receiver (signal SMC1*)
MR_MODE	Used to control the signal "M20SEL" of the G-Link Receiver.
/MASTER RESET	Used to reset all the electronics. It will reset both the G-Link Receiver and the Altera PLD.
P-STATUS 0	Used to forward the clock coming from the G-Link Receiver to the GSTM. This clock will be forwarded by the GSTM to the GSTM SRC CSA.
P-STATUS 1	Copy of the signal "RUN/INIT*" coming from the SRC on the G-Link Status Cable.
P-STATUS 2	Not used.
GPS 0	Copy of the signal "RUN/INIT*" coming from the G-Link Receiver.
GPS 1	Copy of the signal "LINKRDY*" coming from the G-Link Receiver.
DAT_R25	Signal "/START_FIFO" generated on the Altera PLD from the Boolean equation:

	(LINKRDY*)OR((CAV*)AND(DAV*)). Is used on the GSTM as FIFOs control signal.
DAT_R24	Copy of the signal "STAT0" coming from the G-Link Receiver.
DAT_R23	Copy of the signal "DAV*" coming from the G-Link Receiver.
DAT_R22	Copy of the signal "CAV*" coming from the G-Link Receiver.
DAT_R21	Copy of the signal "FF" coming from the G-Link Receiver.
DAT_R20	Copy of the signal "FLAG" coming from the G-Link Receiver.
DAT_R[19..0]	Copy of the signals "D[0..19]" coming from the G-Link Receiver.
DAT_I/O[8..4]	Not used. Not connected.
DAT_I/O3	Signal SM2; trace the behavior of the Readout FIB State Machine.
DAT_I/O2	Signal SM1; trace the behavior of the Readout FIB State Machine.
DAT_I/O1	Signal SM0; trace the behavior of the Readout FIB State Machine.
DAT_I/O0	Copy of the signals "ERR" coming from the G-Link Receiver.

Table 5 GSTM R2-Port Connector on G-Link-RA [Ref. 2, 8]

Signal	use in the SRC Command Status Adapter
SYS CLK	This clock is a copy of the clock coming from the G-Link Receiver. Is used as clock for the sequential logic on the Altera PLD.
DAT_I/O[8..0]	Not used.
P-CNTRL 0	Used to reset the state machines on the Altera PLD.
P-CNTRL 1	Not used.
P-CNTRL 2	Not used.
TEST BIT 0	Not used.
TEST BIT 1	Not used.
/CR_CNTRL	Not used.
MR_MODE	Not used.
/MASTER RESET	Used to reset all the electronics. It will reset the Altera PLD.
P-STATUS 0	Not used.
P-STATUS 1	Not used.
P-STATUS 2	Not used.
GPS 0	Not used.
GPS 1	Not used.
GSTM RESERVED1	Signal "/START_FIFO" generated on the Altera PLD from the Boolean equation: (LINKRDY*)OR((CAV*)AND(DAV*)). Is used on the GSTM as FIFOs control signal.
DAT_R24	Signal SM1; trace the behavior of the Scan State Machine.
DAT_R23	Signal SM0; trace the behavior of the Scan State Machine.
DAT_R[22..13]	Copy of the signals "STAT[9..0]" generated on the Altera PLD.
DAT_R12	Copy of the signal "DATA_STROBE" coming from the VRB Command Cable.
DAT_R[11..0]	Copy of the signals "MSG[11..0]" coming from the VRB Command Cable.

Table 6: GSTM R1-Port Connector on SRC-CSA [Ref. 2, 8]

### 2.1.5 Board to Board Connectors

**Board to Board Connectors  
on the G-Link Receiver Adapter  
and on the SRC Command Status Adapter**

**40 pin Vertical Header connector  
3M p/n:3432-6303**

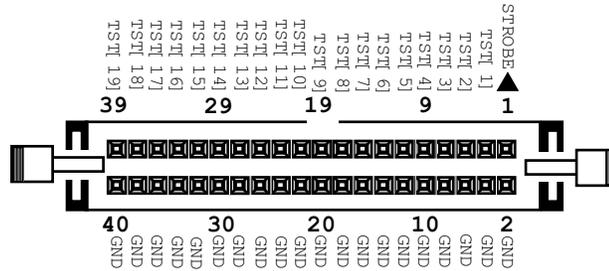


Figure 11: Board to Board connectors

Signal	use
TST[19..5]	Not used.
TST[4]	Signal “/Start_fifo” from SRC G-Link RA to SRC CSA.
TST[3]	Signal “endcount_FIB_counters” from G-Link RA to SRC CSA.
TST[2]	Signal “received_VRB_commands” from SRC CSA to G-Link RA.
TST[1]	Not used.
STROBE	Signal STROBE from SRC G-Link RA to SRC CSA.

Table 7: Board to Board connectors on G-Link-RA and SRC-CSA

### 2.1.6 GSTM Power ID connectors

**GSTM Power Connector  
on the G-Link Receiver Adapter  
and on the SRC Command Status Adapter**

**Header connector  
AMPMODU System 50 p/n:104068-4**

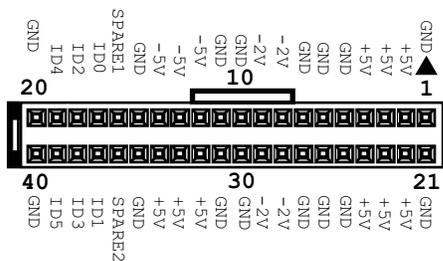


Figure 12: GSTM Power ID connectors

2.2 STATE MACHINES

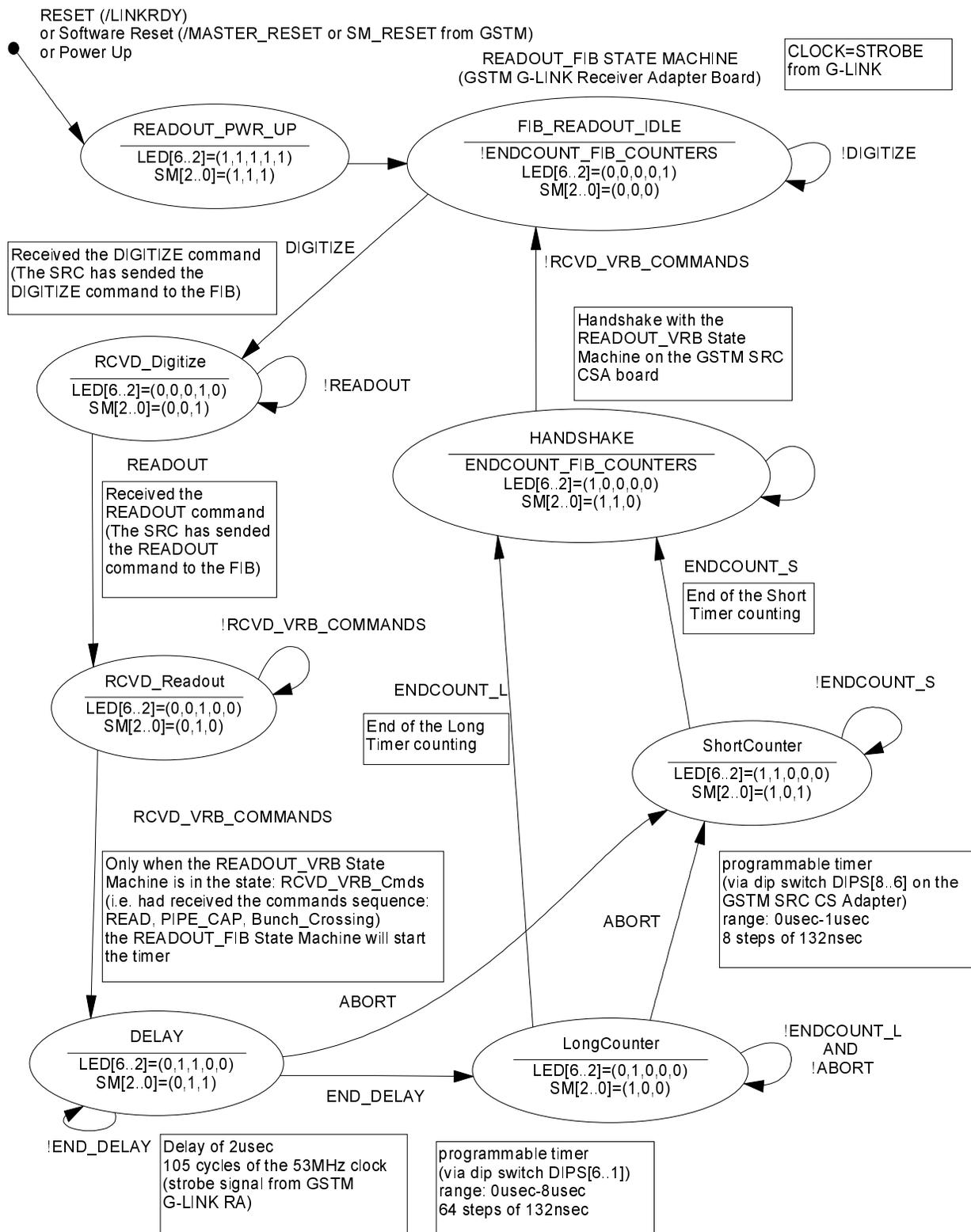
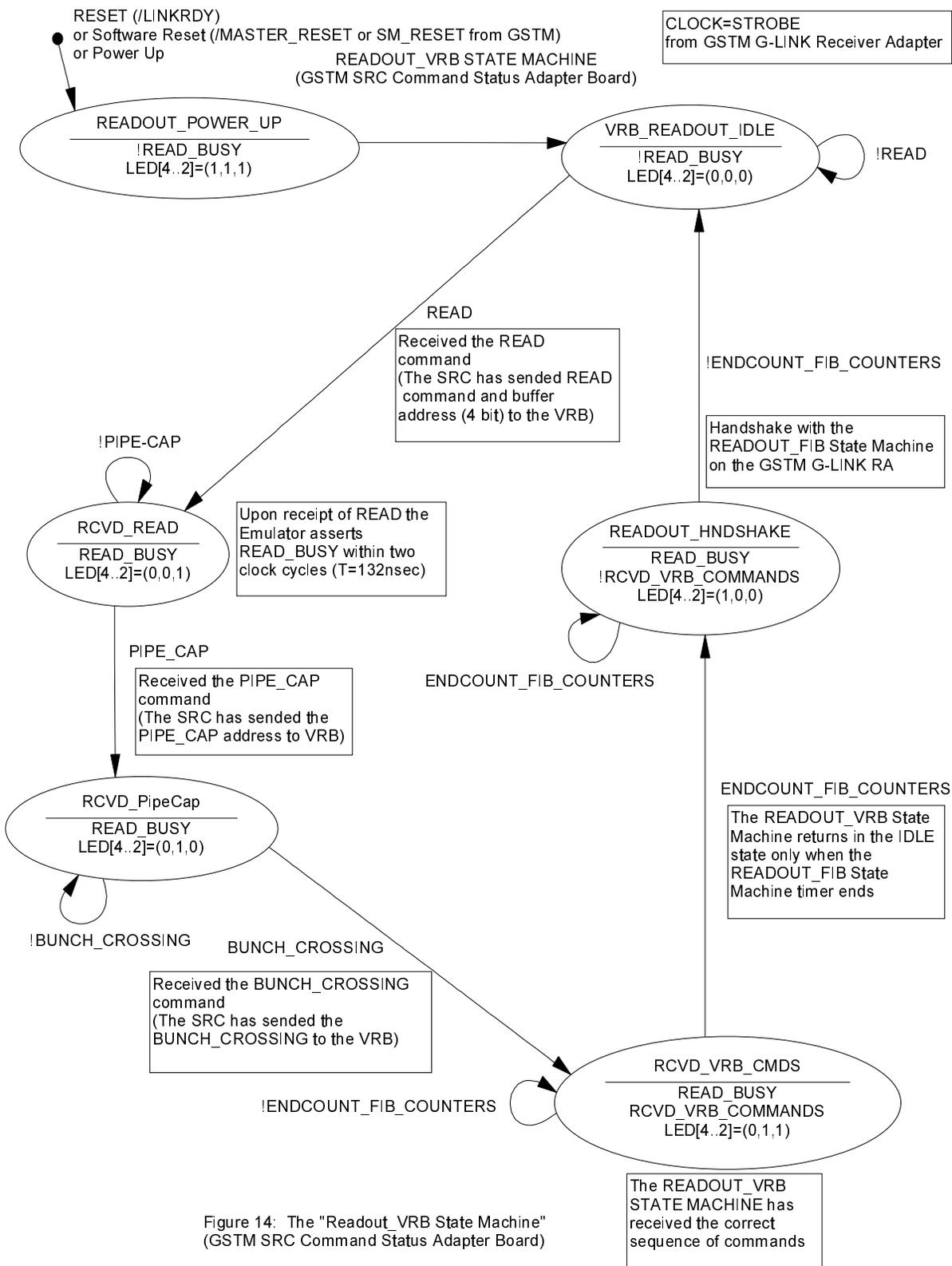


Figure 13: The "Readout\_FIB State Machine" (GSTM G-LINK Receiver Adapter Board)







### 2.2.2 Jumper, Switches and Test Points

Jumper	standard position	use
J1	open	Signal GL_DIV0 to GND. This jumper together with J3 program the VCO divider chain of the G-Link Receiver board (FRC-1101-1) to operate at full speed, half speed, quarter speed or one-eighth speed.
J3	open	Signal GL_DIV1 to GND. This jumper together with J1 program the VCO divider chain of the G-Link Receiver board (FRC-1101-1) to operate at full speed, half speed, quarter speed or one-eighth speed.
J4	closed	Signal MSEL1 to GND. The Jumper J4, J5, J6 are used to select the configuration mode of the Altera PLD. When all three jumper are installed the selected configuration is "Active Serial".
J5	closed	Signal MSEL0 to GND. See J4.
J6	closed	Signal nSP to GND. See J4.
J7	left position	EPROM Output Enable to /MASTER_RESET or to /STATUS. Allow selecting two different types of serial configuration of the Altera PLD. Active serial (right position) and Active Serial with Reconfiguration on Error (left position).
J9	closed	Signal ID0 to GND. Used by the GSTM to identify which daughter card is plugged in the Receiving Port (R2).
J10	open	Signal ID2 to GND. Used by the GSTM to identify which daughter card is plugged in the Receiving Port (R2).
J11	closed	Signal ID4 to GND. Used by the GSTM to identify which daughter card is plugged in the Receiving Port (R2).
J12	open	Signal ID1 to GND. Used by the GSTM to identify which daughter card is plugged in the Receiving Port (R2).
J13	open	Signal ID3 to GND. Used by the GSTM to identify which daughter card is plugged in the Receiving Port (R2).
J14	open	Signal ID5 to GND. Used by the GSTM to identify which daughter card is plugged in the Receiving Port (R2).

Table 8: Jumpers on the G-Link RA

Jumper	standard position	use
J2	closed	Signal MSEL1 to GND. The Jumper J2, J3, J4 are used to select the configuration mode of the Altera PLD. When all three jumper are installed the selected configuration is "Active Serial".
J3	closed	Signal MSEL0 to GND. See J2.
J4	closed	Signal nSP to GND. See J2.
J5	left position	EPROM Output Enable to /MASTER_RESET or to /STATUS. Allow selecting two different types of serial configuration of the Altera PLD. Active serial (right position) and Active Serial with Reconfiguration on Error (left position).

Table 9: Jumpers on the SRC CSA

Switch	use
[8..7]	Control the use of the LEDs. <b>Switch[8..7]      use of the LEDs</b> (0,0)      Monitor the READOUT_FIB State Machine (0,1)      Monitor the signals: FLAG, FF, /CAV, /DAV, /LINKREADY (1,0)      Monitor the signals: /CR_CONTROL, P_CONTROL0, P_CONTROL1, ENDCOUNT_FIB_COUNTERS, RCVD_VRB_COMMANDS (1,1)      Monitor the signals: LV_RUN, TEST_BIT0, TEST_BIT1, STAT0, /LINKREADY
[6..1]	Used to control the delay introduced by the "Long Counter" on the READOUT_FIB STATE MACHINE in steps of 132nsec (64 steps, range 0usec-8usec). The "STROBE" signal (53Mhz clock) from the G-Link Receiver (FRC-1101-1) is used as time reference.

Table 10: Micro-switches on the G-Link RA

Switch	use
[8..6]	Used to control the delay introduced by the "Short Counter" on the READOUT_FIB STATE MACHINE ( <u>on the G-Link RA</u> ) in steps of 132nsec (8 steps, range 0usec-1usec). The "STROBE" signal (53Mhz clock) from the G-Link Receiver (FRC-1101-1) is used as time reference.
[5..1]	Used to control the delay introduced by the "Scan Timer" on the SCAN STATE MACHINE in steps of 50usec (32 steps, range 0usec-1600usec). The "SYS_CLOCK" signal (53Mhz clock) from the GSTM is used as time reference.

Table 11: Micro-switches on the SRC CSA

Test Point	use
P1	Copy of the signal FLAG (TTL) from G-Link Receiver Board FRC-1101-1.
P2	Copy of the signal FF (TTL) from G-Link Receiver Board FRC-1101-1.
P3	Copy of the signal CAV* (TTL) from G-Link Receiver Board FRC-1101-1.
P5	Copy of the signal DAV* (TTL) from G-Link Receiver Board FRC-1101-1.
P6	Copy of the signal LINKRDY* (TTL) from G-Link Receiver Board FRC-1101-1.
P7	Copy of the signal STAT0 (TTL) from G-Link Receiver Board FRC-1101-1.
P8	Copy of the signal /START_FIFO (TTL) generate on the Altera PLD from the Boolean equation: (LINKRDY*)OR((CAV*)AND(DAV*)).

Table 12: Test Points on the G-Link RA

Test Point	use
P20	Copy of the signal READOUT_BUSY generated on the Altera PLD.
P21	Copy of the signal SCAN_BUSY generated on the Altera PLD.
P22	Copy of the signal SYNC_ERROR from GSTM.
P23	Copy of the signal FRAME_ERROR from GSTM.
P24	Copy of the signal IDENTIFIER_ERROR from GSTM.
P25	Copy of the signal FORMAT_ERROR from GSTM.
P26	Copy of the signal CONTROLLER_ERROR from GSTM.
P27	Copy of the signal VRB_ERROR from GSTM.
P28	Copy of the signal SRC_RESERVED1 from GSTM.
P29	Copy of the signal SRC_RESERVED2 from GSTM.
P30	Copy of the signal SYS_CLK from GSTM.
P31	Dedicate Input of the Altera PLD. Not used.

Table 13: Test Points on the SRC CSA

### 3. ELECTRICAL & MECHANICAL SPECIFICATIONS

#### 3.1 Packaging and Physical size

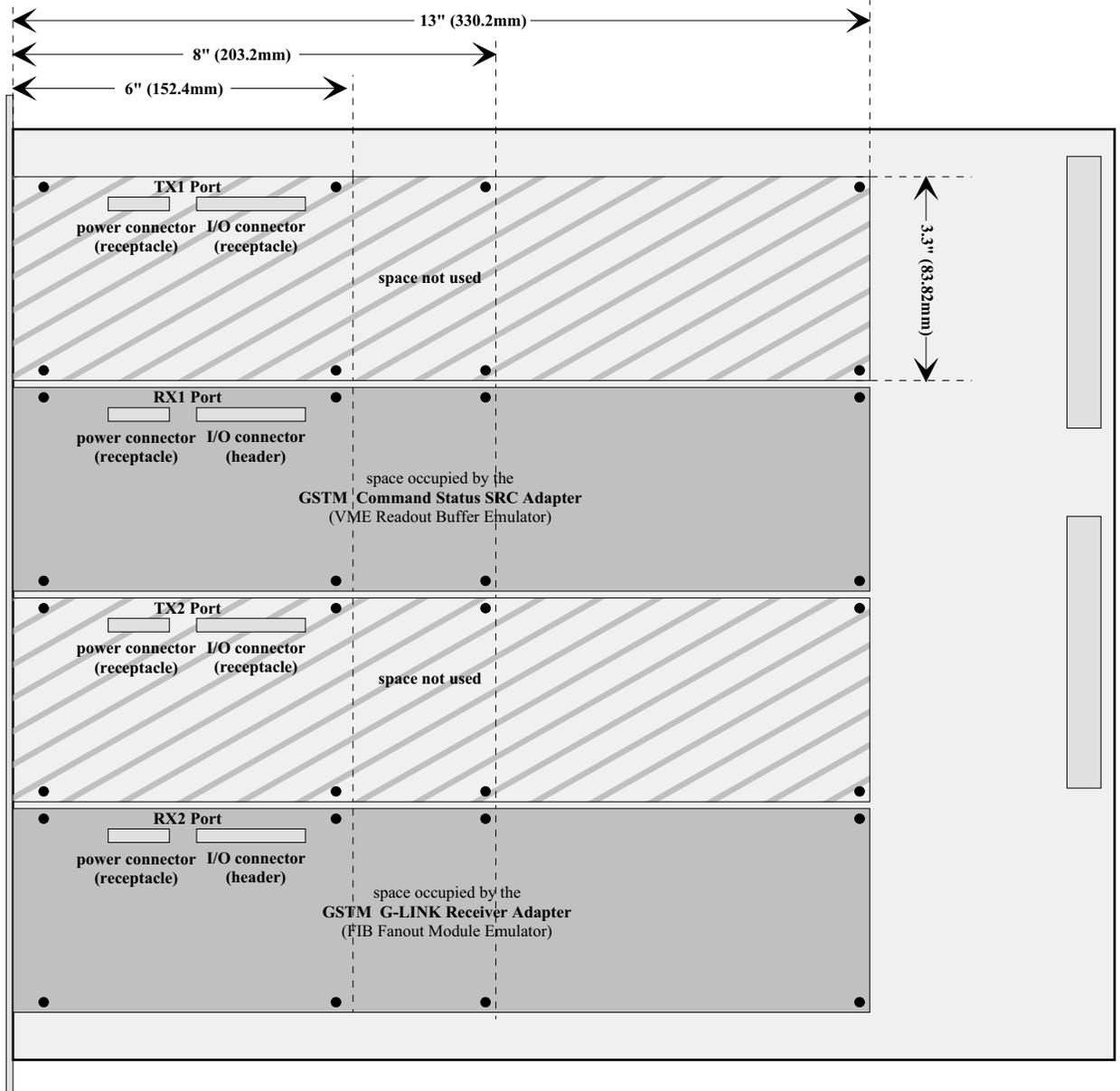


Figure 18: The GSTM Module with two of the three GSTM daughter cards used for the SRC testing

### 3.2 PC Board Construction

Both boards have been designed using Synario Software for the Schematic Capture and OrCAD Software for the Layout. PC Board construction specifications as follows:

The boards are made of FR4 glass-fabric-base epoxy with a thickness of .093" (2.36mm).

Their dimension is: 3.3" X 13" (83.82mm X 330.2mm)

G-Link RA:

8 Layers (2 grounds, 2 powers, 4 traces)

Impedance controlled board (100 Ohm).

SRC CSA:

6 Layers (1 ground, 1 power, 4 traces)

### 3.3 Power Requirements

G-Link RA:

3.25 watts (current: 0.65 Amp.) from the +5V supply (VCC).

4.42 watts (current: 0.85 Amp.) from the -5.2V supply (VEE).

0.3 watts (current: 0.15 Amp.) from the -2V supply (VTT).

SRC CSA:

0.5 watts (current: 0.1 Amp.) from the +5V supply (VCC).

### 3.4 Cooling Requirements

Minimally, a conventional VME air-cooling fan tray is recommended for any VME installation. Otherwise, no supplemental cooling is required for the GSTM G-Link RA and the GSTM SRC CSA.

#### **4. SAFETY FEATURES & QUALITY ASSURANCE PROCEDURES**

##### **4.1 Module Fusing & Transient Suppression**

Both the G-Link Receiver Adapters and the SRC Command Status Adapter are protected with fuses and transorbs.

G-Link RA:

Fuse on the +5V supply (VCC from GSTM), F1, 1A fast.

Fuse on the -5V supply (VEE from GSTM), F2, 1A fast.

Fuse on the -2V supply (VTT from GSTM), F3, 1A fast.

Transorbs: Motorola ICTE 1N5908.

SRC CSA:

On the +5V supply (VCC from GSTM):

Fuse F1, 1A fast.

Transorb Motorola ICTE 1N5908.

## 5. APPENDICES

### 5.1 Part List and Component Documentation

#### G-Link RA:

Component	Quantity	Information
Altera EPF8452AQC160-3	1	Programmable Logic Device. <a href="#">[Ref. 18]</a>
Altera EPC1064LC20	1	EPROM. One Time Programmable package. <a href="#">[Ref. 18]</a>
Synergy 100H600JC	1	9 bit TTL to ECL Translator. <a href="#">[Ref. 21]</a>
Synergy 100H601JC	3	9 bit ECL to TTL Translator. <a href="#">[Ref. 21]</a>
National 100325JC	1	Low Power Hex ECL to TTL Translator. <a href="#">[Ref. 22]</a>
National 90C031TM	1	LVDS Quad CMOS Differential Line Driver. <a href="#">[Ref. 23]</a>
National 90C032TM	1	LVDS Quad CMOS Differential Line Receiver. <a href="#">[Ref. 23]</a>
SN74ALS1004	1	HEX Inverting Drivers. <a href="#">[Ref. 24]</a>
FRC-1101-1	1	Finisar fiber optic/G-Link receiver card <a href="#">[Ref. 11, 12, 13, 14]</a>
AMP 104068-4	1	40 pin header connector, AMPMODU System 50. <a href="#">[Ref. 25]</a>
AMP 104078-6	2	60 pin receptacle connector, AMPMODU System 50. <a href="#">[Ref. 25]</a>
AMP 821815-1	1	20 pin PLCC socket. <a href="#">[Ref. 25]</a>
3M 3432-6302	1	40 pin header connector. <a href="#">[Ref. 26, 27]</a>
3M 3417-6640	1	40 pin flat cable connector. <a href="#">[Ref. 26, 27]</a>

#### SRC CSA:

Component	Quantity	Information
Altera EPF8452AQC160-3	1	Programmable Logic Device. <a href="#">[Ref. 18]</a>
Altera EPC1064LC20	1	EPROM. One Time Programmable package. <a href="#">[Ref. 18]</a>
National 90C031TM	3	LVDS Quad CMOS Differential Line Driver. <a href="#">[Ref. 23]</a>
National 90C032TM	4	LVDS Quad CMOS Differential Line Receiver. <a href="#">[Ref. 23]</a>
SN74ALS1004	1	HEX Inverting Drivers. <a href="#">[Ref. 24]</a>
AMP 104068-4	1	40 pin header connector, AMPMODU System 50. <a href="#">[Ref. 25]</a>
AMP 104078-6	1	60 pin receptacle connector, AMPMODU System 50. <a href="#">[Ref. 25]</a>
AMP 821815-1	1	20 pin PLCC socket. <a href="#">[Ref. 25]</a>
3M 3432-6302	1	40 pin header connector. <a href="#">[Ref. 26, 27]</a>
3M 3417-6640	1	40 pin flat cable connector. <a href="#">[Ref. 26, 27]</a>
3M 3433-5302	1	50 pin header connector. <a href="#">[Ref. 26, 27]</a>

## 5.2 Schematics

Follow the schematics of the G-Link Receiver Adapter (3 pages) and the SRC Command Status Adapter (3 pages).

## 5.3 G-Link Receiver Board FRC-1101-1 Connector pinout

Pin Number	Signal [type]	Information
1	DVCC [power]	Digital +5Volts for optics
2	DIV0 [ECL output]	<b>VCO Divider Select</b> pin0. This pin together with pin DIV1 program the VCO divider chain to operate at full speed, half speed, quarter speed or one-eighth speed. {Jumper to Ground [J1], Connector [J2]}
3	VCC1 [power]	ECL_VCC (Connected to Ground)
4	D0 [ECL input]	D0 to D19 are the Data Outputs. 20 bit of data are received and decoded when M20SEL is Active, otherwise 16 bit of data are decoded and D16..D19 are undefined. All this pins are designed to interface directly with the ECL100K family. The termination must be done just before the Translator with a 300Ω Resistor to VTT. {Connector [J2], 100Ω Transmission line (L<10cm), 300Ω Termination to VTT [R1], Translator [U3], Altera PLD}
5	D2 [ECL input]	{Connector [J2], 100Ω Transmission line, 300Ω Termination to VTT [R1], Translator [U3], Altera PLD}
6	D4 [ECL input]	{Connector [J2], 100Ω Transmission line, 300Ω Termination to VTT [R1], Translator [U3], Altera PLD}
7	D6 [ECL input]	{Connector [J2], 100Ω Transmission line, 300Ω Termination to VTT [R1], Translator [U3], Altera PLD}
8	D8 [ECL input]	{Connector [J2], 100Ω Transmission line, 300Ω Termination to VTT [R2], Translator [U1], Altera PLD}
9	D9 [ECL input]	{Connector [J2], 100Ω Transmission line, 300Ω Termination to VTT [R2], Translator [U1], Altera PLD}
10	D11 [ECL input]	{Connector [J2], 100Ω Transmission line, 300Ω Termination to VTT [R2], Translator [U1], Altera PLD}
11	D13 [ECL input]	{Connector [J2], 100Ω Transmission line, 300Ω Termination to VTT [R2], Translator [U1], Altera PLD}
12	D15 [ECL input]	{Connector [J2], 100Ω Transmission line, 300Ω Termination to VTT [R2], Translator [U1], Altera PLD}
13	D17 [ECL input]	{Connector [J2], 100Ω Transmission line, 300Ω Termination to VTT [R3], Translator [U2], Altera PLD}
14	VCC2 [power]	ECL_VCC (Connected to Ground)
15	D19 [ECL input]	{Connector [J2], 100Ω Transmission line, 300Ω Termination to VTT [R3], Translator [U2], Altera}
16	FLAG [ECL input]	<b>Flag Bit:</b> if both Tx and Rx have FLAGSEL asserted, this output indicates the value of the transmitted flag bit, then this received bit can be treated <u>just like an extra data bit</u> . If both Tx and Rx have FLAGSEL set low, FLAG is used to differentiate the even frame from the odd frame in the line code. {Connector [J2], 100Ω Transmission line, 300Ω Termination to VTT [R3], Translator [U2], Altera PLD}

17	FF [ECL input]	<b>Fill Frame Status:</b> During a given STRBOUT clock cycle, if neither DAV, CAV, or ERROR are active, then the currently received frame is a fill frame. The type of fill frame received is indicated by FF pin. If FF is low, then FF0 has been received. If FF is High, then either FF1a or FF1b has been received. {Connector [J2], 100Ω Transmission line, 300Ω Termination to VTT [R3], Translator [U2], Altera PLD}
18	DAV* [ECL input]	<b>Data Available Output:</b> This active-low signal indicates that the Rx chip (on the Finisar G-Link receiver board) data output, D0..D19, have received data frames. Data should be latched on the rising edge of STRBOUT. Note that during link startup, false data indications may be given. The DAV* and LINKRDY outputs can be used together to avoid confusion during link startup. {Connector [J2], 100Ω Transmission line, 300Ω Termination to VTT [R3], Translator [U2], Altera PLD}
19	RX_SIG_DET* [CMOS input]	CMOS input, active low, must be left open or be tied to pin 16 on the FTM-8510 transmitter. This line is used to drive a low current (<3mA) LED for link status indication on the Finisar FRC-1101-1 board. Refer to Finisar FRM-8510 Data Sheet and to Finisar AN-2010. {Connector [J2], Floating}
20	STRBOUT- [ECL input]	<b>Recovered Frame-rate Data Clock Output</b> (complementary input) The terminations should be compliant to the Hewlett Packard HDMP-1014 Receiver Data Sheet. {Connector [J2], 100Ω Transmission line, 120Ω Termination to VTT [R5B], Translator [U5]}
21	STRBOUT+ [ECL input]	<b>Recovered Frame-rate Data Clock Output</b> this signal is the PLL recovered frame rate clock. D0..D19, FLAG, DAV, CAV, FF, LINKRDY, and ERROR should all be latched on the rising edge of STRBOUT. {Connector [J2], 100Ω Transmission line, 120Ω Termination to VTT [R5A], Translator [U5], Altera & GSTM}
22	SIMCLK- [H50 output]	Reference clock (inverting output). To the Rx module during simplex operation. See Hewlett Packard HDMP-1014 Receiver Data Sheet, Simplex Method III: Simplex with Reference Oscillator. {Connector [J2], Floating}
23	SIMCLK+ [H50 output]	Reference clock. To the Rx module during simplex operation. See Hewlett Packard HDMP-1014 Receiver Data Sheet, Simplex Method III: Simplex with Reference Oscillator. {Connector [J2], Floating}
24	STAT1 [ECL input]	<b>State Machine Status Output.</b> This signal together with STAT0 indicates the current Rx Link Control state-machine state. See Hewlett Packard HDMP-1014 Receiver Data Sheet, Rx Control State Machine Operation Principle. {Connector [J2], connection with FDIS and ACTIVE, 300Ω Termination to VTT [R4]}
25	VCC3 [power]	ECL_VCC (Connected to Ground)
26	STAT0 [ECL input]	<b>State Machine Status Output.</b> This signal together with STAT1 indicates the current Rx Link Control state-machine state. See Hewlett Packard HDMP-1014 Receiver Data Sheet, Rx Control State Machine Operation Principle. {Connector [J2], 100Ω Transmission line (L<10cm), 300Ω Termination to VTT [R3], Translator [U2], Altera PLD}
27	M20SEL [ECL output]	<b>16 or 20 bit Word Select:</b> When this signal is high, the link operates in 20-bit data reception mode. Otherwise, the link operates in 16 bit mode and data signals D16..D19 are undefined. The termination must be done just before the Connector with a Resistor (matched to the transmission line) to VTT. {Altera PLD, Translator, Transmission line, Termination to VTT [R4], Connector [J2]}
28	VTT1 [power]	ECL_VCC - 2Volts (typically -2Volts)
29	VTT2 [power]	ECL_VCC - 2Volts (typically -2Volts)
30	DGND1	Digital ground for optics.
31	DGND2	Digital ground for optics.
32	DIV1 [ECL output]	<b>VCO Divider Select</b> pin1. This pin together with pin DIV0 program the VCO divider chain to operate at full speed, half speed, quarter speed or one-eighth speed.

		{Jumper to Ground [J3], Connector [J2]}
33	ERROR [ECL input]	<b>Received Data Error:</b> asserted when is received a frame that does not correspond to either a valid Data, Control, or Fill frame encoding. When FLAGSEL is not active, the Hewlett Packard Rx chip also tests for strict alternation of flag bits during data frames. A flag bit alternation error will also cause an ERROR indication. {Connector [J2], 100Ω Transmission line (L<10cm), 300Ω Termination to VTT [R1], Translator [U3], Altera PLD}
34	D1 [ECL input]	{Connector [J2], 100Ω Transmission line, 300Ω Termination to VTT [R1], Translator [U3], Altera PLD}
35	D3 [ECL input]	{Connector [J2], 100Ω Transmission line, 300Ω Termination to VTT [R1], Translator [U3], Altera PLD}
36	D5 [ECL input]	{Connector [J2], 100Ω Transmission line, 300Ω Termination to VTT [R1], Translator [U3], Altera PLD}
37	D7 [ECL input]	{Connector [J2], 100Ω Transmission line, 300Ω Termination to VTT [R1], Translator [U3], Altera PLD}
38	VCC4 [power]	ECL_VCC (Connected to Ground)
39	D10 [ECL input]	{Connector [J2], 100Ω Transmission line, 300Ω Termination to VTT [R2], Translator [U1], Altera PLD}
40	D12 [ECL input]	{Connector [J2], 100Ω Transmission line, 300Ω Termination to VTT [R2], Translator [U1], Altera PLD}
41	D14 [ECL input]	{Connector [J2], 100Ω Transmission line, 300Ω Termination to VTT [R2], Translator [U1], Altera PLD}
42	D16 [ECL input]	{Connector [J2], 100Ω Transmission line, 300Ω Termination to VTT [R2], Translator [U1], Altera PLD}
43	D18 [ECL input]	{Connector [J2], 100Ω Transmission line, 300Ω Termination to VTT [R3], Translator [U2], Altera PLD}
44	VCC5 [power]	ECL_VCC (Connected to Ground)
45	CAV* [ECL input]	<b>Control Frame Available Output:</b> This Active-low signal indicates that the Hewlett Packard Rx chip data outputs are receiving Control Frames. False CAV indications may be generated during link startup. {Connector [J2], 100Ω Transmission line, 300Ω Termination to VTT [R3], Translator [U2], Altera PLD}
46	LINKRDY* [ECL input]	<b>Link Ready Indicator.</b> This active-low signal is a re-timed version of ACTIVE signal. The LINKRDY* signal is normally driven by the HP chip's Rx State Machine output. LINKRDY* then indicates that the startup sequence is complete and that the data and control indications are valid. {Connector [J2], 100Ω Transmission line, 300Ω Termination to VTT [R3], Translator [U2], Altera PLD}
47	LOOPEN [ECL]	<b>Loop back Control.</b> When asserted, this signal causes the loop back data inputs (LIN, LIN*) to be used instead of the normal data inputs (DIN, DIN*). The G-Link chip Rx state machine normally controls this input of the HP chip. {Connector [J2], Floating}
48	ACTIVE [ECL]	This signal is driven by the G-Link chip's Rx state machine output (PACTIVE pin). The ACTIVE signal is internally re-timed (in the HP chip) by STRBOUT and presented to the user as LINKRDY signal. This is how the G-Link chip Rx state machine signals the user that the startup sequence is complete. {Connector [J2], connection to STAT1}
49	FDIS [ECL]	<b>Frequency Detector Disable Input.</b> When active this input (HP chip) disable the Rx PLL Frequency detector and enable a phase detector. The frequency detector is used during the start-up sequence to acquire wide-band lock on Fill Frames, but must be disabled prior to sending data patterns. The G-Link Rx state machine normally controls this input. {Connector [J2], connection to STAT1}
50	VCC6 [power]	ECL_VCC (Connected to Ground)
51	EQEN	<b>Enable Input for Cable Equalization.</b> When asserted this signal activates the

	[ECL]	cable equalization amplifier on the DIN, DIN* serial data inputs. {Connector [J2], Floating}
52	RX_OPT_PWR	Not for Host use. {Connector [J2], Floating}
53	RX_SYS2 [TTL input/output]	Internal signal. {Connector [J2], Jumper, Ground}
54	RX_SYS1 [TTL input/output]	internal signal {Connector [J2], Jumper, Ground}
55	FLAGSEL [ECL output]	<b>Flag bit mode select.</b> When this output is high, the extra FLAG bit input is effectively an extra transparent data bit. Otherwise, the FLAG bit is checked for alternation during data frames. Any break in strict alternation results in an ERROR indication to the user. {Altera PLD, Translator [U4], Transmission line, Termination to VTT [R4], Connector [J2]}
56	VEE1 [power]	ECL_VEE (typically -5V)
57	VEE2 [power]	ECL_VEE (typically -5V)
58	SMC1* [ECL output]	<b>State Machine Reset Input.</b> Each of the SMC1* and SMC2* (active low) signals reset the Rx state machine to the initial startup state. This initiates a complete PLL restart and handshake at both ends of the duplex link. Normally, SMC0* is connected to power-up reset circuit or a host system reset signal. The SMC1* pin is normally connected to the Tx LOCKED output. The LOCKED signal holds the state machine in the start-up state until the Tx PLL is locked. (same as SMCRST1* on HP chip data sheet). {Altera PLD, Translator [U4], Transmission line, Termination to VTT [R4], Connector [J2]}
59	SMC0* [ECL output]	<b>State Machine Reset Input.</b> Each of the SMC1* and SMC2* (active low) signals reset the Rx state machine to the initial startup state. This initiates a complete PLL restart and handshake at both ends of the duplex link. Normally, SMC0* is connected to power-up reset circuit or a host system reset signal. The SMC1* pin is normally connected to the Tx LOCKED output. The LOCKED signal holds the state machine in the start-up state until the Tx PLL is locked. (same as SMCRST1* on HP chip data sheet). {RESET line, Translator [U4], Transmission line, Termination to VTT [R4], Connector [J2]}
60	VCC7 [power]	ECL_VCC (Connected to Ground)

Table 11:G-Link Receiver Board FRC-1101-1 Connector pinout

## 5.4 PLD Pinout

### GSTM G-Link Receiver Adapter daughter card (former Board Test 1)

(Revision 12/05/96)

ALTERA PLD

Active serial configuration with the Altera EPROM (EPC1064LC20), two possible options (using the jumper J7):

- normal
- automatic reconfiguration on error

Pin Number	Info	Pin Number	Info
<b>1</b> (left)	(DCLK) {Output. To pin "DCLK" of the EPROM [U7]}	<b>81</b> (right)	(VCCINT) {to VCC (+5Volt)}
<b>2</b>	(No Connect, N.C.) {Floating}	<b>82</b>	(No Connect, N.C.) {Floating}
<b>3</b>	(No Connect, N.C.) {Floating}	<b>83</b>	(No Connect, N.C.) {Floating}
<b>4</b>	(CONF_DONE) {to the pin "nCS" of the EPROM [U7], to 1K $\Omega$ pull-up resistor to VCC [R6], to the LEDs Driver [U10]}	<b>84</b>	(MSEL1) {jumper to Ground [J4]} The pins nSP, MSEL0, MSEL1, when connected to Ground select the "Active serial" configuration of the PLD [U6] (using the EPROM [U7]).
<b>5</b>	(Dedicate input) STROBE {Input from the ECL to TTL Translator [U5]}	<b>85</b>	(Dedicate input) DI1. Connected on the PC board to TP1 (pin113) {TP1, trace, termination resistor [R20], DI1}
<b>6</b>	LED2 {Output to LEDs driver [U10]}	<b>86</b>	DAT_R[14] {Output to GSTM R2 port connector [J16]}
<b>7</b>	LED3 {Output to LEDs driver [U10]}	<b>87</b>	DAT_R[9] {Output to GSTM R2 port connector [J16]}
<b>8</b>	FLAGSEL {Output to the TTL to ECL Translator [U4]}	<b>88</b>	DAT_R[8] {Output to GSTM R2 port connector [J16]}
<b>9</b>	M20SEL {Output to the TTL to ECL Translator [U4]}	<b>89</b>	DAT_R[3] {Output to GSTM R2 port connector [J16]}
<b>10</b>	nSMC1 {Output to the TTL to ECL Translator [U4]} Used by the Altera PLD to reset the G-Link receiver.	<b>90</b>	DAT_R[2] {Output to GSTM R2 port connector [J16]}
<b>11</b>	LV_RUN {Input from LVDS to TTL Translator [U8]}	<b>91</b>	TST[19] {to SRC CS Adapter Board connector [J17]}
<b>12</b>	(DATA0) {to the pin "DATA" of the EPROM [U7]}	<b>92</b>	TST[18] {to SRC CS Adapter Board connector [J17]}
<b>13</b>	(GND) {Ground}	<b>93</b>	(GND) {Ground}
<b>14</b>	(GND) {Ground}	<b>94</b>	TST[17] {to SRC CS Adapter Board connector [J17]}
<b>15</b>	LV_ST0 {Output to TTL to LVDS Translator [U9]}	<b>95</b>	TST[16] {to SRC CS Adapter Board connector [J17]}
<b>16</b>	LV_ST1 {Output to TTL to LVDS Translator [U9]}	<b>96</b>	TST[15] {to SRC CS Adapter Board connector [J17]}
<b>17</b>	LV_OK {Output to TTL to LVDS Translator [U9]}	<b>97</b>	TST[14] {to SRC CS Adapter Board connector [J17]}
<b>18</b>	LED4 {Output to LEDs driver [U10]}	<b>98</b>	TST[13] {to SRC CS Adapter Board connector [J17]}
<b>19</b>	LED5 {Output to LEDs driver [U10]}	<b>99</b>	TST[12] {to SRC CS Adapter Board connector [J17]}
<b>20</b>	LED6 {Output to LEDs driver [U10]}	<b>100</b>	(VCCINT) {to VCC (+5Volt)}
<b>21</b>	(VCCINT) {to VCC (+5Volt)}	<b>101</b>	TST[11] {to SRC CS Adapter Board connector [J17]}
<b>22</b>	DIPS1 {Output to pull-up resistor [R18]}	<b>102</b>	TST[10] {to SRC CS Adapter Board connector [J17]}

	and Dip Switch [S1]}		
23	DIPS2 {Output to pull-up resistor [R18] and Dip Switch [S1]}	103	TST[9] {to SRC CS Adapter Board connector [J17]}
24	DIPS3 {Output to pull-up resistor [R18] and Dip Switch [S1]}	104	TST[8] {to SRC CS Adapter Board connector [J17]}
25	DIPS4 {Output to pull-up resistor [R18] and Dip Switch [S1]}	105	TST[7] {to SRC CS Adapter Board connector [J17]}
26	DIPS5 {Output to pull-up resistor [R18] and Dip Switch [S1]}	106	TST[6] {to SRC CS Adapter Board connector [J17]}
27	DIPS6 {Output to pull-up resistor [R18] and Dip Switch [S1]}	<b>107</b>	(GND) {Ground}
<b>28</b>	(GND) {Ground}	<b>108</b>	(GND) {Ground}
29	DIPS7 {Output to pull-up resistor [R18] and Dip Switch [S1]}	109	TST[5] {to SRC CS Adapter Board connector [J17]}
30	DIPS8 {Output to pull-up resistor [R18] and Dip Switch [S1]}	110	TST[4] {to SRC CS Adapter Board connector [J17]}
31	MR_MODE {Input from GSTM R2 port connector [J16]}	111	TST[3] {to SRC CS Adapter Board connector [J17]}
32	P_CNTRL0 (Input from GSTM R2 port connector [J16])	112	TST[2] {to SRC CS Adapter Board connector [J17]}
33	GPS0 (Output to GSTM R2 port connector [J16])	113	TP1 Connected on the PC board to DI1 (pin85) {TP1, trace, termination resistor [R20], DI1}
34	DAT_R[21] (FF) (Output to GSTM R2 port connector [J16])	114	TP2 {to a test point [P2]}
35	DAT_R[20] (FLAG) (Output to GSTM R2 port connector [J16])	115	TP3 {to a test point [P3]}
36	(Dedicate input) SYS_CLK. {Input from GSTM R2 port connector} {connector [J16], trace, termination resistor [R21], SYS_CLK}	116	(Dedicate input) TST[1]. From SRC CS Adapter Board connector. {connector [J17], trace, termination resistor [R22], TST[1]}
<b>37</b>	(nSTATUS) {1K $\Omega$ resistor to VCC [R7] and a Jumper [J7] to the pin "OE" of the EPROM [U7]}	<b>117</b>	(MSEL0) {jumper to Ground [J5]} The pins nSP, MSEL0, MSEL1, when connected to Ground select the "Active serial" configuration of the PLD [U6] (using the EPROM [U7]).
<b>38</b>	(No Connect, N.C.) {Floating}	<b>118</b>	(No Connect, N.C.) {Floating}
<b>39</b> (left)	(No Connect, N.C.) {Floating}	<b>119</b>	(No Connect, N.C.) {Floating}
<b>40</b> (bottom)	(nCONFIG) {to the reset line (active low). A jumper [J7] to the pin "OE" of the EPROM [U7]}	<b>120</b> (right)	(nSP) {jumper to Ground [J6]} The pins nSP, MSEL0, MSEL1, when connected to Ground select the "Active serial" (AS) configuration of the PLD [U6] (using the EPROM [U7]).
<b>41</b>	(VCCINT) {to VCC (+5Volt)}	<b>121</b> (top)	(VCCINT) {to VCC (+5Volt)}
42	P_CNTRL1 {Input from GSTM R2 port connector [J16]}	122	D[3] (former TP4) {Input from the ECL to TTL Translator [U3]} {to a test point [P4]} Required PCB modification.
43	P_CNTRL2 {Input from GSTM R2 port connector [J16]}	123	ERROR {Input from the ECL to TTL Translator [U3]}
44	DAT_R[25] (START_FIFO*) {Output to GSTM R2 port connector [J16]}	124	D[0] {Input from the ECL to TTL Translator [U3]}
45	DAT_R[24] (STAT0) {Output to GSTM R2 port connector [J16]}	125	D[1] {Input from the ECL to TTL Translator [U3]}
<b>46</b>	(GND) {Ground}	<b>126</b>	(GND) {Ground}

47	P_STATUS1 {Output to GSTM R2 port connector [J16]}	127	D[2] {Input from the ECL to TTL Translator [U3]}
48	GPS1 {Output to GSTM R2 port connector [J16]}	<b>128</b>	SDOUT (former D[3] (now pin122)) {Reserved Configuration Output, drives out during Command Mode} Required PCB modification.
49	DAT_R[23] (DAV*) {Output to GSTM R2 port connector [J16]}	129	D[4] {Input from the ECL to TTL Translator [U3]}
50	DAT_R[22] (CAV*) {Output to GSTM R2 port connector [J16]}	130	D[5] {Input from the ECL to TTL Translator [U3]}
51	DAT_R[19] (D[19]) {Output to GSTM R2 port connector [J16]}	131	D[6] {Input from the ECL to TTL Translator [U3]}
52	DAT_R[18] (D[18]) {Output to GSTM R2 port connector [J16]}	132	D[7] {Input from the ECL to TTL Translator [U3]}
<b>53</b>	(VCCINT) {to VCC (+5Volt)}	<b>133</b>	(VCCINT) {to VCC (+5Volt)}
54	/CR_CNTRL {Input from GSTM R2 port connector [J16]}	134	D[8] {Input from the ECL to TTL Translator [U1]}
55	DAT_I/O[3] (NOT USED) {Output to GSTM R2 port connector [J16]}	135	D[9] {Input from the ECL to TTL Translator [U1]}
56	DAT_R[17] (D[17]) {Output to GSTM R2 port connector [J16]}	136	D[10] {Input from the ECL to TTL Translator [U1]}
57	DAT_R[16] (D[16]) {Output to GSTM R2 port connector [J16]}	137	D[11] {Input from the ECL to TTL Translator [U1]}
58	DAT_R[13] (D[13]) {Output to GSTM R2 port connector [J16]}	138	D[12] {Input from the ECL to TTL Translator [U1]}
59	DAT_R[12] (D[12]) {Output to GSTM R2 port connector [J16]}	139	D[13] {Input from the ECL to TTL Translator [U1]}
<b>60</b>	(GND) {Ground}	<b>140</b>	(GND) {Ground}
61	DAT_I/O[2] (NOT USED) {Output to GSTM R2 port connector [J16]}	141	D[14] {Input from the ECL to TTL Translator [U1]}
62	DAT_I/O[1] (LINKREADY*) {Output to GSTM R2 port connector [J16]}	142	D[15] {Input from the ECL to TTL Translator [U1]}
63	DAT_R[11] (D[11]) {Output to GSTM R2 port connector [J16]}	143	D[16] {Input from the ECL to TTL Translator [U1]}
64	DAT_R[10] (D[10]) {Output to GSTM R2 port connector [J16]}	144	D[17] {Input from the ECL to TTL Translator [U2]}
65	DAT_R[7] (D[7]) {Output to GSTM R2 port connector [J16]}	145	D[18] {Input from the ECL to TTL Translator [U2]}
66	DAT_R[6] (D[6]) {Output to GSTM R2 port connector [J16]}	146	D[19] {Input from the ECL to TTL Translator [U2]}
<b>67</b>	(VCCINT) {to VCC (+5Volt)}	<b>147</b>	(VCCINT) {to VCC (+5Volt)}
68	TEST_BIT0 {Input from GSTM R2 port connector [J16]}	<b>148</b>	(No Connect, N.C.) {Floating}
69	TEST_BIT1 {Input from GSTM R2 port connector [J16]}	149	FLAG {Input from the ECL to TTL Translator [U2]}
<b>70</b>	(No Connect, N.C.) {Floating}	150	FF {Input from the ECL to TTL Translator [U2]}
71	DAT_R[5] (D[5]) {Output to GSTM R2 port connector [J16]}	151	CAV* {Input from the ECL to TTL Translator [U2]}
72	DAT_R[4] (D[4]) {Output to GSTM R2 port connector [J16]}	152	DAV* {Input from the ECL to TTL Translator [U2]}
73	DAT_R[1] (D[1]) {Output to GSTM R2 port connector [J16]}	153	LINKRDY* {Input from the ECL to TTL Translator [U2]}
74	DAT_R[0] (D[0]) {Output to GSTM R2 port connector [J16]}	154	STAT0 {Input from the ECL to TTL Translator [U2]}

<b>75</b>	(GND) {Ground}	<b>155</b>	(GND) {Ground}
<b>76</b>	(CLKUSR) {to a test point}	156	TP5 {to a test point [P5]}
77	P_STATUS2 {Output to GSTM R2 port connector [J16]}	157	TP6 {to a test point [P6]}
78	DAT_I/O[0] (ERROR) {Output to GSTM R2 port connector [J16]}	158	TP7 {to a test point [P7]}
79	DAT_R[15] (D[15]) {Output to GSTM R2 port connector [J16]}	159	TP8 {to a test point [P8]}
<b>80</b> (bottom)	(VCCINT) {to VCC (+5Volt)}	<b>160</b> (top)	(VCCINT) {to VCC (+5Volt)}

Table 12: PINOUT of the ALTERA PLD used on the GSTM G-Link Receiver Adapter daughter card

Pin Number	Info	Pin Number	Info
<b>1</b>	(N.C.) {Floating}	<b>11</b>	(N.C.) {Floating}
<b>2</b>	(DATA) {to "DATA0" of the ALTERA PLD [U6]}	<b>12</b>	(nCASC) {Floating}
<b>3</b>	(N.C.) {Floating}	<b>13</b>	(N.C.) {Floating}
<b>4</b>	(DCLK) {to "DCLK" of the ALTERA PLD [U6]}	<b>14</b>	(N.C.) {Floating}
<b>5</b>	(N.C.) {Floating}	<b>15</b>	(N.C.) {Floating}
<b>6</b>	(N.C.) {Floating}	<b>16</b>	(N.C.) {Floating}
<b>7</b>	(N.C.) {Floating}	<b>17</b>	(N.C.) {Floating}
<b>8</b>	(OE) {jumper [J7] to: "nCONFIG", "nSTATUS" of the ALTERA PLD [U6]}	<b>18</b>	(VCC) {to VCC (+5Volt)}
<b>9</b>	(nCS) {to "CONF_DONE" of the ALTERA PLD [U6] and 1K $\Omega$ resistor [R6] to VCC}	<b>19</b>	(N.C.) {Floating}
<b>10</b>	(GND) {Ground}	<b>20</b>	(VCC) {to VCC (+5Volt)}

Table 13: PINOUT of the ALTERA Configuration EPROM (EPC1064LC20, 20-pin PLCC package) used on the GSTM G-Link Receiver Adapter daughter card

**GSTM SRC Command Status Adapter daughter card (former Board Test2)**

(Revision 12/31/96)

ALTERA PLD

Active serial configuration with the Altera EPROM (EPC1064LC20), two possible options (using the jumper J5):

- normal
- automatic reconfiguration on error

Pin Number	Info	Pin Number	Info
<b>1</b> (left)	(DCLK) {Output. To pin "DCLK" of the EPROM [U2]}	<b>81</b> (right)	(VCCINT) {to VCC (+5Volt)}
<b>2</b>	(No Connect, N.C.) {Floating}	<b>82</b>	(No Connect, N.C.) {Floating}
<b>3</b>	(No Connect, N.C.) {Floating}	<b>83</b>	(No Connect, N.C.) {Floating}
<b>4</b>	(CONF_DONE) {to the pin "nCS" of the EPROM [U2], to 1K $\Omega$ pull-up resistor [R17] to VCC, to the LEDs Driver [U10]}	<b>84</b>	(MSEL1) {jumper [J2] to Ground} The pins nSP, MSEL0, MSEL1, when connected to Ground select the "Active serial" configuration of the PLD [U1] (using the EPROM [U2]).
<b>5</b>	(Dedicate input) CC_STROBE {Input from the LVDS Receiver [U6]}. Terminated near the pin with 100 Ohm resistor [R26].	<b>85</b>	(Dedicate input) SYS_CLK {Input, from GSTM R1 port connector [J7]}. Terminated near the pin with 100 Ohm resistor [R30].
<b>6</b>	DAT_IO[2] {input/output to GSTM R1 port connector [J7]}	<b>86</b>	DAT_R[9] {Output to GSTM R1 port connector [J7]}
<b>7</b>	DAT_IO[3] {input/output to GSTM R1 port connector [J7]}	<b>87</b>	DAT_R[12] {Output to GSTM R1 port connector [J7]}
<b>8</b>	TST[1] {to GSTM G-Link RA Board connector [J8]}	<b>88</b>	DAT_R[13] {Output to GSTM R1 port connector [J7]}
<b>9</b>	TST[2] {to GSTM G-Link RA Board connector [J8]}	<b>89</b>	DAT_R[18] {Output to GSTM R1 port connector [J7]}
<b>10</b>	TST[3] {to GSTM G-Link RA Board connector [J8]}	<b>90</b>	DAT_R[19] {Output to GSTM R1 port connector [J7]}
<b>11</b>	DAT_IO[4] {input/output to GSTM R1 port connector [J7]}	<b>91</b>	TP3 {to a test point}
<b>12</b>	(DATA0) {to the pin "DATA" of the EPROM [U2]}	<b>92</b>	TP4 {to a test point}
<b>13</b>	(GND) {Ground}	<b>93</b>	(GND) {Ground}
<b>14</b>	(GND) {Ground}	<b>94</b>	TP5 {to a test point}
<b>15</b>	DAT_IO[5] {input/output to GSTM R1 port connector [J7]}	<b>95</b>	LED6 (Output to LEDs driver [U10])
<b>16</b>	DAT_IO[6] {input/output to GSTM R1 port connector [J7]}	<b>96</b>	LED5 (Output to LEDs driver [U10])
<b>17</b>	DAT_IO[7] {input/output to GSTM R1 port connector [J7]}	<b>97</b>	LED4 (Output to LEDs driver [U10])
<b>18</b>	DAT_IO[8] {input/output to GSTM R1 port connector [J7]}	<b>98</b>	LED3 (Output to LEDs driver [U10])
<b>19</b>	TP1 {to a test point}	<b>99</b>	LED2 (Output to LEDs driver [U10])
<b>20</b>	DIPS1 (Output to pull-up resistor [RP1] and Dip Switch [S1])	<b>100</b>	(VCCINT) {to VCC (+5Volt)}
<b>21</b>	(VCCINT) {to VCC (+5Volt)}	<b>101</b>	TP6 {to a test point}

22	DIPS2 (Output to pull-up resistor [RP1] and Dip Switch [S1])	102	TP7 {to a test point}
23	DIPS3 (Output to pull-up resistor [RP1] and Dip Switch [S1])	103	TP8 {to a test point}
24	DIPS4 (Output to pull-up resistor [RP1] and Dip Switch [S1])	104	TP9 {to a test point}
25	DIPS5 (Output to pull-up resistor [RP1] and Dip Switch [S1])	105	TP10 {to a test point}
26	DIPS6 (Output to pull-up resistor [RP1] and Dip Switch [S1])	106	TP11 {to a test point}
27	DIPS7 (Output to pull-up resistor [RP1] and Dip Switch [S1])	<b>107</b>	(GND) {Ground}
<b>28</b>	(GND) {Ground}	<b>108</b>	(GND) {Ground}
29	DIPS8 (Output to pull-up resistor [RP1] and Dip Switch [S1])	109	TP12 {to a test point}
30	TP2 {to a test point}	110	TP13 {to a test point}
31	TST[4] {to GSTM G-Link RA Board connector [J8]}	111	P_CNTRL1 {Input from GSTM R1 port connector [J7]}
32	TST[7] {to GSTM G-Link RA Board connector [J8]}	112	P_CNTRL0 {Input from GSTM R1 port connector [J7]}
33	TST[8] {to GSTM G-Link RA Board connector [J8]}	113	MR_MODE {Input from GSTM R1 port connector [J7]}
34	DAT_R[2] {Output to GSTM R1 port connector [J7]}	114	/CR_CNTRL {Input from GSTM R1 port connector [J7]}
35	DAT_R[3] {Output to GSTM R1 port connector [J7]}	115	GPS1 {Output to GSTM R1 port connector [J7]}
36	(Dedicate input) STROBE {Input from GSTM G-Link RA Board connector [8]}. Terminated near the pin with 100 Ohm resistor [R27].	116	(Dedicate input) Dedicated_IN. Connected on the PC board to TP13 (pin110) {TP13, trace, termination resistor [R29], Dedicated_IN }
<b>37</b>	(nSTATUS) {1K $\Omega$ resistor [R18] to VCC and a Jumper [J5]to the pin "OE" of the EPROM [U2]}	<b>117</b>	(MSEL0) {jumper [J3] to Ground} The pins nSP, MSEL0, MSEL1, when connected to Ground select the "Active serial" configuration of the PLD [U1] (using the EPROM [U2]).
<b>38</b>	(No Connect, N.C.) {Floating}	<b>118</b>	(No Connect, N.C.) {Floating}
<b>39</b> (left)	(No Connect, N.C.) {Floating}	<b>119</b>	(No Connect, N.C.) {Floating}
<b>40</b> (bottom)	(nCONFIG) {to the reset line (active low). A jumper [J5] to the pin "OE" of the EPROM [U2]}	<b>120</b> (right)	(nSP) {jumper [J4] to Ground} The pins nSP, MSEL0, MSEL1, when connected to Ground select the "Active serial" (AS) configuration of the PLD [U1] (using the EPROM [U2]).
<b>41</b>	(VCCINT) {to VCC (+5Volt)}	<b>121</b> (top)	(VCCINT) {to VCC (+5Volt)}
42	TST[5] {to GSTM G-Link RA Board connector [J8]}	122	GPS0 {Output to GSTM R1 port connector [J7]}
43	TST[6] {to GSTM G-Link RA Board connector [J8]}	123	P_STATUS2 {Output to GSTM R1 port connector [J7]}
44	TST[9] {to GSTM G-Link RA Board connector [J8]}	124	SB_STAT[9] {Output to the TTL to LVDS Translator [U9]}
45	TST[10] {to GSTM G-Link RA Board connector [J8]}	125	SB_STAT[8] {Output to the TTL to LVDS Translator [U9]}
<b>46</b>	(GND) {Ground}	<b>126</b>	(GND) {Ground}
47	TST[11] {to GSTM G-Link RA Board	127	SB_STAT[7] {Output to the TTL to LVDS Translator

	connector [J8]}		[U8]}
48	TST[12] {to GSTM G-Link RA Board connector [J8]}	128	SB_STAT[6] {Output to the TTL to LVDS Translator [U8]}. Pin 128 is Reserved to SDOOUT in the Configuration Mode. This mean at power up this pin will drive a signal (SDOOUT).
49	DAT_R[0] {Output to GSTM R1 port connector [J7]}	129	SB_STAT[5] {Output to the TTL to LVDS Translator [U8]}
50	DAT_R[1] {Output to GSTM R1 port connector [J7]}	130	SB_STAT[4] {Output to the TTL to LVDS Translator [U8]}
51	DAT_R[4] {Output to GSTM R1 port connector [J7]}	131	SB_STAT[3] {Output to the TTL to LVDS Translator [U7]}
52	DAT_R[5] {Output to GSTM R1 port connector [J7]}	132	SB_STAT[2] {Output to the TTL to LVDS Translator [U7]}
<b>53</b>	(VCCINT) {to VCC (+5Volt)}	<b>133</b>	(VCCINT) {to VCC (+5Volt)}
54	TST[13] {to GSTM G-Link RA Board connector [J8]}	134	SB_STAT[1] {Output to the TTL to LVDS Translator [U7]}
55	TST[14] {to GSTM G-Link RA Board connector [J8]}	135	SB_STAT[0] {Output to the TTL to LVDS Translator [U7]}
56	DAT_R[6] {Output to GSTM R1 port connector [J7]}	136	P_STATUS1 {Output to GSTM R1 port connector [J7]}
57	DAT_R[7] {Output to GSTM R1 port connector [J7]}	137	P_STATUS0 {Output to GSTM R1 port connector [J7]}
58	DAT_R[10] {Output to GSTM R1 port connector [J7]}	138	CC_MSG[11] {Input from the LVDS to TTL Translator [U5]}
59	DAT_R[11] {Output to GSTM R1 port connector [J7]}	139	CC_MSG[10] {Input from the LVDS to TTL Translator [U5]}
<b>60</b>	(GND) {Ground}	<b>140</b>	(GND) {Ground}
61	TST[15] {to GSTM G-Link RA Board connector [J8]}	141	CC_MSG[9] {Input from the LVDS to TTL Translator [U5]}
62	TST[16] {to GSTM G-Link RA Board connector [J8]}	142	CC_MSG[8] {Input from the LVDS to TTL Translator [U5]}
63	TST[17] {to GSTM G-Link RA Board connector [J8]}	143	CC_MSG[7] {Input from the LVDS to TTL Translator [U4]}
64	TST[18] {to GSTM G-Link RA Board connector [J8]}	144	CC_MSG[6] {Input from the LVDS to TTL Translator [U4]}
65	DAT_R[14] {Output to GSTM R1 port connector [J7]}	145	CC_MSG[5] {Input from the LVDS to TTL Translator [U4]}
66	DAT_R[15] {Output to GSTM R1 port connector [J7]}	146	CC_MSG[4] {Input from the LVDS to TTL Translator [U4]}
<b>67</b>	(VCCINT) {to VCC (+5Volt)}	<b>147</b>	(VCCINT) {to VCC (+5Volt)}
68	TST[19] {to GSTM G-Link RA Board connector [J8]}	<b>148</b>	(No Connect, N.C.) {Floating}
69	TEST_BIT1 {Input from GSTM R1 port connector [J7]}	149	CC_MSG[3] {Input from the LVDS to TTL Translator [U3]}
<b>70</b>	(No Connect, N.C.) {Floating}	150	CC_MSG[2] {Input from the LVDS to TTL Translator [U3]}
71	DAT_R[16] {Output to GSTM R1 port connector [J7]}	151	CC_MSG[1] {Input from the LVDS to TTL Translator [U3]}
72	DAT_R[17] {Output to GSTM R1 port connector [J7]}	152	CC_MSG[0] {Input from the LVDS to TTL Translator [U3]}
73	DAT_R[20] {Output to GSTM R1 port connector [J7]}	153	DAT_IO[0] {input/output to GSTM R1 port connector [J7]}
74	DAT_R[21] {Output to GSTM R1 port	154	DAT_IO[1] {input/output to GSTM R1 port connector

	connector [J7]}		[J7]}
<b>75</b>	(GND) {Ground}	<b>155</b>	(GND) {Ground}
<b>76</b>	(CLKUSR) {to a test point [P34]}	156	Reserved1 {to GSTM R1 port connector [J7]}
77	TEST_BIT0 {Input from GSTM R1 port connector [J7]}	157	DAT_R[24] {Output to GSTM R1 port connector [J7]}
78	P_CNTRL2 {Input from GSTM R1 port connector [J7]}	158	DAT_R[23] {Output to GSTM R1 port connector [J7]}
79	DAT_R[8] {Output to GSTM R1 port connector [J7]}	159	DAT_R[22] {Output to GSTM R1 port connector [J7]}
<b>80</b> (bottom)	(VCCINT) {to VCC (+5Volt)}	<b>160</b> (top)	(VCCINT) {to VCC (+5Volt)}

Table 14: PINOUT of the ALTERA PLD used on the GSTM SRC Command Status Adapter daughter card

Pin Number	Info	Pin Number	Info
<b>1</b>	(N.C.) {Floating}	<b>11</b>	(N.C.) {Floating}
<b>2</b>	(DATA) {to "DATA0" of the ALTERA PLD [U1]}	<b>12</b>	(nCASC) {Floating}
<b>3</b>	(N.C.) {Floating}	<b>13</b>	(N.C.) {Floating}
<b>4</b>	(DCLK) {to "DCLK" of the ALTERA PLD [U1]}	<b>14</b>	(N.C.) {Floating}
<b>5</b>	(N.C.) {Floating}	<b>15</b>	(N.C.) {Floating}
<b>6</b>	(N.C.) {Floating}	<b>16</b>	(N.C.) {Floating}
<b>7</b>	(N.C.) {Floating}	<b>17</b>	(N.C.) {Floating}
<b>8</b>	(OE) {jumper [J5] to: "nCONFIG", "nSTATUS" of the ALTERA PLD [U1]}	<b>18</b>	(VCC) {to VCC (+5Volt)}
<b>9</b>	(nCS) {to "CONF_DONE" of the ALTERA PLD [U1] and 1K $\Omega$ resistor [R17] to VCC}	<b>19</b>	(N.C.) {Floating}
<b>10</b>	(GND) {Ground}	<b>20</b>	(VCC) {to VCC (+5Volt)}

Table 15: PINOUT of the ALTERA Configuration EPROM (EPC1064LC20, 20-pin PLCC package) used on the GSTM SRC Command Status Adapter daughter card.

## 5.5 PLDs Programming

The Altera Programmable Logic Devices (PLDs) on both boards are programmed using two configurations EPROMs. The description of the logic implemented with these devices is written in AHDL (Altera Hardware Description Language). The AHDL description of the PLDs have been written, compiled, and simulated using the Altera Software (MAX+PLUSII). The result of the compilation are the files (with extension: “.POF”) used to burn the two configuration EPROM (Altera EPC1064, 20pin PLCC, One Time Programmable package). The Altera EPROM has been burned using a DATA I/O Programmer. The programming specification are the following:

- Manufacturer: Altera
- Device type: 1064-PL (POF)
- I/O Translation Format: Altera POF

Note: In the Revision 1 of the G-Link RA design could be used either the 20pin PLCC or the 8pin PDIP packages. The 8pin PDIP socket allow to use the Atmel AT17C65 configuration EEPROM (8pin PDIP package, pin compatible with the Altera EPC1064) [\[Ref. 28\]](#). The advantage is that the AT17C65 could easily be erased and reprogrammed.

## 5.6 Timing Diagrams

## 5.7 Glossary

### **Fiber-Optic Interface Board (FIB) [\[Ref. 4\]](#):**

Receive and process the data from 10 HDI links

On a HDI the data rate is 26.5 Mbyte/sec.

The FIB is a 9U x 400 VME card, which interfaces to a customized J3 backplane and the J1 VMEbus backplane. It is one of the modules designed to control and readout the SVX-III chips. The FIB interfaces with FIB Crate Fanout Board over the custom J3 backplane. The FIB Crate Fanout Board receives timing and command information from the Silicon Readout Controller (SRC) from a dedicated Gigabit Fiber-optic Data Link (G-Link) or from the Test Module if it is enabled. The FIB will be used to both control the SVX-III chips and to transfer data to the Level 2 data collection buffers (VMEbus Readout Buffers (VRB) ).

The FIB executes commands from one of three sources:

- Commands delivered by the SRC board through the J3 backplane.
- Commands previously stored by the VMEbus CPU inside the Command FIFO.
- Commands executed via selectable bits of the FIB’s Control Register (these may be limited).

TFIB ARCHITECTURE CHANGE:

The original TFIB issued micro-commands to the Test Port Card. The word “micro-commands” referred specifically to the sequence of bits that the TFIB-CT sends to the Test Port Card controller (TPC-CT). The Test Port Card controller has been eliminated, in favor of a much simpler control output generator.

When the FIB executes commands, they are executed synchronously with the PC. The FIB interprets these in-coming commands and delivers encoded control information to the PC. The state/control information is translated on the PC and generates the logic levels to control the internal features of the SVX-III chips. One PC can control up to five chains of SVX-III chips, which are mounted on a hybrid. These hybrids are connected to the PC through the High-Density Interconnect (HDI) cable.

**Command Flow:**

The following is the flow of commands and clocks from the SRC to the SVX-III chips.

- The SRC sends a 53 MHz clock (Master Clock), timing signals, and commands to the FIB Crate Fanout Board via a dedicated G-Link fiber.
- The FIB Crate Fanout Board distributes the 53 MHz clock and SRC commands through the J3 backplane.
- The FIB interprets the commands from the SRC and sends the SVX-III clocks (FE\_CLK, BE\_CLK, L1A), the Control Clock (C\_CLK), and the encoded control information (C[3:0]) to PC using low voltage differential levels. Note these drivers are on the FIB/PC transition module.
- The PC controller interprets the encoded control information using the Control Clock (C\_CLK) and delivers the proper CMOS logical levels to the SVX-III chips through the HDI.

The clock sequences for the SVX-III chips are generated directly by the FIB. These clocks are fanned out by the PC to the five HDIs.

**Data Flow:**

The data flow from the SVX-III chips travels via the following path:

- SVX-III chips transmit the data to the PC, through the HDI, using CMOS levels (single ended).
- The PC converts these signals, places them on a parallel optical link, and transmits the data to the TFIB through five 9 bit parallel optical links (8 bits of data and a Data Valid signal). Note: these receivers are on the FIB/PC transition module, which will be described, in a future document.
- The FIB board accepts data from ten of these HDI links.
- Data from the HDI is processed (header frames and End Of Records added) and then transferred to the Level 2 buffers (VMEbus Readout Buffer (VRB) modules) and Silicon Vertex Trigger (SVT) system buffers (FIFO).

**FIB Crate [Ref. 19]:**

VME Crate that houses the FIBs.

There is a special J3 backplane used by the System Controller to drive the buffer number for event readout and scan, and to monitor operational status.

#### **FIB Crate Fanout Board [Ref. 5]:**

The FIB Fanout Board is a 9Ux400 VME card, which resides in a Fiber Interface Board (FIB) crate. The FIB Fanout interfaces to a customized J3 backplane, the Silicon Readout Controller (SRC) module, and the VMEbus backplane. There is a single FIB Fanout board in slot 15 of each FIB crate. The FIB Fanout board receives commands and timing signals from the SRC module on a G-Link and places them on the J3 backplane for use by the FIBs. The VME master in the FIB crate configures the FIB Fanout.

#### **G-Link (High Speed Optical Serial Connection) [Ref. 10, 11, 12, 13, 14]:**

#### **GRT [Ref. 20]:**

The GRT is a 9U transition board whose purpose is to receive serial optical data from the SVXII front end and transform them into parallel TTL compatible signals for input to SVX DAQ systems. More specifically, the VRB boards accept the signals. The GRT will reside in the rear of a standard CDF VME DAQ upgrade crate. It passes its signals through the J3 connector at the rear of the crate to VRB module residing in the front of the crate.

#### **Master clock signals [Ref. 20]**

The Research Division Master Clock provides the Master clock signals to the SRC board. Four signals are used by the SRC to provide synchronization between the Tevatron accelerator and the SVX data acquisition system:

- **CDF Clock:** the CDF Master system clock (approximately 53.104 MHz) synchronized to the Tevatron clock. The clock frequency will vary over a small range depending on the beam energy. The clock has a 50% duty cycle.
- **SYNC:** This clock is one seventh of the CDF clock or approximately 7.6 MHz. and has 132 ns. period and 19 ns. duration. It indicates the possible presence of a proton-antiproton bunch crossing as only one out of seven cycles of the CDF clock is defined to contain particles. This clock is active high.
- **BX:** The bunch crossing clock has 132 ns. or 396 ns. period depending on accelerator operating mode and position of bunch gaps. It tags the presence of a proton-antiproton bunch crossing. This clock is active high with 19 ns. duration.
- **BZ:** The bunch zero clock has a duration of 19 ns. and occurs once every revolution of the beam in the ring or at almost a 21 microsecond period. This clock is active high.

#### **Silicon Read-out Controller board (SRC) [Ref. 1]:**

The Silicon Read-out Controller is the controller for SVX. It is a D16 VME (9U x 400 mm VME card format) slave module that mediates upper level commands from the Trigger Supervisor Interface (TSI) to the Fiber Interface Board and VRB, compiles and reports readout status from

the VRB to the TSI, and passes the timing signals from the Master Clock to the FIB and VRB modules.

SRC to TS Commands (on a copper link):

- **DONE** (LVDS active high): indicates a level 2 accepted buffer transfer has completed.
- **Wait** (LVDS active high): indicates the SRC cannot accept any more "accepts" because it is out of scan buffers in the VRB.
- **ERROR** (LVDS active high): indicates a catastrophic error condition in or sensed by the SRC.
- **RACK** (LVDS active high): indicates acknowledgment of a L2 reject.

**TAXI [Ref. 15]:**

Transparent Asynchronous Xmitter-Receiver Interface. Is the name of the communication protocol used by the Advanced Micro Devices (AMD) chip (am7968) used in the communication link between the Silicon Readout Controller (SRC) and the Trigger Supervisor (TS). Further information could be found in the document [TAXI] or at the AMD web site: <http://www.amd.com/> .

**Trigger Supervisor [Ref. 20] :**

The Trigger Supervisor is the master of the readout controllers within the data acquisition system. It issues commands and analyzes the status of all the readout controllers and makes system level decisions.

TS to SRC Commands (on a fiber link):

The trigger supervisor sends two (9-bit) words every 132 ns. The control link between the TS and the SRC is implemented by means of the AMD Am7968-175 TAXI (Transparent Asynchronous Xmitter-Receiver Interface) chip set. TAXI chips provide a simple parallel interface through a high-speed (up to 175MHz) serial link, while maintaining the data bandwidth required by the system.

**VME Bus ReadOut Buffer (VRB) [Ref. 3]:**

The VRB is a single-width 9U VME module that includes VME64 slave capability. The VME interface is used for module initialization, diagnostics and readout of accepted events. The VRB receives data via transition module data links, which are typically serial optical connections, and communicates with the System Controller through the J3 backplane. The VRB can accept input data at a combined rate of up to 600 MBytes/sec on multiple channels. The output rate is limited by VME transfer speeds and by the number of VRB modules sharing the VME bus. To make optimum use of the module, a significant trigger rejection factor between input and output event rates is assumed. The VRB memory is partitionable allowing a trade-off between buffer size and number of buffers. The VRB module normally does not implement its own buffer management, which is delegated to the System Controller module. The main function of the VRB module is to provide Level 2 buffering for the SVX silicon readout system. A set of VRB

modules resides in a VME subrack along with one System Controller or Controller Fanout Module. They communicate via a special J3 backplane used by the System Controller to drive the buffer number for event readout/scan and to monitor operational status. Data received on each link is stored in the buffer pointed to by the readout buffer number supplied by the System Controller.

For the SVX system, the events stored by the VRB are events which have been accepted by the Level 1 trigger and are waiting for a Level 2 accept or reject. For a reject, the buffer is re-used when the System Controller requests an overwrite (i.e. re-uses the buffer number). Events that are accepted by the Level 2 trigger are accessed via the VME interface with the System Controller supplying the scan buffer number. Either of the VRB ports may be programmed to operate in FIFO mode. In this mode the readout and/or scan buffer numbers are incremented automatically. Buffer numbers supplied by the System Controller are ignored. Information normally supplied by the System Controller can also be provided through VME if the control traffic will not interfere with data transfer.

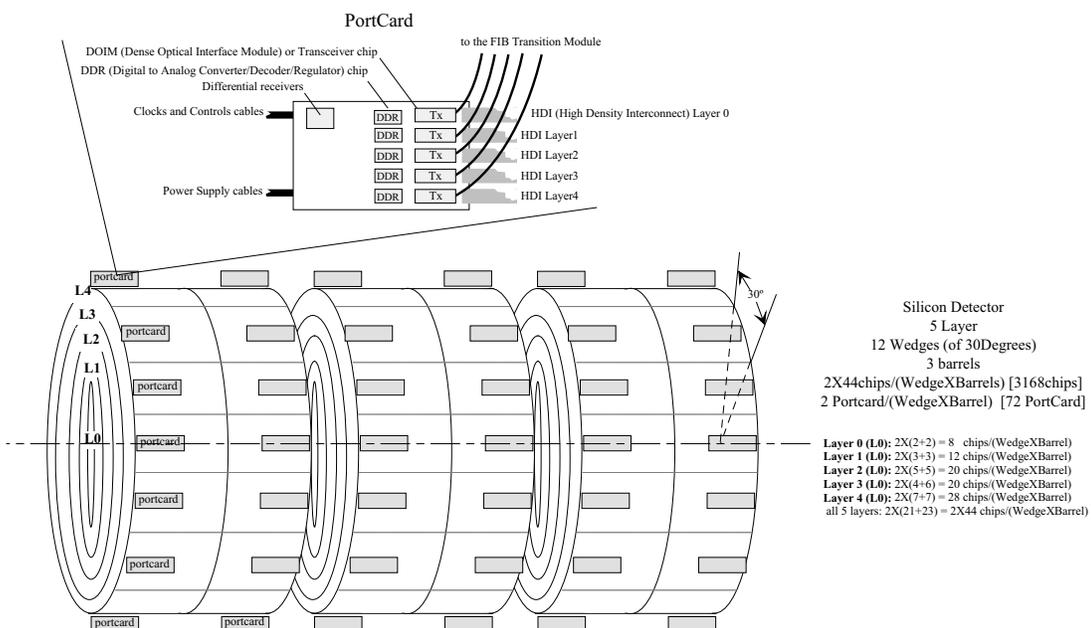
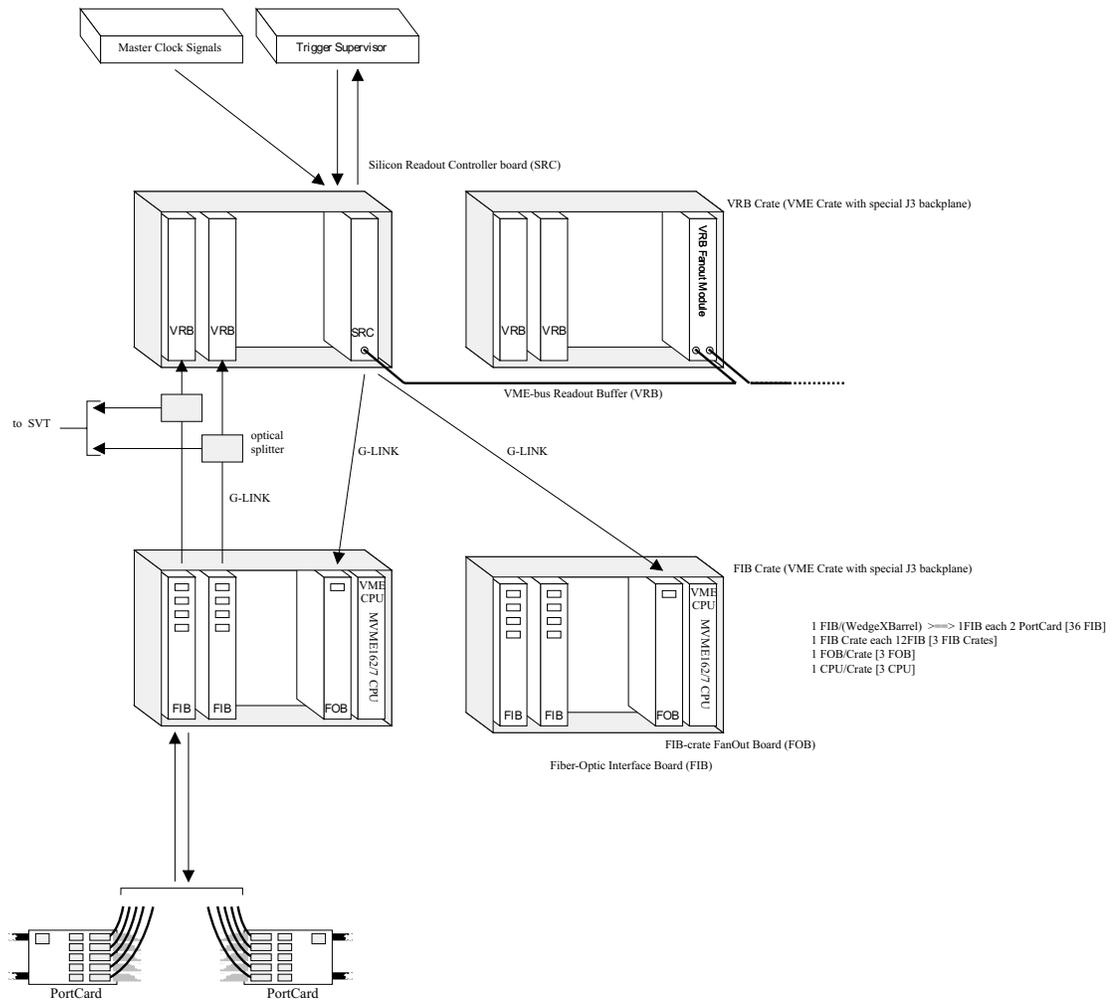
**VRB Crate [Ref. 20]:**

VME Crate that houses the VRBs and SRCs There is a special J3 backplane used by the System Controller to drive the buffer number for event readout/scan and to monitor operational status.

**VRB Fanout Module [Ref. 6]:**

The VRB Fanout Module is a single-width 9U VME module. It resides in slot 15 of an SVX VRB subrack and translates differential PECL signals on the cable to TTL signals on the J3 backplane. There are three groups of signals: a control bus which is used by the System Controller to send commands to the VRBs, a status bus used by the VRBs to signal completion of event readout and various error conditions, and clock drivers used to operate the VRBs synchronously in some.

SVX Data Acquisition System sketch



## 5.8 References

- [1] Colin Gay, John Huth, John Oliver, Maria Spiropolu, “Silicon Readout Controller”. Harvard University Technical Design Report, August 20, 1996. Document (ESE Project index) HAR-SVX-960210.  
Available on Internet: <http://www-ese.fnal.gov/eseproj/index/svxii/svxii.htm> .
- [2] Mingshen Gao, “General System Test Module (Mother Board)”, April 29, 1996. Fermilab Document #ESE-SVX-960126.  
Available on Internet: <http://www-ese.fnal.gov/eseproj/index/svxii/svxii.htm> .
- [3] Hector Gonzalez, Daniel Mendoza, Mark Bowden, Ted Zmuda, Marvin Johnson, Ed Barsotti, “VME Readout Buffer”. Fermilab, Universidad de Los Andes, June 26 1996. Fermilab Document # ESE-SVX-950719.  
Available on Internet: <http://www-ese.fnal.gov/eseproj/index/svxii/svxii.htm> .
- [4] Kerry Woodbury, “Fiber Interface Board”, January 10, 1997, Fermilab Document # ESE-SVX-951010.  
Available on Internet: <http://www-ese.fnal.gov/eseproj/index/svxii/svxii.htm> .
- [5] Ken Treptow, Kerry Woodbury, Ed Barsotti, Sergio Zimmerman, John Anderson, “FIB Crate Fanout Module”, March 29 1996. Fermilab Document #ESE-SVX-951128.  
Available on Internet: <http://www-ese.fnal.gov/eseproj/index/svxii/svxii.htm> .
- [6] Ted Zmuda, Thin Pham, Mark Bowden, “VME Readout Buffer Fanout Module & Link”, June 26 1996. Fermilab Document #ESE-SVX-960418.  
Available on Internet: <http://www-ese.fnal.gov/eseproj/index/svxii/svxii.htm> .
- [7] Vince Pavlicek, “Master Clock/Trigger Supervisor Interface Adapter Card for the General System Test Module”. Fermilab Document #ESE-SVX-960426.  
Available on Internet: <http://www-ese.fnal.gov/eseproj/index/svxii/svxii.htm> .
- [8] Greg Deuerling, “General System Test Module Daughter Card Design Specifications”, June 14 1996. Fermilab Document.
- [9] R.Yarema, “A Beginner Guide to the SVXII”, June 1994. Fermilab Document FERMILAB-TM-1892.  
Available on Internet: <http://www-ese.fnal.gov/eseproj/index/svxii/svxii.htm> .
- [10] Hewlett Packard, “Low Cost Gigabit Rate Transmit/Receive Chip Set”. HDMP-1012 Transmitter, HDMP-1014 Receiver Technical Data. Available on the Hewlett Packard Web site: <http://www.hp.com/HP-COMP/fiber/hdmp1012.html> .
- [11] Finisar Corp., “FRC-1101 Receiver Card” and “FTC-1101 Transmitter Card”. Finisar Internal Document.
- [12] Finisar Corp., “Low Cost, Gigabit Fiber Optic Transmitter/Receiver”. FTM/FRM-8510 Technical Data. Available on the Finisar Web site: <http://www.finisar.com/> .
- [13] Finisar Corp., “Application Note AN-2012”. Interfacing various Gb/s chip sets to FTR-XX10 Transceivers, FTM-XX10 Transmitters and FRM-XX10 Receivers.  
Available on the Finisar Web site: <http://www.finisar.com/> .

- [14] Finisar Corp., “Application Note AN-2010”. Using the built-in test/diagnostic port on FTR-XX10 Transceivers, FTM-XX10 Transmitters and FRM-XX10 Receivers. Available on Internet: <http://www.finisar.com/> .
- [15] Advanced Micro Devices , “TAXIchip Integrated Circuits Transparent Asynchronous Transmitter Receiver Interface, Am7968/Am7969-125, Am7968/Am7968-175, Data Sheet and Technical Manual”, 1994. Document available at the Advanced Micro Devices Web site: <http://www.amd.com/>.
- [16] Paul Horowitz, Winfield Hill, “The Art of Electronics”, 1995, Cambridge University Press. ISBN 0-521-37095-7.
- [17] Altera Corp., “MAX+PLUS II AHDL”. User manual for the Altera Hardware Description Language. Information about Altera products, software and literature are available on the Altera Web site: <http://www.altera.com/> .
- [18] Altera Corp, “1996 Digital Library”. CD ROM containing all current Altera technical literature. Relevant documents: Application Note 33, “Configuring FLEX8000 Devices”; Application Note 36, “Designing with FLEX8000 Devices”; Application Brief 121, “Designing Counters in FLEX8000 Devices”. Information about Altera products, software and literature are available on the Altera Web site: <http://www.altera.com/> .
- [19] Information available on Internet:  
<http://eseserver1/kwtemp/j3&conn.htm>
- [20] Information available on Internet:  
<http://www-ese.fnal.gov/eseproj/index/svxii/svxii.htm>.
- [21] Synergy Semiconductor, 1996 Data Book.  
Some information are available on Internet:  
<http://www.synergyssemi.com/>
- [22] National Semiconductor, Data Sheet of the NS 100325JC.  
Information available on Internet:  
<http://www.national.com/>.
- [23] National Semiconductor, “An Overview of LVDS Technology (Application Note 971)”, “PCB Design Guidelines for LVDS Technology” (Application Note 1035), Data sheets of DS90C031 (LVDS Quad CMOS Differential Line Driver) and of DS90C032 (LVDS Quad CMOS Differential Line Receiver).  
Information available on Internet:  
<http://www.national.com/>.
- [24] Texas Instrument, Data Sheet of SN74ALS1004 (HEX Inverting Drivers).  
Information available on Internet:  
<http://www.ti.com/sc/docs/schome.htm>.
- [25] AMP Inc., Data Sheets of connectors 104068-4 104078-6 and of socket 821815-1.  
Information available on Internet:  
<http://www.amp.com/>

- **[26]** 3M, “1996 Interconnect Products Catalog”.  
Some information are available on Internet:  
<http://www.3m.com/>
- **[27]** Fermilab Stock Catalog.  
Information available on Internet:  
<http://www-stock.fnal.gov/stock/>.
- **[28]** Atmel, Data Sheet of AT17C65 (FPGA Configuration EEPROM).  
Information available on Internet:  
<http://www.atmel.com/atmel/products/prod182.htm>