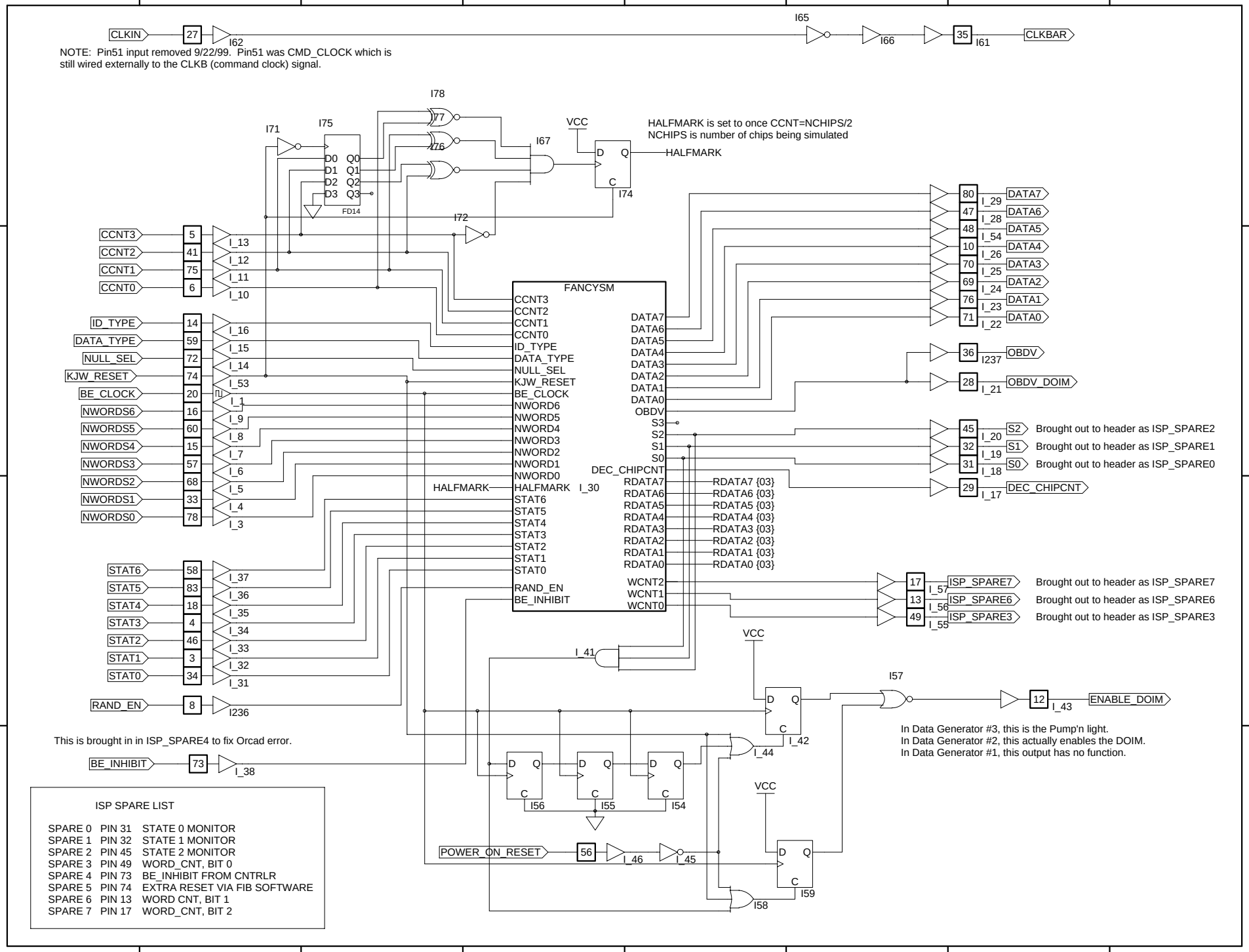
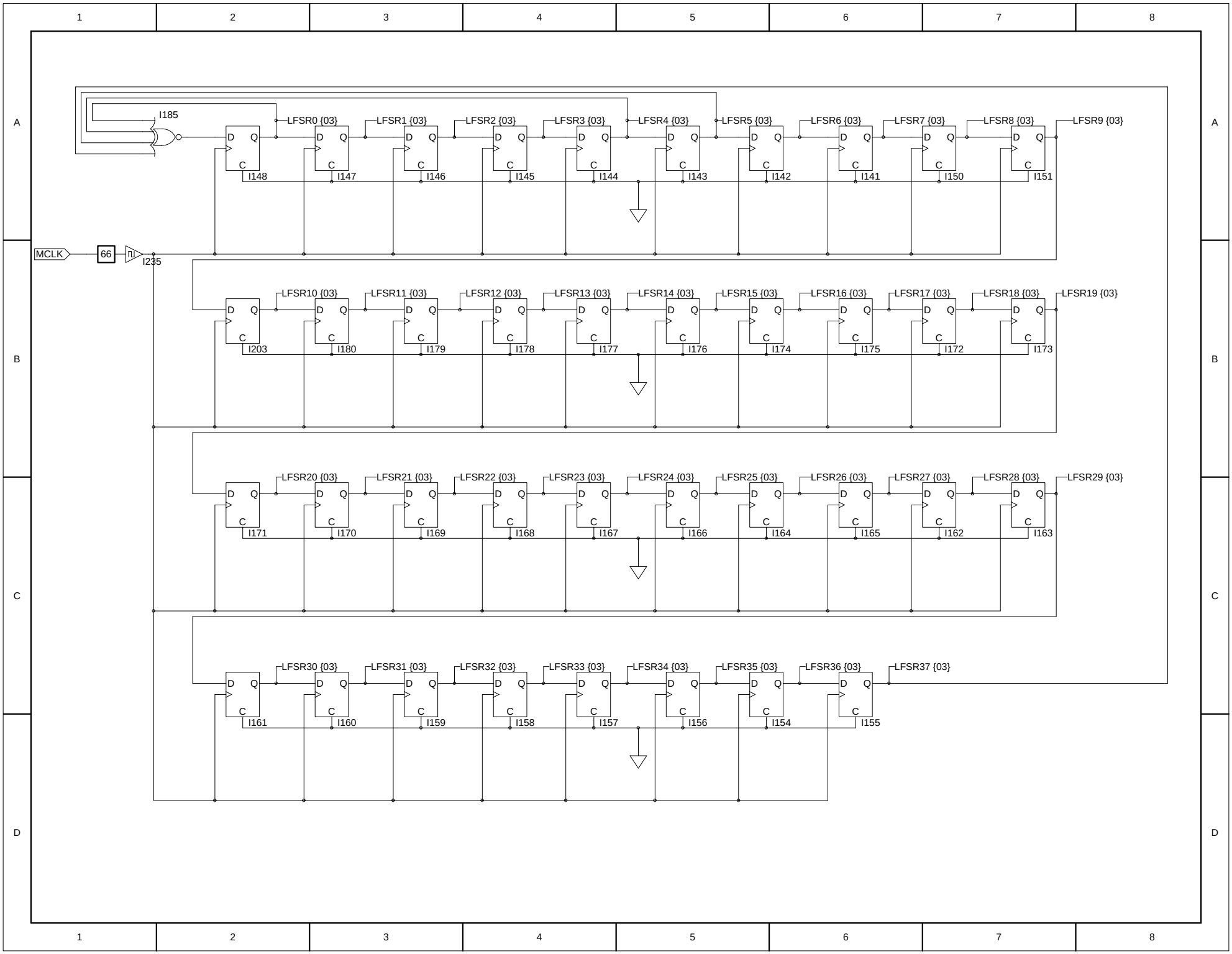
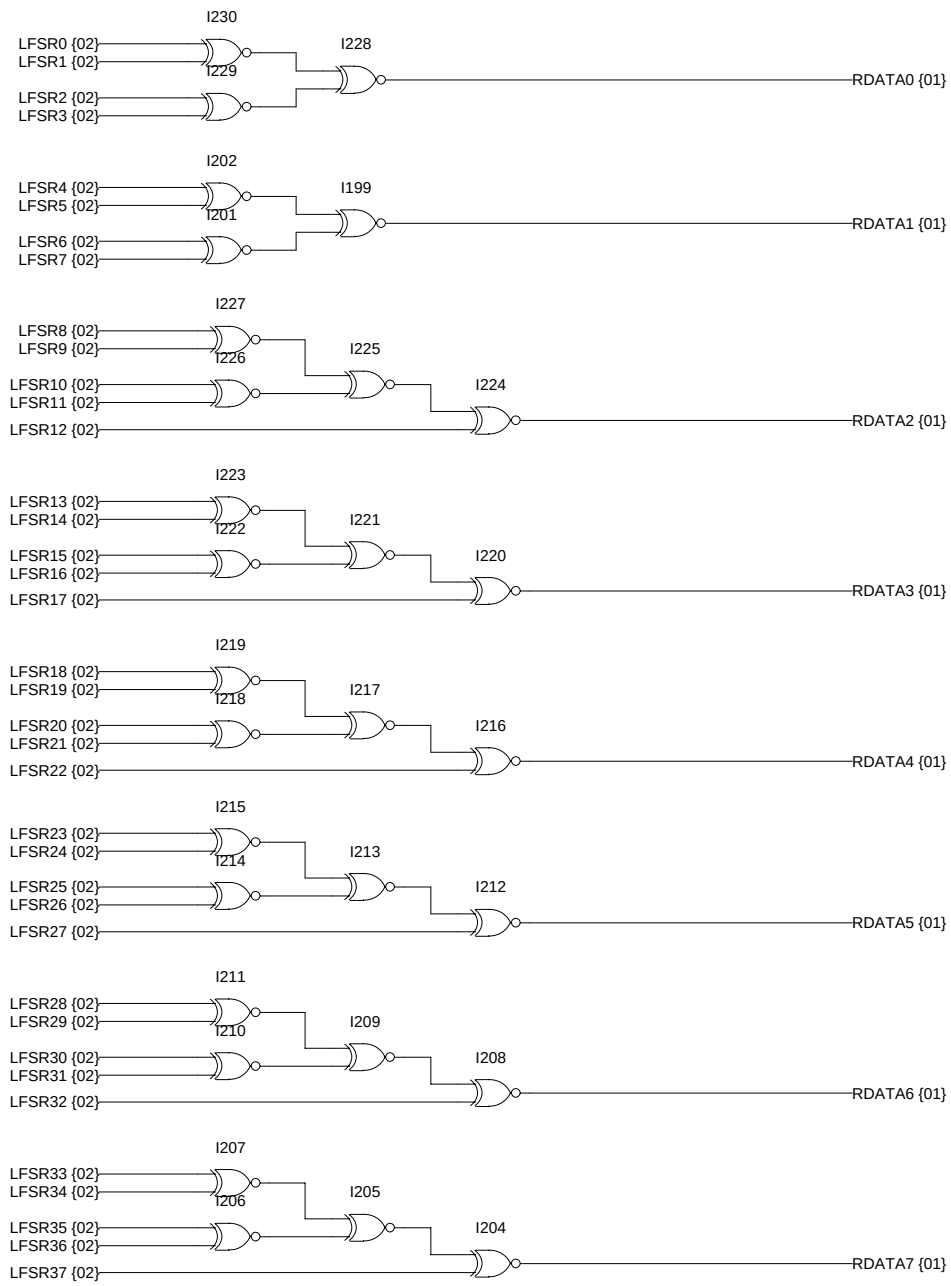

CLKIN
27
I62
I65
I66
35
I61
CLKBAR
NOTE: Pin51 input removed 9/22/99. Pin51 was CMD_CLOCK which is still wired externally to the CLKB (command clock) signal.
I78
I77
I76
I71
I75
D0 Q0
D1 Q1
D2 Q2
D3 Q3
FD14
I67
VCC
D Q
C
I74
HALFMARK
HALFMARK is set to once CCNT=NCHIPS/2
NCHIPS is number of chips being simulated
I72
CCNT3
CCNT2
CCNT1
CCNT0
5
41
75
6
I_13
I_12
I_11
I_10
ID_TYPE
DATA_TYPE
NULL_SEL
KJW_RESET
BE_CLOCK
NWORDS6
NWORDS5
NWORDS4
NWORDS3
NWORDS2
NWORDS1
NWORDS0
14
59
72
74
20
16
60
15
57
68
33
78
I_16
I_15
I_14
I_53
I_1
I_9
I_8
I_7
I_6
I_5
I_4
I_3
FANCYSM
CCNT3
CCNT2
CCNT1
CCNT0
ID_TYPE
DATA_TYPE
NULL_SEL
KJW_RESET
BE_CLOCK
NWORD6
NWORD5
NWORD4
NWORD3
NWORD2
NWORD1
NWORD0
HALFMARK
STAT6
STAT5
STAT4
STAT3
STAT2
STAT1
STAT0
RAND_EN
BE_INHIBIT
DATA7
DATA6
DATA5
DATA4
DATA3
DATA2
DATA1
DATA0
OBDV
S3
S2
S1
S0
DEC_CHIPCNT
RDATA7
RDATA6
RDATA5
RDATA4
RDATA3
RDATA2
RDATA1
RDATA0
WCNT2
WCNT1
WCNT0
HALFMARK
I_30
RDATA7 {03}
RDATA6 {03}
RDATA5 {03}
RDATA4 {03}
RDATA3 {03}
RDATA2 {03}
RDATA1 {03}
RDATA0 {03}
80
47
48
10
70
69
76
71
I_29
I_28
I_54
I_26
I_25
I_24
I_23
I_22
DATA7
DATA6
DATA5
DATA4
DATA3
DATA2
DATA1
DATA0
36
I237
OBDV
28
I_21
OBDV_DOIM
45
32
31
I_20
I_19
I_18
S2
S1
S0
Brought out to header as ISP_SPARE2
Brought out to header as ISP_SPARE1
Brought out to header as ISP_SPARE0
29
I_17
DEC_CHIPCNT
STAT6
STAT5
STAT4
STAT3
STAT2
STAT1
STAT0
58
83
18
4
46
3
34
I_37
I_36
I_35
I_34
I_33
I_32
I_31
17
13
49
I_57
I_56
I_55
ISP_SPARE7
ISP_SPARE6
ISP_SPARE3
Brought out to header as ISP_SPARE7
Brought out to header as ISP_SPARE6
Brought out to header as ISP_SPARE3
I_41
VCC
I57
RAND_EN
8
I236
12
I_43
ENABLE_DOIM
I_42
I_44
In Data Generator #3, this is the Pump'n light.
In Data Generator #2, this actually enables the DOIM.
In Data Generator #1, this output has no function.
This is brought in in ISP_SPARE4 to fix Orcad error.
BE_INHIBIT
73
I_38
I56
I55
I54
VCC
POWER_ON_RESET
56
I_46
I_45
I59
I58
ISP SPARE LIST
SPARE 0 PIN 31 STATE 0 MONITOR
SPARE 1 PIN 32 STATE 1 MONITOR
SPARE 2 PIN 45 STATE 2 MONITOR
SPARE 3 PIN 49 WORD_CNT, BIT 0
SPARE 4 PIN 73 BE_INHIBIT FROM CNTRLR
SPARE 5 PIN 74 EXTRA RESET VIA FIB SOFTWARE
SPARE 6 PIN 13 WORD CNT, BIT 1
SPARE 7 PIN 17 WORD_CNT, BIT 2


MCLK
66
I235
I185
LFSR0 {03}
LFSR1 {03}
LFSR2 {03}
LFSR3 {03}
LFSR4 {03}
LFSR5 {03}
LFSR6 {03}
LFSR7 {03}
LFSR8 {03}
LFSR9 {03}
I148
I147
I146
I145
I144
I143
I142
I141
I150
I151
LFSR10 {03}
LFSR11 {03}
LFSR12 {03}
LFSR13 {03}
LFSR14 {03}
LFSR15 {03}
LFSR16 {03}
LFSR17 {03}
LFSR18 {03}
LFSR19 {03}
I203
I180
I179
I178
I177
I176
I174
I175
I172
I173
LFSR20 {03}
LFSR21 {03}
LFSR22 {03}
LFSR23 {03}
LFSR24 {03}
LFSR25 {03}
LFSR26 {03}
LFSR27 {03}
LFSR28 {03}
LFSR29 {03}
I171
I170
I169
I168
I167
I166
I164
I165
I162
I163
LFSR30 {03}
LFSR31 {03}
LFSR32 {03}
LFSR33 {03}
LFSR34 {03}
LFSR35 {03}
LFSR36 {03}
LFSR37 {03}
I161
I160
I159
I158
I157
I156
I154
I155


I230
LFSR0 {02}
LFSR1 {02}
I229
LFSR2 {02}
LFSR3 {02}
I228
RDATA0 {01}
I202
LFSR4 {02}
LFSR5 {02}
I201
LFSR6 {02}
LFSR7 {02}
I199
RDATA1 {01}
I227
LFSR8 {02}
LFSR9 {02}
I226
LFSR10 {02}
LFSR11 {02}
LFSR12 {02}
I225
I224
RDATA2 {01}
I223
LFSR13 {02}
LFSR14 {02}
I222
LFSR15 {02}
LFSR16 {02}
LFSR17 {02}
I221
I220
RDATA3 {01}
I219
LFSR18 {02}
LFSR19 {02}
I218
LFSR20 {02}
LFSR21 {02}
LFSR22 {02}
I217
I216
RDATA4 {01}
I215
LFSR23 {02}
LFSR24 {02}
I214
LFSR25 {02}
LFSR26 {02}
LFSR27 {02}
I213
I212
RDATA5 {01}
I211
LFSR28 {02}
LFSR29 {02}
I210
LFSR30 {02}
LFSR31 {02}
LFSR32 {02}
I209
I208
RDATA6 {01}
I207
LFSR33 {02}
LFSR34 {02}
I206
LFSR35 {02}
LFSR36 {02}
LFSR37 {02}
I205
I204
RDATA7 {01}