

#	Modification	Reason	Comment
1	Add wire from R36 FIB* to U39 pin 19	Needed for FIB slot detect	
2	Add wire from U39 pin 73 to U39 pin 63	Routes CMD_CLK to dedicated clock resource pin on DEM control latch.	
3	Add wire from J33 pin 17 to U30 pin 72	Firmware modified to recognize this clock. NUL_SELECT input to all three data generators was floating (missing trace).	
4	Add wire from U31 pin 24 to U32 pin 24	Supplies power to U32	
5	Add wire from U33 pin 24 to U41 pin 24	Supplies power to U41	
6	Add wire from U42 pin 42 to U43 pin 24	Supplies power to U43	
7	Add wire from U30 pin 66 to J5 pin 16	Supplies MCLK to LFSR in datagen1	
8	Add wire from U40 pin 66 to J5 pin 16	Supplies MCLK to LFSR in datagen2	
9	Add wire from U24 pin 66 to J5 pin 16	Supplies MCLK to LFSR in datagen3	
10	Add wire from U51 pin 7 to U39 pin 24	Provides power on reset to controller	
11	Add wire from U51 pin 7 to U30 pin 24	Provides power on reset to datagen1	
12	Add wire from U51 pin 7 to U40 pin 24	Provides power on reset to datagen2	
13	Add wire from U51 pin 7 to U24 pin 24	Provides power on reset to datagen3	
14	U57 should be rotated counter clockwise once. Tab on U57 should be pointed towards R28 (silkscreen is incorrect).	Voltage regulator to bias DOIM has wrong orientation.	
15	Remove R28, replace with 500 Ohm potentiometer.	Allows for control of DOIM bias voltage.	
16	<i>Wire form U49 pin 1 to U39 pin 51</i>	<i>Changes DOIM STRB from BE_CLK to OBDV</i>	<i>(Wire Changed 9/22/99)</i>
17	Cut BE_BCLK trace going to U49 pin 1	Removed BE_CLK going to pin 1.	
18	<i>Wire from U40 pin 28 to U39 pin 50</i>	<i>Sends OBDV_DOIM to Controller for delay</i>	<i>(Wire Changed 3/15/00)</i>
19	Cut GND trace coming off of U46 pin 10	Removes GND to pin 10.	No longer needed 9/22/99
20	Lift the leads from their pads on U46 pins 16-23	Need to do this for the next modifications.	
21	Wire from U46 pin 16 to pad 23	Modifications #21-28 are done in order to flip the bit order of DATA going to the DOIM.	
22	Wire from U46 pin 17 to pad 22		

Hardware modification needed for DEM II modules (continued) Rev: 2.1

3/16/00

#	Modification	Reason
23	Wire from U46 pin 18 to pad 21	
24	Wire from U46 pin 19 to pad 20	
25	Wire from U46 pin 20 to pad 19	
26	Wire from U46 pin 21 to pad 18	
27	Wire from U46 pin 22 to pad 17	
28	Wire from U46 pin 23 to pad 16	
29	Wire from U39 pin 34 to U30 pin 8	RAND Enable control signal to Datagens
30	Wire from U30 pin 8 to U40 pin 8	RAND Enable control signal to Datagens
31	Wire from U40 pin 8 to U24 pin 8	RAND Enable control signal to Datagens
32	Wire from U30 pin 20 to U30 pin 27	BECLK to Datagen input
33	Wire from U40 pin 20 to U40 pin 27	BECLK to Datagen input
34	Wire from U24 pin 20 to U24 pin 27	BECLK to Datagen input
35	Wire from U30 pin 35 to U32 pin 13	Clk for data latch
36	Wire from U40 pin 35 to U46 pin 13	Clk for data latch
37	Wire from U40 pin 35 to U42 pin 13	Clk for data latch
38	Wire from U24 pin 35 to U28 pin 13	Clk for data latch
39	Lift the leads from their pads on U1 pins 11,13,14, and 15.	Remove original clks going to data latches.
40	Wire from U39 pin 46 to U39 pin 83	OBDV delay in controller
41	Wire from U26 pin 1 to U25 pin 1	Adds enable to data latch for Ch 7.
42	Cut the board top side trace coming off U40 pin 28 outside the U40 footprint. Cut it between U40 pin 28 and where it goes underneath U46.	Disconnect OBDV to the Ch 3,4,5 latches, but leave the OBDV trace to U39 pin 50.
		U40 pin 28 is now OBDV_DOIM
43	Add wire from U40 pin 36 to U43 pin 10	Connect OBDV to Ch 3,4,5 latches.
42	Added label "HW 2.1"	Update hardware revision
		U40 pin 36 is now OBDV HW Rev 2.1 requires Firmware Rev 5.3