Fermi National Accelerator Laboratory

SVX II Silicon Strip Detector Upgrade Project
Readout Electronics

DIGITAL TO ANALOG CONVERTER/ DECODER/REGULATOR CHIP (Version B)

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1. INTRODUCTION

This document describes the Digital to Analog Converter/Decoder/Regulator chip (DDR). Initially, in this section, we will briefly describe the Port Card (PC), to introduce the environment where the DDR chip will be used. Then, we will describe the major features of the DDR chip.

1.1 General Overview of the Port Card

The PC interfaces with the Fiber Interface Board (FIB), and with the SVX3 chip set (hereafter called SVX3 chip). The SVX3 chip is actually composed of two chips, the Front-End (FE) chip and the Back-End (BE) chip. Most of the communication of the PC is with the BE chip, while the FE connects directly to the Silicon Detector.

The basic functions and features of the PC are provided in the following list:

- Connects to five layers of SVX3 chips by means of the high density interconnects (HDIs).
- Initialize, control and readout the SVX3 chips through the HDIs.
- Regulated power supplies for the analog section of the SVX3 chips through the HDIs.
- Implements one digital-to-analog converters (DAC) to generate the calibration voltages for the *f* and *z* sides of the silicon detector.
- Implements the PC Decoder, which interfaces with the FIB and decodes commands to the SVX3 chips.
- Forwards the Level 1 Accept (L1A) and Pipeline Read 2 control signals to the SVX3 chips.
- During SVX3 chip initialization, selects the appropriate HDI to download the initialization bit stream.
- Transmits SVX3 event data (BUS[0:7]) with associated Odd Byte Data Valid strobe (OBDV) to the FIB.
- Buffer the front end clock (FE-CLK) and back end clock (BE-CLK) to the SVX3 chips.

The control of the SVX3 chips is split into two boards, the FIB and the PC. In this application, the PC, which provides local control to the SVX3 chips, may be considered as an extension of the FIB. This approach is taken to reduce the complexity of the PC.

The three main components of the PC are the following: the transceiver chips, the DAC/Decoder/Regulator (DDR) chips, and the Dense Optical Interface Module (DOIM) [1]. All these components are described elsewhere, and the reader should be acquitted with their specification.

The basic function of each one of these components are the following:

a) Transceiver - The FIB transmits controls and clocks to the PC using wires and differential signals. On the PC side, the transceivers acts as receivers, and translates the differential signals to single ended.

b) DDR - It has four main functions: generates the analog references required for the calibration inject feature of the SVX3 chips, decodes the controls sent by the FIB to the control pattern required by the SVX3 chips, regulates the analog voltages of the SVX3 chips and buffers the FE-CLK, the BE-CLK and the L1A signals.

c) DOIM - This is a set of components, a driver and a receiver, capable to transmit nine parallel data bits through fiber optic ribbon cable. The driver is assembled on the PC and is be used to transmit the SVX3 data and OBDV strobe to the FIB.

There is a substantial effort to develop and test these DOIMs. However, as a back up solution in case the DOIMs are not available, we can use the transceiver chips to transmit the SVX3 data through wire cables.

There are several issues that need to be addressed in the design of the PC. Three of them are radiation, size and mass. Based on the present information, the PC has to support about 300 KRads, and the size and mass should be kept to a minimum possible. To address these three issues, the DDR, the transceiver and the DOIM are custom made components. Both, the DDR and the transceiver chips will be design and manufacture with the same technology used for the SVX3 chips, which should ensure its rad-hardness.

A sketch of a possible layout of the PC, is shown in Figure 1.

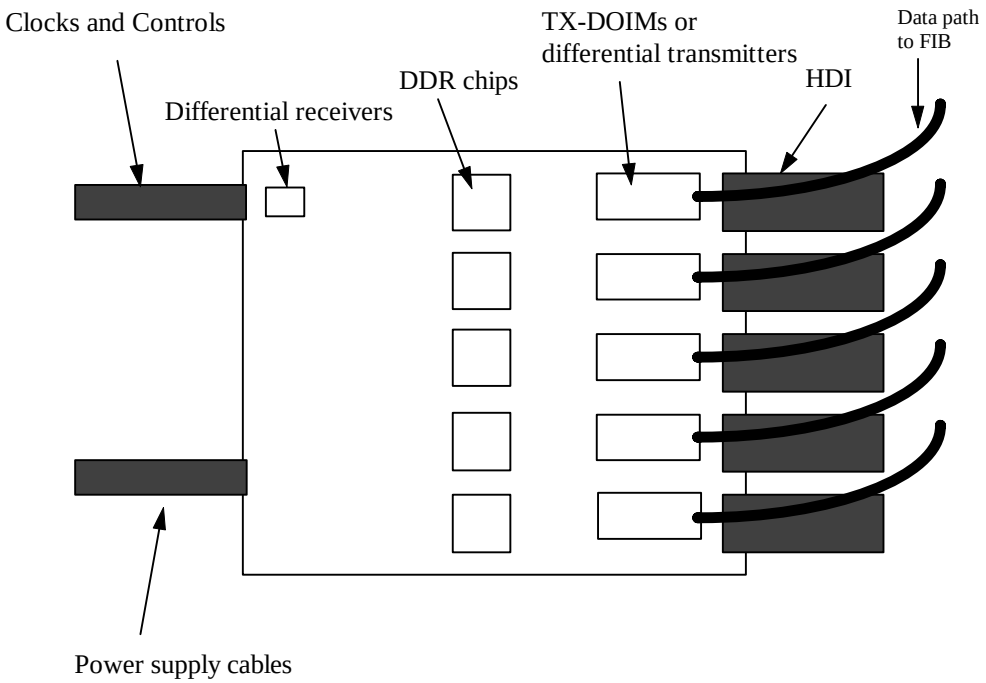

Figure 1. Sketch of the PC layout

1.2 The DDR Chip

The Digital to Analog Converter/Decoder/Regulator (DDR) chip is an analog and digital device that will be used on the Port Card (PC) of the Silicon Vertex Detector II (SVX). The main functions of the DDR chip are the following:

- Implements the one decoder and latches that allow the Fiber Interface Board (FIB) to remotely control the SVX3 chips.

- Tri-state buffers with differential outputs for lines shared by control and data.
- Implement one analog to digital converter (ADC) to generate the calibration voltage reference for the SVX3 chips.
- Implement the amplifier and voltage reference for the voltage regulator of the SVX3 chips. The series transistors are external to the DDR chip.
- Selectable divide by two circuit for the Back-End Clock (BE-CLK). Differential buffer for the Front-End Clock (FE-CLK).
- Buffer for control signals of the SVX3 chips.

There are several documents worth reading for a fully understanding of the utilization of the DDR chip: the FIB specifications [2], the PC specifications [3] and the SVX3 chip specifications [4].

The PC has five high density interconnect (HDI) cables. These cables interconnect the PC with the hybrids, where the SVX3 chips are assembled. Each one of these HDI cables will be connected to one DDR chip. One side of these five DDR chips will be connected in parallel to the FIB, while the other side will be connected to its specific HDI. Therefore, there is a one-to-one relationship between the DDR chip and its HDI.

During data acquisition, digitization and readout, all SVX3 chips will be operating in parallel, and the same will happen with the DDR chips. However, during the configuration of the SVX3 chips, just one specific set of SVX3 chips associated with one HDI must be accessed. The configuration of the SVX3 chips are unique, and therefore, just the selected set of SVX3 chips should be configured.

Figure 2 depicts the block diagram of the DDR chip. In Appendix A we have included the schematics (Figure A.1). Next sections will specify and describe in detail the custom made chip for the PC. This chip will incorporate analog and digital features and is to be designed and manufactured using the same or equivalent technology used for the SVX3 chips.

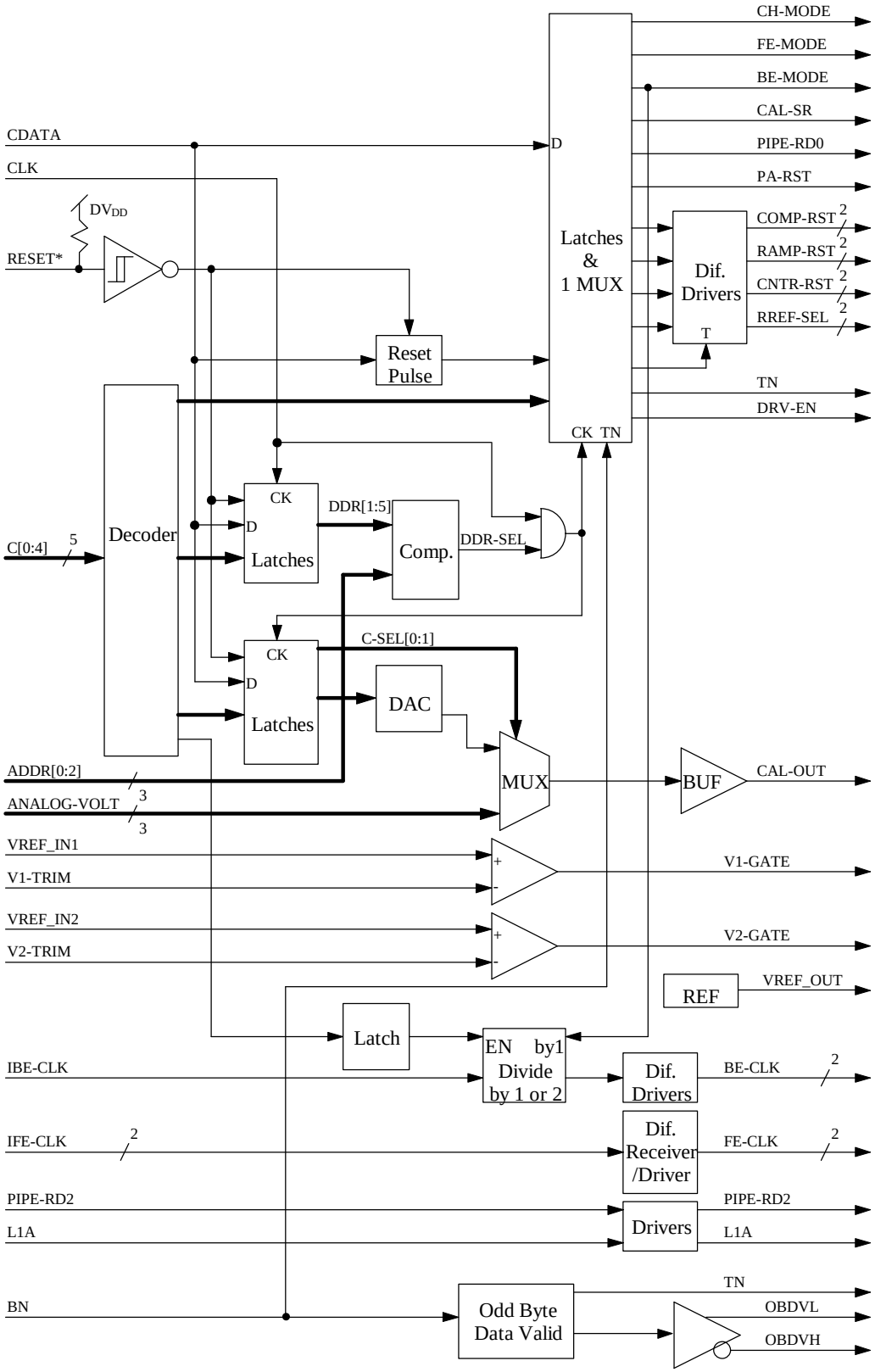

Figure 2. Block Diagram of the DDR Chip

2. DECODER

The control of the internal units of the DDR chip and associated SVX3 chips is implemented by an interface that includes seven signals:

- five control signals (C[0:4]),
- clock (CLK),
- level control signal (CDATA)

The C[0:4], CDATA, and CLK lines are used to control the bit levels of the units inside the DDR chip, as well as several control lines of the SVX3 chips. Figure 3 shows one of the FF latches. The CDATA and CLK line connects directly to all D and clock inputs of the FFs, respectively. The output of the decoder (a 5 inputs to 32 output decoder) is connected to the enable (E) input of the FF. Therefore, to set and reset a bit of some internal unit of the DDR chip or a control line of the SVX3 chip one has to proceed in the following way:

- select the bit or line (i. e., the proper FF) by setting the proper code on the C[0:4] lines.
- select the desired logical level by setting to “1” or “0” the CDATA.
- generate a rising edge on the CLK line.

We refer to this sequence as the command sequence.

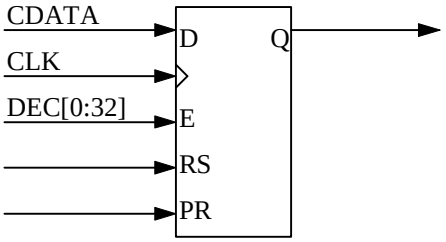

Figure 3. The FF Latch

Each FF also has a preset (PR) or reset (RS) inputs (but not both). Through these inputs, the FFs are force to a specific state during power up or during a DDR reset command.

2.1 Command Timing

The timing of the C[0:4], CDATA, CLK lines and internal reset/preset (RS/PR) and Q FF latch lines are given by Figure 4 and Table 1. The timing associated with the internal RS/PR and Q lines are not critical, and it is specified in such a way that should be easy for the chip designers to accomplish it. Note that the time of the DELAY depicted in Figure A.1 is given by the minimum reset/preset pulse width (t_8 = 15ns). We are assuming the 15 ns will be enough to reset/preset all FFs but, of course, this will depend on the design and process. If this is the case,

the time of the delay should be larger than 15 ns, say, 25 ns. We will return to this subject in Section 3.

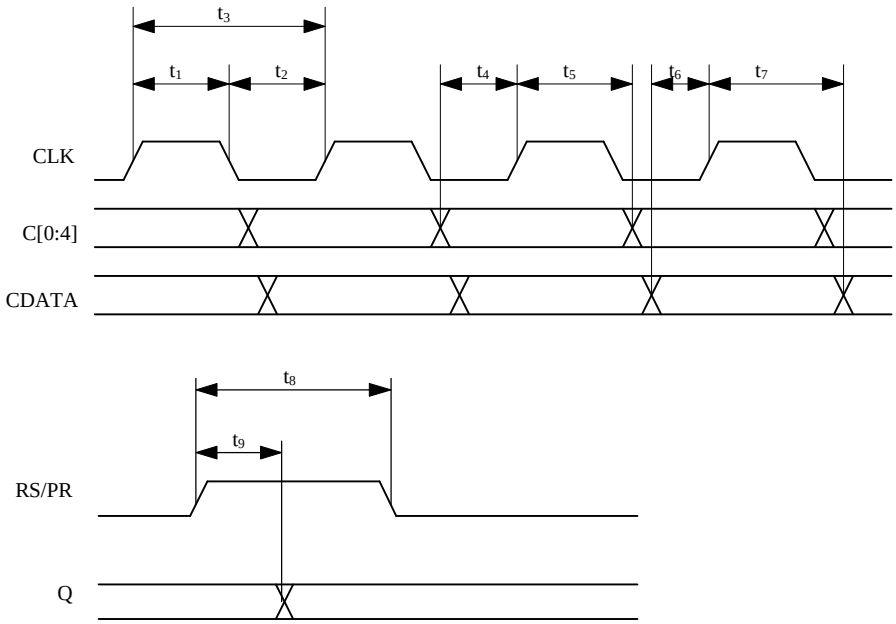

Figure 4. Command and Reset/Preset Timing

Table 1. Command Timing

Parameter	Description	Min	Max	Units
t_1	Clock high time	8		ns
t_2	Clock low time	8		ns
t_3	Clock cycle time	20		ns
t_4	Setup time	6		ns
t_5	Hold time	3		ns
t_6	Setup time	4		ns
t_7	Hold time	3		ns
t_8	Reset/preset pulse width	15		ns
t_9	Reset/preset to Q output		8	ns

DV_{DD}=5V±5%, T_A=+5°C to +65°C

2.2 Command Decoding

Command decoding of the C[0:4] lines is shown in Table 2.

Table 2. Command Code Definitions

C[0:4]	NAME	Description
0	RESET	Reset/preset the FFs of the control lines of the SVX3 chips
1	DDR1	Enable DDR1 chip
2	DDR2	Enable DDR2 chip
3	DDR3	Enable DDR3 chip
4	DDR4	Enable DDR4 chip
5	DDR5	Enable DDR5 chip
6	SVX3_RB	Enable SVX3 Readback on BUS3
7	DAC0	DAC0 Value
8	DAC1	DAC1 Value
9	DAC2	DAC2 Value
10	DAC3	DAC3 Value
11		available
12		available
13	SEL0	Multiplexer output select 0
14	SEL1	Multiplexer output select 1
15		available
16	NOP	No Operation
17	CH_MODE	Change Mode signal for SVX3 chips
18	FE_MODE	Front End Mode signal for SVX3 chips
19	BE_MODE	Back End Mode signal for SVX3 chips
20	CAL_SR	Calibration inject, Strobe signal for SVX3 chips
21	PIPE_RD1	PIPE-RD1 signal for SVX3 chips
22	PA_RST	Pre-amplifier reset
23	COMP_RST	Comparator Reset (BUS0) signal for SVX3 chips
24	RAMP_RST	Ramp Reset (BUS1) signal for SVX3 chips
25	CNTR_RST	Counter Reset (BUS2) signal for SVX3 chips
26	RREF_RST	Ramp Reference Reset signal(BUS3) for SVX3 chips
27	TN	Top Neighbor signal for SVX3 chips
28	BUF_EN	Tri state control for BUS[0:3]
29	BE_CLK_EN	Back End Clock Enable
30	DRV_EN	Driver enable (enables the TX-DOIM outputs)
31		available

3. RESET CIRCUITRY

The FF latches of the DDR chip can be reset or preset through the RESET* input. The FFs latches associated with the control lines of the SVX3 chips are also reset or preset as the result of the execution of the command sequence C[0:4]=16. The block diagram of the reset circuit is shown in Figure 2, while the details are shown in Figure A.1.

The RESET* input goes to most of the reset/preset inputs of the FF latches. A logical level ZERO in this input will reset or preset all FFs. It enters the chip through a Schmitt trigger circuit and it is connected to DV_{DD} by the resistor. The resistor serves two purposes: to set to ONE the RESET* input if it is not connected, and to provide a reasonable electrical resistance in case we want to connect the RESET* input to an external capacitor, to generate the power up reset. Table 3 shows the electrical characteristics of the RESET* input. Note that Table 3 specifies the input resistance measured to DV_{DD}. In case the input impedance of the Schmitt trigger is far higher than the resistance of the resistor, the RESET* input resistance will basically be the value of the resistor.

Table 3. RESET* Input Characteristics

Parameter	Condition	Min	Typ	Max	Unit
RESET threshold for positive going inputs	DV_{DD}=5V	2.7	3.0	3.3	V
RESET threshold for negative going inputs	DV_{DD}=5V	1.7	2.0	2.3	V
RESET input resistance	Measured to DV_{DD}	80	100	120	KΩ

DV_{DD}=5V±5%, T_A=+5°C to +65°C, unless otherwise noted

This RESET* input has one important characteristic: when we are ramping DV_{DD} (as we intend to do for V_{IN}, see Section 9), it should keep the control outputs and the clocks of the SVX3 chip at the levels specified by the reset/preset inputs of the FF latches. The reason for this is that the SVX3 chip may require a specific configuration on the clocks and control lines to avoid some unknown state that draws more current from the power supplies (this was the case of the SVX2 chip).

For the FFs associated with the control lines of the SVX3 chip, there is an additional circuitry to generate a reset/preset. When the DDR executes the reset command sequence C[0:4]=16, the DELAY and its associated FF generates a reset/preset pulse long enough to guarantee that all selected FFs will switch to the required level (in Section 2.1 we suggest 25 ns).

The proper state of the FF latches after a power up reset or a reset command sequence is shown in Figure A.1 of Appendix A. The FFs that employ the reset (RS) input should go to “0”, while the FFs with the preset (PR) input should go to “1”.

4. FRONT END CLOCK DIFFERENTIAL RECEIVER/DRIVER

The DDR chip has one differential receiver/driver cell associated with the front end clock (FE_CLK) whose timing is critical (see Figure 5 and Figure A.1). This is the clock that provides the correct sampling time for all SVX3 chip. So, to ensure that all the SVX3 chips in all hybrids will sample in synchronism and phase, the maximum and minimum delays, as well as the rise and fall time of this receiver/driver has to be within specifications.

The electrical protocol of the differential lines must conform with the Low Current Differential Signals (LCDS) specifications. Section 12.2 describes the features of this protocol, and for the detailed specifications the chip designer should refer to [5]. All differential lines that connect to the DDR chip, inputs or outputs, should conform with this protocol.

The "Driver AC Characteristics" table of the LCDS specifications describes the rise and fall time for the differential lines. The rise and fall times are critical because the FE_CLK input of the front end portion of the SVX3 chip should have some hysterisis and threshold. We want to make sure that the switching time of the differential FE_CLK lines do not add any significant delay for the correct sampling time of the SVX3 chip.

Figure 5 shows how to measure the maximum and minimum delays for the driver/receiver cell. The propagation delay of the driver is measured at 0V differential on the inputs and outputs of the cell. Table 4 specifies the delays.

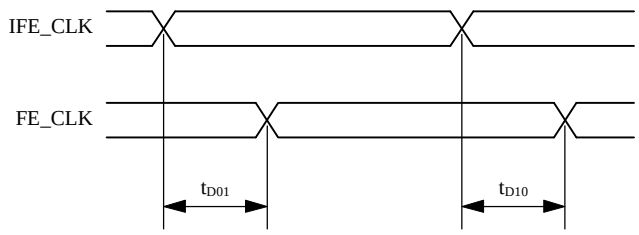

Figure 5. Delay of the FE_CLK

Table 4. FE_CLK maximum and minimum delay specifications

Symbol	Parameter	Conditions	Min	Max	Unit
t_{D01}, t_{D10}	Propagation delay t_{D01} = low to high t_{D10} = high to low	$25\Omega < Z_{LOAD} < 120\Omega$	6	10	ns

DV_{DD}=5V±5%, T_A=+5°C to +65°C

5. BACK END CLOCK

The Back End Clock (BE_CLK) circuitry of the DDR has two features: control of clock frequencies and the ability to enable and disable the clock.

The Back End portion of the SVX3 chip requires two clock frequencies during data digitization and readout: BE_CLK = 53 MHz and BE_CLK = 26.5 MHz, respectively. The 26.5 MHz frequency has a critical feature: it has to be as close as possible of a square wave. Therefore, in order to avoid further duty cycle distortion of the clock on the cables and buffers utilized to send commands and clocks to the PC, we decided to perform a “divide by two” clock division directly on the PC, through the DDR chip. In this way, the FIB can transmit just 53 MHz during data digitization and readout, and the DDR chip transforms it to 26.5 MHz clock with duty cycle close to 50 %.

The circuitry to perform this task is shown in details in Figure A.1 of the Appendix (also see the block diagram in Figure 2). When the control line BE_MODE of the SVX3 is set to “0”, the “divide by two” circuit is selected by the multiplexer. Then, the DDR chip uses the differential IBE_CLK input, which is always running at 53 MHz, to generate the 26.5 MHz on the differential BE_CLK output. This is depicted in Figure 6. Observe that the delay between the IBE_CLK input and the BE_CLK output is not critical, and it is not actually represented. Table 5 describes the maximum duty cycle distortion of the clock in such circunstance. The numbers are equivalent to approximately ±3% duty cycle distortion. Note that, contrasting with critical delay and rise/fall times feature of the FE_CLK, the BE_CLK does not have this requirement. In this sense, we specified a bigger maximum delay, hoping that this requirement will not impose any major constraints on the chip designers.

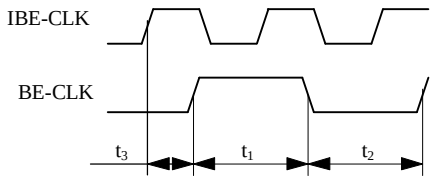

Figure 6. Divide by Two Timing

Table 5. Divide by Two Timing

Parameter	Description	Min	Max	Units
t_1	Clock high time @ 53 MHz IBE-CLK input	18.6	19.8	ns
t_2	Clock low time @ 53 MHz IBE-CLK input	18.6	19.8	ns
t_2	Delay		14	ns

DV_{DD}=5V±5%, T_A=+5°C to +65°C, unless otherwise noted

Figure 7 and Table 6 specify the 50% duty cycle distortion and delay on the BE_CLK when the multiplexer is selecting the IBE_CLK input directly (BE_MODE = 1), i.e., we have a “divide by 1”. This is the moment the BE portion of the SVX3 chip will digitize the analog information stored on the FE portion of the chip. In this situtation, both the IBE_CLK and the BE_CLK will be operating at 53 MHz.

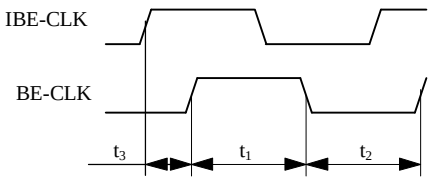

Figure 7. BE_CLK Timing with Divide by 1

Table 6. BE_CLK Timing with Divide by 1

Parameter	Description	Min	Max	Units
t_1	Clock high time @ 53 MHz IBE-CLK, 50% duty cycle	8.4	10.4	ns
t_2	Clock low time @ 53 MHz IBE-CLK, 50% duty cycle	8.4	10.4	ns
t_3	Delay		10	ns

DV_{DD}=5V±5%, T_A=+5°C to +65°C, unless otherwise noted

As previously observed, the BE_CLK also has circuitry to enable and disable the front end clock (see Figure A.1 of the Appendix and block diagram in Figure 2). This is accomplished through the DDR command code C[0:4] = 29, BE_CLK_EN. The two flip flops in a row are used to remove any metastability problem with synchronism of the command clock and the BE_CLK.

The differential signals must conform with LCDS specifications.

6. ADDRESSING OF THE DDR CHIPS

In order to provide the DDR chip with the ability to perform operations unique to one selected DDR chip, it employs addressing capability. All DDR chips in one PC are connected in parallel to the FIB. However, several operations are uniquely related to one specific DDR chip and, therefore, we have to implement this addressing feature. The internal units of the DDR chip that can be enable or disable depending on the DDR address are:

a) The FF latches associated with the control lines of the SVX3 chips

b) DAC

c) Voltage regulator enable

d) Multiplexer selection

The addressing feature operates in the following way (see the block diagram in Figure 2 and, for more details, Figure A.1). The DDR chip contains three inputs, ADDR[0:2], which allow the selection of a binary address for the DDR. It also contains one set of FF latches that are connected directly to the clock (CK) input, while the CK of another set passes through an AND gate. The first set employs five FF latches, named DDR[1:5], whose outputs are connected to one multiplexer. These FF latches are accessible through the normal command sequence operation and the FIB can set or reset any of the DDR[1:5] bits. The multiplexer selects the DDR[1:5] bits based on the logical level of ADDR[0:2] lines, and if the selected DDR[1:5] bit is logical level “1”, it sets the DDR selected (DDR-SEL) control line, enabling the CK to follow to the other FF latches.

The reason for enabling or disabling the access of the control lines of the SVX3 chips is the following. The PC has five HDI cables, that interconnect the PC with the hybrids, where the SVX3 chips are assembled. During data acquisition, digitization and readout, all SVX3 chips will be operating in parallel and, therefore, the control lines of the HDI must be switching in parallel. However, during the configuration of the SVX3 chips, just the group of SVX3 chips associated with one HDI must be set to the configuration mode. So, using the addressing capability of the DDR chip, the FIB can enable the CK of the FF latches associated with the control lines of one specific DDR chip. Now, the FIB can change the state of the control lines of this specific HDI, and configure the group of SVX3 chips. The control lines of the other HDIs will remains unchanged and, therefore, their associated SVX3 chips will not be reconfigured.

Table 7 shows the configuration of the DDR[1:5] FF latches and the ADDR[0:2] inputs to select one specific DDR chip. To select all DDR chips, independently of the ADDR[0:2] inputs, the procedure is to set all DDR[1:5] bits to one. This is used during data acquisition, digitization and readout, when all SVX3 chips must be operating in parallel.

Table 7. DDR[1:5] and ADDR[0:2] for DDR Selection

DDR[5]	DDR[4]	DDR[3]	DDR[2]	DDR[1]	ADDR[0:2]
0	0	0	0	1	1
0	0	0	1	0	2
0	0	1	0	0	3
0	1	0	0	0	4
1	0	0	0	0	5

The ADDR[0:2] inputs have internal 47KΩ pull-up resistors, and if they are not connected the default logical level is “1”.

7. READING BACK THE CONFIGURATION OF THE SVX3 CHIPS

The DDR chip also employs a feature that allows reading back the configuration of the SVX3 chips. After the chips were configured, it is advisable to perform this readback, to check if all configuration bits were properly downloaded. For this, the FIB has to set the SVX3_RB bit, command code C[0:4]=22, and then provide the BE-CLK (Figure A.1).

The readback operation, as well several other operations, are unique to one specific DDR chip. So, before the FIB performs the readback, it has to address a specific DDR chip.

Observe that the readback destroys part of the SVX3 chip configuration. Therefore, after the chip was readback, the FIB has to execute one configuration cycle again, to reconfigure the SVX3 chips that are connected with that DDR chip.

8. DIGITAL TO ANALOG CONVERTER

The DDR chip needs to generate calibration (CAL) voltage reference to the back end portion of the SVX3 chips. Some the SVX3 chips are connected to the f side of the silicon detector, while others are connected to the z side of the silicon detector. The CAL voltage level is different for each side of the detector and the SVX3 chip has a feature that enables it to generate this two different voltage levels internally, from one single CAL reference input. Figure 8 shows the connection of the CAL output of the DDR with the SVX3 chips. The DAC on the DDR is a four bit DAC. Table 8 shows the specifications of the DAC.

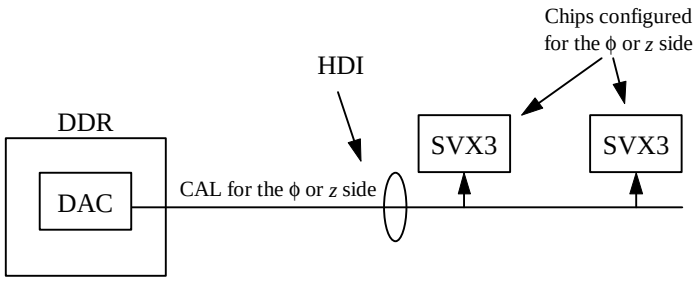

Figure 8. Two DACs inside the DDR

Table 8. Calibration DAC specifications

Parameter	Condition	Min	Max	Unit
Resolution		4		bits
One bit resolution		65	90	mV
Temperature dependency	Full temp. range, any bit combination		2	%
Output voltage	All bits at one	3.15	3.25	V
Output voltage	All bits at zero	1.9	2.05	V
Degradation	150 Krad		50	mV
Power supply sensitivity	AV_{DD}=4.75V to 5.25V		50	mV

AV_{DD}=5V±5%, T_{DIE}=+5°C to +65°C, V_{REF} = 5V, unless otherwise noted

The only AC performance characteristic of the DAC to impose major constrains on the design is the output noise spectral density, which generates a RMS noise voltage in the output of the DAC. One way to limit the RMS noise is to limit the bandwidth of the output amplifier of the DAC, or, similarly, its slew rate. Other AC characteristics like settling time, channel-to-channel isolation, digital crosstalk, digital feedthrough, etc. will not be specified.

a) Temperature dependence: this measure is done with AV_{DD} = 5V and with the reference voltages fixed, and includes all effects of temperature. The DAC characteristics specify the maximum variation of the DAC output voltage considering a temperature variation from 5°C to +65°C.
b) Degradation: this measure is done with all voltages and temperature fixed, and with the DAC submitted to a dose rate of 0.01 rad/s. The DAC characteristics specify the maximum variation of the output, due to radiation or any other aging or degrading effect.

9. VOLTAGE REGULATOR

The PC will employ five sets of two voltage regulators, one voltage regulator adjusted to AV_{DD}=5V, the other for AV_{DD2}=3.5V. Presently, there is a strong desire to remove the AV_{DD2} power supply, and supply all the current through the AV_{DD} power supply. If this is the case, just one of the operational amplifiers inside the DDR will be used.

The DDR chip includes the operational amplifier and voltage reference portion of the voltage regulator, as depicted in Figure 9. The series transistors, the feedback resistors R_1 and R_2 and the capacitors C_C, C_L and C_R are outside the chip. Probably, more than one JFET will be connected in parallel to the base of the NPN transistor. Also, observe that the V2_IN input (see Figure A.1), identified as V_{IN} in Figure 9, besides powering up the operational amplifier, also powers up the voltage reference. Therefore, V1_IN and V2_IN in Figure A.1 are not the same.

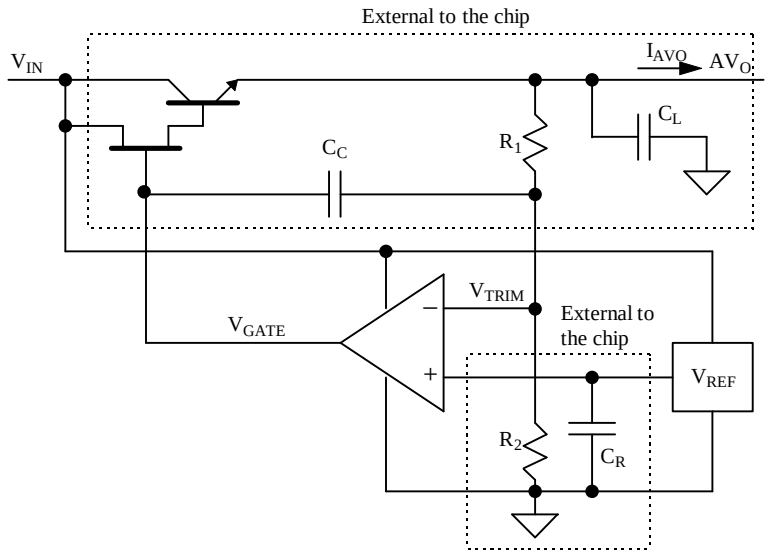

Figure 9. Voltage regulator

These regulators must ramp the analog voltage AV_O if we ramp the input voltage AV_{IN}[1]. So, for example, if the regulator is designed for AV_O = 5V, AV_O should follow AV_{IN}, as sketched in Figure 10. Note that there is no glitch or voltage step in AV_O, and that it clamps at 5V when it reaches this voltage. Presently we do not know if the SVX3 chips will require this ramp. We believe that the ramps will be slow, something like 30 ms for AV_O to go from 0 to 5V. Exactly the same rule apply to the 3.5V power supply (which generates AV_{DD2}) but, of course, with AV_{IN} ramping from 0 to, say, 4.2V and AV_O from 0 to 3.5V.

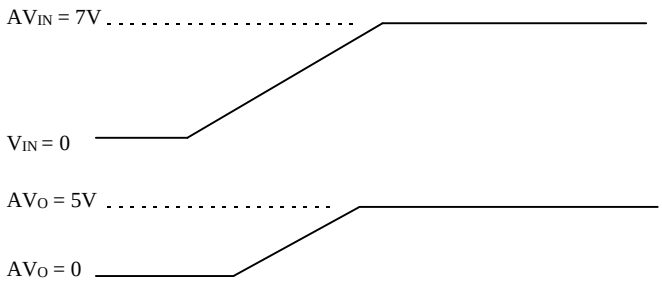

Figure 10. Behavior of AV if V_{IN} ramps

Observe that this voltage regulator will not have any protection for over current or temperature. However, the power supplies themselves, the units that supply the current to the collector of the NPN and the drain of the JFET will actually employ current limiting. Therefore, the heat dissipation should be such that the transistors, as well as the custom made chip, will resist

[1] V_{IN} refers to V_{1_IN} and V_{2_IN} in Figure A.1.

a short circuit in its output. In any case, care must be taken to avoid any short circuit in the output.

The JFET and NPN transistor pair has to be implemented with transistors that will support the radiation produced by the accelerator beam. Presently, it looks like we can use the die version of the JFET U290 (manufactured by Siliconix [6]) and the die number 184 or 185 from Solitron. We have tested these three transistors in the booster beam, and they have performed satisfactorily for radiation levels up to 300 Krads.

The capacitor C_R was included for the following reason: fast variations on the power supply of the V_{REF} circuitry may cause variations on the voltage V_{REF}, that will refect into variations of AV_O (see Figure 9). However, since the operational amplifier can be design to have high power supply rejection, if we keep with a capacitor the voltage V_{REF} at the same level, the voltage AV_O will not change. This is the reason why C_R was included. However, we should say that we would prefer to avoid the use of C_R, if the chip designers find a way to avoid it.

9.1 Characteristics of the Voltage Regulator

Table 9 and Table 10 describe the characteristics of the voltage regulator. These characteristics include all components associated with the voltage regulator, internal and external to the DDR chip (see Figure 9). So, it includes the JFET and the NPN transistor, the feedback resistors R_1 and R_2 and the external capacitors C_C, C_L and C_R. Table 11 shows the absolute maximum ratings.

The external compensating capacitor C_C should be chosen in such a way that the voltage regulator does not oscillate and have good response for steps on the AV_{IN} voltage or output load.

Table 9. Voltage Regulator DC Characteristics

Characteristic	Test Conditions	5.0V		3.5V		Unit
		Min	Max	Min	Max	
AV_O Output voltage	Trimmed to 5V @ I_{AV} = 0.25A, $0.05<I_{AV}<0.75A$	4.90	5.10	3.40	3.61	V
ΔAV_O Line regulation	$6.5V<V_{IN}<7.5V$ for 5V voltage reg. $5.0V<V_{IN}<6.0V$ for 3V voltage reg. I_{AV} = 0.25A		18		10	mV
ΔAV_O Load regulation	$0.05<I_{AV}<0.75A$		15		15	mV
V_{REF} Reference voltage	$6.5V<V_{IN}<7.5V$	2.35	2.65	2.35	2.65	V
V_{GATE} Control Output[2]	$\|I_{GATE}\|$ = 1µA	0.1	V_{IN}–0.2	0.1	V_{IN}–0.2	V
$R_{INPUT\ OP.AMP.}$		2		2		MΩ
Degradation	300 Krads		±0.1		±0.07	V
AV_N Output noise voltage	T_j = 25°C, 10 Hz < f < 100KHz		4		3	μV_{RMS}

T_j=5°C to +65°C, V_{IN}=5.7V (for the 5V regulator) or V_{IN}=4.2V (for the 3.5V regulator), C_R=1µF, C_L=15µF, unless otherwise specified

[2] We have exposed the JFET U290 to 300 KRads. After it was radiated, the I_{GSS} leakage current increased to less than 10 nA. So, the 1µA requirement should be a safe margin.

Table 10. Voltage Regulator AC Characteristics

Characteristic	Test Conditions	5.0V		3.5V		Unit
		Min	Max	Min	Max	
Line transient response	$5.5V<V_{IN}$ & $AV_{IN}<6.5V$ for $AV_O=5V$ $4.0V<V_{IN}$ & $AV_{IN}<5.0V$ for $AV_O=3.5V$		0.1		0.1	V
			1		1	µs
Load transient response	$\Delta I_{AVO}=0.1A$		50		50	mV
			1		1	µs

T_j=5°C to +65°C, V_{IN}=5.7V (for the 5V regulator) or V_{IN}=4.2V (for the 3.5V regulator), C_R=1µF, C_L=15µF, unless otherwise specified

Table 11. Absolute Maximum Ratings of the Operational Amplifier

Characteristic	Test Conditions	
V_{IN}		7.5V
V_{GATE} short circuit duration	V_{IN}=7.0V	Indefinite
V_{TRIM}[3]		0 to V_{IN}

Figure 11 shows the transient time (t_T) and transient voltage (ΔV_T) cause by disturbance on the load (ΔI_{AVO}) or the line voltage (ΔAV_{IN}). The transient time is measured from the beginning of the disturbance until the amplitude of the variation ΔV_T reaches 10% of its peak.

[3] V_{TRIM} refers to V_{1_TRIM} and V_{2_TRIM} in Figure A.1.

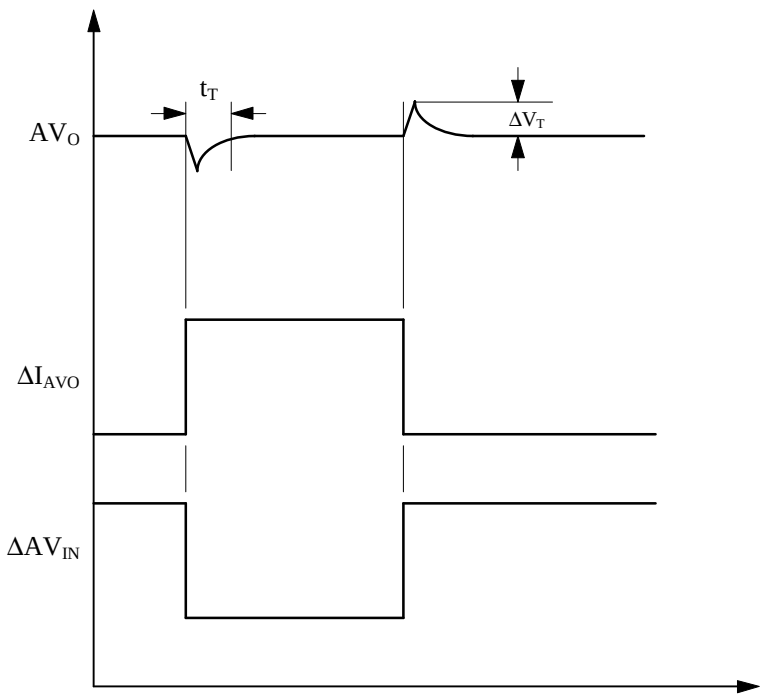

Figure 11. Transient Time and Voltage

The degradation of the voltage regulator due to radiation adds to the AV_O Output Voltage. So, after the whole voltage regulator (including the DDR chip and external components) were exposed to 300 KRads, the maximum error on the output voltage should be less than ±5%, considering T_j=5°C to +65°C, V_{IN}=7.0V (for the 5V regulator) or V_{IN}=5.5V (for the 3.5V regulator).

The operational amplifier portion of the voltage regulator should have reasonable high input resistance, to avoid loading the voltage divider formed by R_1 and R_2.

9.2 Diodes

The DDR has two diodes in series, as shown in Figure A.1, connected to pads CAT and ANODE. The objective of these diodes is to decrease the voltage supplied delivered to the operational amplifier. The transistors on the Honeywell process support the maximum voltage of 8 volts. If we want to decrease the voltage drop over the transistors of the operational amplifier, these two diodes can be connected in series with the V1_IN or V2_IN pads.

Preliminary tests with the DDR hint that it is not necessary to use the diodes to decrease the power supply voltage of the operational amplifiers, since the current doesn't significantly increase until V1_IN or V2_IN are higher than 10 V. The voltage regulator operates properly with power supplies of 10 V.

10. ODD BYTE DATA VALID

The SVX3 chips are connected in a chain of top neighbors/bottom neighbors (TN/BN), also known as Priority In and Priority Out, respectively. The TN tells the SVX3 chips when the readout starts, and the BN tells when it is done. So, if the BN of one chip is connected with the TN of the next, we can readout one chip after another.

The SVX3 chip has the differential Odd Byte Data Valid (OBDV) lines that validates the readout data. The OBDV lines have to be very clean of electrical noise and glitches, because this signal is used by the FIB to save the data. Since the OBDV signal is asserted by several SVX3 chips in a chain, each SVX3 chip has the capability to assert and tri-state these lines in a specific sequence. This sequence is controlled by the 26.5 MHz BE_CLK and the TN line and is depicted in Figure 12. For more details on this protocol, see reference [7]. Note that two SVX3 chips will be driving the OBDV lines during portion of the null cycle.

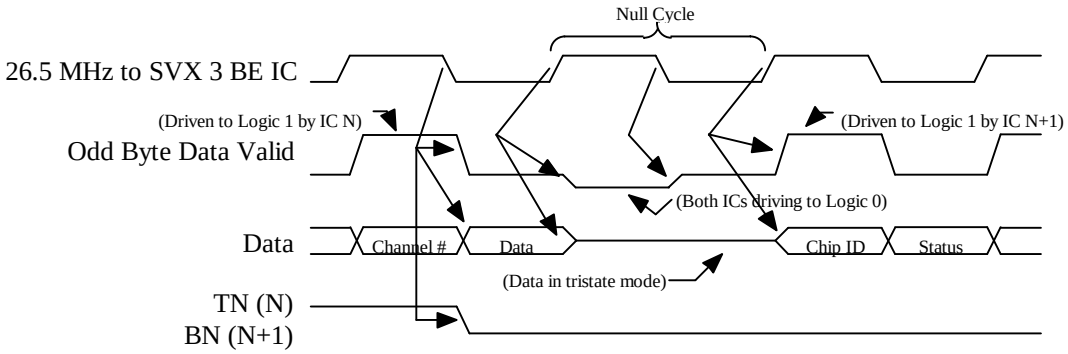

Figure 12. Operation of the OBDV between the Readout of Two Consecutive SVX3 Chips

When the SVX3 chips are not being readout, their OBDV outputs are tri-state and the differential voltage on these lines will be zero or very close to zero. At this moment, the output of the Dense Optical Interface Modules (DOIM), the units that will be used to transmit the data from the PC to the FIB will be unknown. Therefore, we need to use the DDR chip to avoid this situation. The DDR chip will be asserting the differential OBDV lines when the SVX3 chips are not being readout.

Figure 13 shows the connection of the OBDV lines among the SVX3 chips, the DOIM and the DDR chip. Note that we have shown just two chips. On a real application, we will have more chips connected on the readout chain.

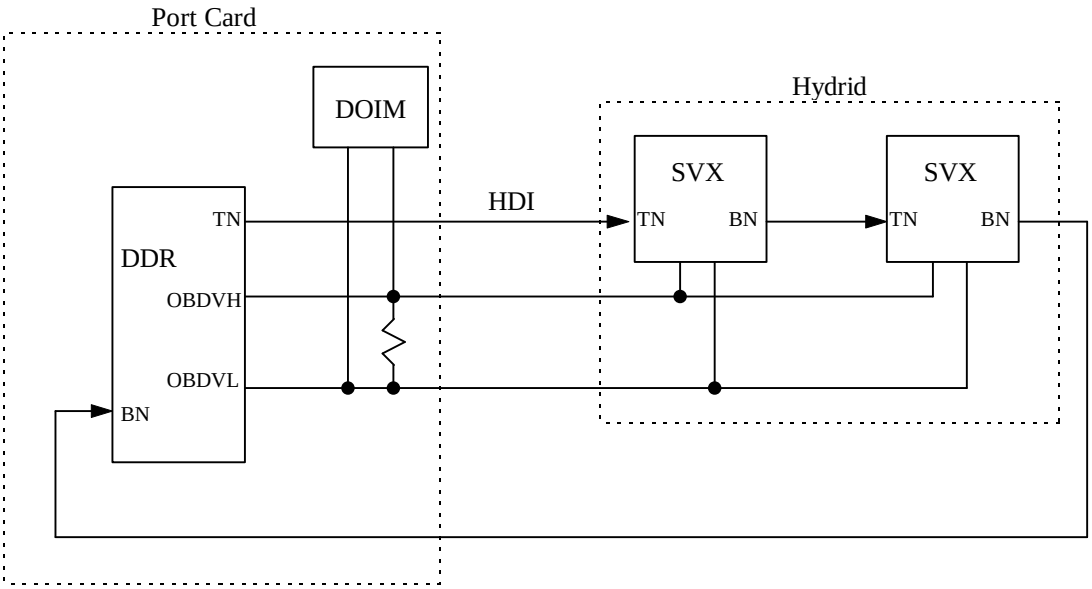

Figure 13. Connection of the OBDV between the DDR and SVX3 chips

To assert the OBDV line, the DDR chip has to respect a protocol compatible with the SVX3 chip. This protocol, similarly to the SVX3 chip, will be based on the BE_CLK, the TN and BN. To explain how this protocol operates we will use Figure 14, where we have number each transition of the BE_CLK. This figure shows the operation of the DDR chip by itself, without depicting the behavior of the OBDV lines when they are connected with the SVX3 chips.

(a) The SVX3 chips are not being readout and the DDR chip is asserting the OBDV lines to logical 0.
(b) The FIB controls the DDR chip to initiate the readout by asserting TN to 0. Then, it delivers the BE_CLK.
(c) On the falling edge of the BE_CLK (#2), the DDR chip tri-state the OBDV lines.
(d) When the last SVX3 chip in the chain is readout, it asserts the BN line to 0.
(e) On the next rising edge of the BE_CLK (#5), the DDR chip asserts again the OBDV to 0. Now the SVX3 chip can release the OBDV lines.

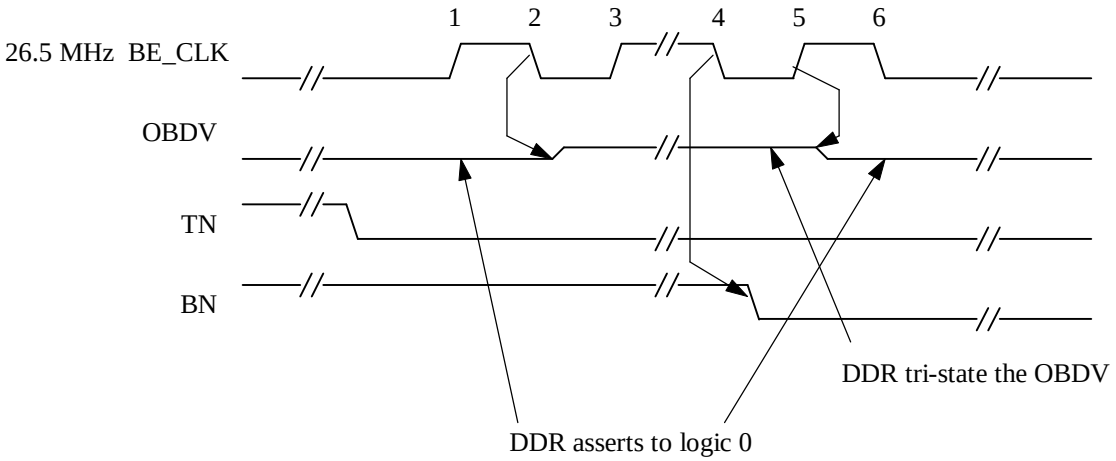

Figure 14. DDR Control of the OBDV when It Is Not Connected with the SVX3 Chips

We will now describe the operation of the OBDV on the beginning and end of readout when the DDR and SVX3 chips are connected together. This is depicted in Figure 15.

(a) Before the rising edge #1, the DDR chip is driving the OBDV.
(b) The FIB controls the DDR chip to initiate the readout by asserting TN to 0. Then, it delivers the BE_CLK.
(c) On the rising edge of the BE_CLK (#1), the first SVX3 chip in the chain drives the OBDV line. Now, the DDR and the first SVX3 chip in the chain are driving the OBDV.
(d) On the falling edge of the BE_CLK (#2), the DDR chip tri-state the OBDV lines.
(e) On the following clocks, the SVX3 chips takes control of the OBDV and use it to validate the data.
(f) When the last SVX3 chip in the chain is readout, it asserts the BN line to 0.
(g) On the rising edge #5, the DDR chip asserts again the OBDV to 0. Now, the DDR and the first SVX3 chip in the chain are driving the OBDV.
(h) On the falling edge #6, the SVX3 chip releases the OBDV lines.

For more details on the implementation of this circuitry, see the block diagram of Appendix A.

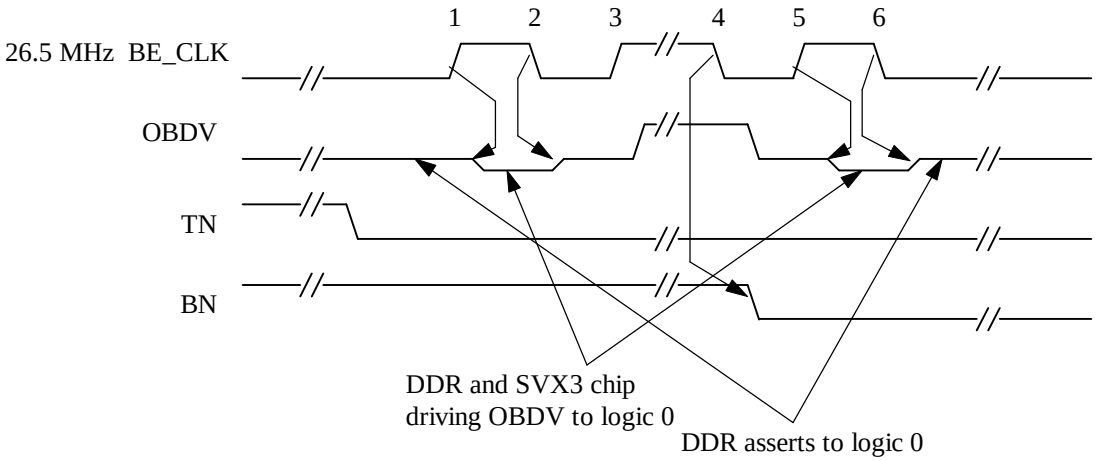

Figure 15. Operation of the OBDV on the Beginning and End of Readout, DDR and SVX3 chips Connected Together

11. ANALOG MULTIPLEXER

The digital to analog converter of the DDR chip (described in Section 8) generates the analog reference used for the calibration of the SVX3 chips. The SVX3 chip have a specific acquisition sequence where it samples its calibration input and, later on, the sampled voltage can be converted from analog to digital and read out. The calibration input of the SVX3 chip can be use for other purposes than just measuring the calibration voltage of the DDR chip. Any voltage with suitable level can be connected to this input, converted to digital and read out through the SVX3 chip.

This characteristic allow us to add a diagnostic feature to the DDR chip: we can use the calibration input of the SVX3 chips to read out the power supply voltages of the PC. By this reason, we have added an analog multiplexer, which allows the DDR chip to deliver different analog voltages through its calibration output (CAL_OUT) line. The analog multiplexer is depicted in Figure 2 and Figure A.1.

The inputs of the analog multiplexer are connected to the analog to digital converter (DAC_OUT) of the DDR chip and to three voltage dividers. These voltage dividers divide the voltages AV_{DD}, AV_{DD2}, and DV_{DD}, generating then the suitable voltage levels for the calibration input of the SVX3 chips (see Figure A.1). Depending on the multiplexer voltage input, we divide the voltage by different ratios. Table 12 shows these ratios, and they are such that the output voltage is close to 2.7V for AV_{DD} and DV_{DD} = 5.0 V and AV_{DD2} = 3.5V. Observe that this table assumes that AV_{DD2} will be used, but this may not be the case. As was previously pointed out, we are studying the options to avoid this power supply.

Table 12 the signals Select 0 and 1 (S[0:1]) are used to select the output of the multiplexer (see Table 12). The output of the multiplexer connects to an analog buffer with gain “1”. This buffer is used solely to produce a low impedance output voltage for the CAL_OUT. Table 13 shows the electrical characteristics of the voltage divider and buffer.

Table 12. Function Table

Select 1 (S1)	Select 0 (S0)	Output
0	0	DAC_OUT
0	1	AVDD/1.85
1	0	AVDD2/1.30
1	1	DVDD/1.85

Table 13. Characteristics of the Voltage Divider and Buffer

Characteristic	Min	Max	Unit
Divide ratio	9.9	10.1	Times
Buffer gain	0.999	1.001	Times
Buffer drift		100	µV/°C
Buffer offset		30	mV

AV_{DD}=5V±5%, T_j=5°C to +65°C

12. ELECTRICAL CHARACTERISTICS OF THE DIGITAL LINES

We will now specify the electrical characteristics of the single ended and differential inputs and outputs of the DDR lines.

12.1 Single Ended Lines

All the single ended lines must be TTL compatible. Table 14 and Table 15 describe the details of the requirements of the single ended lines.

Table 14. Electrical Characteristics of the Single Ended Inputs

Symbol	Parameter	Conditions	Min	Max	Units
V_{EDH}	Enable high level input voltage	V_{CC} = 5.25 V	2		V
V_{EDL}	Enable low level input voltage	V_{CC} = 4.75 V		0.8	V
I_{EDH}	Enable high level input current	V_{CC} = 5.25 V		40	µA
I_{EDL}	Enable low level input current	V_{CC} = 4.75 V		-1.6	mA
C_{IN}	Input capacitance			3	pF

DV_{DD}=5V±5%, T_A=5°C to +65°C,

Table 15. Electrical Characteristics of the Single Ended Outputs

Symbol	Parameter	Conditions	Min	Max	Units
V_{OL}	Output voltage low	V_{CC} = 5.25 V I_{OL} = 10 mA	0.2	0.4	V
V_{OH}	Output voltage high	V_{CC} = 4.75 V I_{OH} = - 10 mA	2.4	4.0	V
t_{Of}	Fall time	C_L= 20pF, R_{LOAD} = 500Ω[4]	1	3	ns
t_{Or}	Rise time	C_L= 20pF, R_{LOAD} = 500Ω[5]	1	3	ns

DV_{DD}=5V±5%, T_A=5°C to +65°C

12.2 Differential Lines

All differential lines must conform with the Low Current Differential Signals (LCDS) electrical protocol [4]. The main characteristics of this protocol are the following:

a) Specified for a maximum frequency of 53 MHz.
b) Differential current signals, with small adjustable current swing for optimization of low EMI radiation and power dissipation.
c) Receivers with selectable hysteresis.
d) Unidirectional or bi-directional operation (if enables are used)
e) Driver and receiver with controllable tri-state output mode.
f) Specified minimum and maximum rise and fall times.

[4]Fall time is the time the output takes to fall from 2.4 V to 0.4 V.
[5]Rise time is the time the output takes to rise from 2.4 V to 0.4 V.

g) Intended for cables with characteristic impedance between 25 Ω to 120 Ω.
h) Allows for different types of cable termination.

13. POWER SUPPLY CONSUMPTION

The power supply consumption of the DDR chip should be as small as possible. The PC will accommodate five DDR chip, and it is important to have small consumption to avoid excessive power dissipation.

14. PIN ASSIGNMENT AND PACKAGING DIMENSIONS

The die size is 2800 x 2835 um, with 150 um pad pitch. Figure 16 shows the pad assignment and location. In Figure 16, there are four corner pads. The pad pitch of these four corner pads are describe in Table 16.

Table 16. Corner Pads Location

Pad location	μm
DVDD2 to CAL_OUT	151.2
V1_TRIM to DVDD2	216.8
OBDVH to AVDD2	234.4
AVDD2 to COMP_REFL	216.8
IBE_CLKH to AVDD	233.2
AVDD to I_CLK	234
BE_MODE to VREF	252
VREF to CAL_SR	233.2

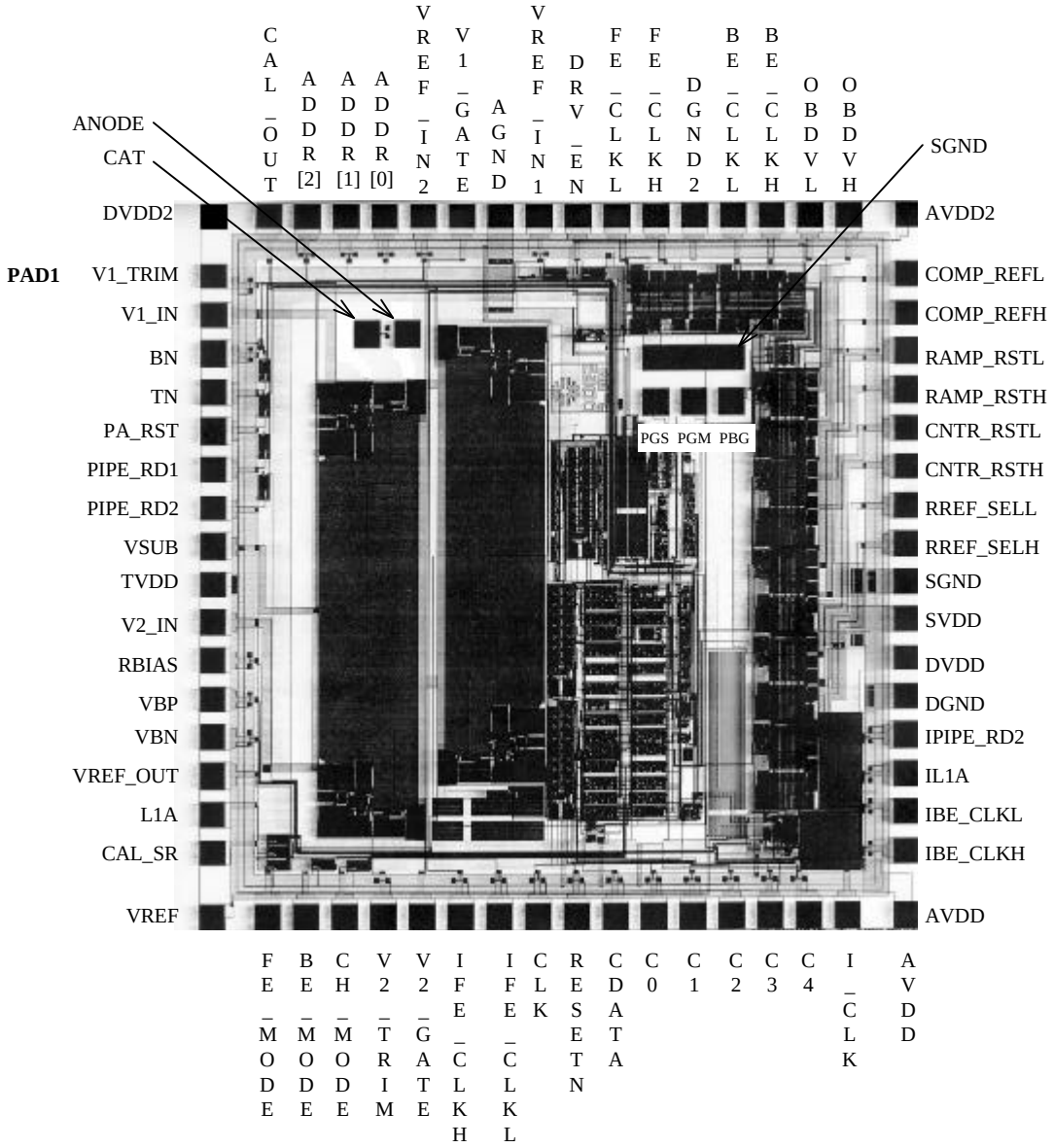

Figure 16. DDR pad assigment

Below, the description of the pads, starting at PAD 1 and going counter clock wise:

1. V1_TRIM: Voltage Trim 1 is inverting input of the Op. Amp.

2. V1_IN: Op. Amp. power supply1, which can be ramped 0 to 5V or 0 to 3.5V.

3. BN: Bottom Neighbor, digital input.

4. TN: Top Neighbor, buffered output. This bit is set or reset by using proper code on the C[0:4] and setting proper logic level at CDATA.

5. PA_RST: Preamp Reset. This bit is set or reset by using proper code on the C[0:4] and setting proper logic level at CDATA.

6. PIPE_RD1: Pipeline Read 1, buffered output. This bit is set or reset by using proper code on the C[0:4] and setting proper logic level at CDATA.

7. PIPE_RD2: Pipeline Read 2, buffered output.

8. VSUB: Substrate connection. Connect directly to Analog Ground.

9. TVDD: +5V power supply of Transceiver Chip.

10. V2_IN: Op. amp. power supply2 and voltage reference power supply2, which can be ramped 0 to 5V or 3 to 3.5V.

11. RBIAS: Input, connect a 33 Ω resistor to AGND to provide the bias to the driver circuit.

12. VBP: Input, this is generated internally to set the current at the output of the differential driver circuit.

13. VBN: Input, this is generated internally to set the current at the output of the differential driver circuit.

14. VREF_OUT: Output of band gap voltage reference.

15. L1A: Level 1 Accept, buffered output.

16. CAL_SR: Calibration or Serial Configuration Strobe. This bit is set or reset by using proper code on the C[0-4] and setting the proper logic level at CDATA.

17. VREF: Input, voltage reference for the driver bias circuit. 2.5V is generated internally.

18. FE_MODE: Front End Mode, buffered output. This bit is set or reset by using proper code on the C[0-4] and setting the proper logic level at CDATA.

19. BE_MODE: Back End Mode, buffered output. This bit is set or reset by using proper code on the C[0-4] and setting the proper logic level at CDATA.

20. CH_MODE: Change Mode. This bit is set or reset by using proper code on the C[0-4] and setting the proper logic level at CDATA.

21. V2_TRIM: Voltage Trim 2 is inverting input of Op. Amp.

22. V2_GATE: Voltage Gate 2 is output of Op. Amp.

23. IFE_CLKH: Differential input Front_end Clock High.

24. IFE_CLKL: Complement of Front_end Clock High.

25. CLK: Input, FFs make transition on rising edge of clock (53 MHZ).

26. RESETN: Input reset not. Need external capacitor to generate a power on reset. A logic level "0" will reset or preset all the FFs. It has an internal pull-up resistor connected to DVDD. The reset circuitry contains Schmitt trigger. The trip voltage for positive going input is 3V and for negative going input is 2V. Minimum pulse width is 15 ns.

27. CDATA: Input Control Data, logical level "1" or "0" should be set prior to the clock.

28-32. C[0:4]: Five bit input select signals(C[0] = LSB) can form 32 different instructions. For each of the 32 codes, one and only one line is changed.

33. I_CLK: An output test pin. This is an internal clock for the FFs. (Not used in the final chip)

34. AVDD: +5V analog power supply.

35. IBE_CLKH: Differential input Back_end Clock High.

36. IBE_CLKL: Complement of Back_end Clock High.

37. IL1A: Level 1 Accept, digital input (0-5V).

38. IPIPE_RD2: Pipeline Read 2, digital input (0-5V).

39. DGND: Digital ground.

40. DVDD: +5V digital power supply.

41. SVDD: +5V output driver power supply. It should be connected to digital power supply.

42. SGND: Output driver ground. It should be connected to digital ground.

43. RREF_SELH: Ramp Reference Select High.

44. RREF_SELL: Complement of Ramp Reference Select High.

45. CNTR_RSTH: Counter Reset High

46. CNTR_RSTL: Complement of Counter Reset High.

47. RAMP_RSTH: Ramp Reset High.

48. RAMP_RSTL: Complement of Ramp Reset High.

49. COMP_RSTH: Comparator Reset High.

50. COMP_RSTL: Complement of comparator Reset High.

51. AVDD2: +3.5V analog power supply.

52. OBDVH: Differential Odd Byte Data Valid High, driver output, the output is either tristate or active low.

53. OBDVL: Complement of Odd Byte Data Valid.

54. BE_CLKH: Back_End Clock High,

55. BE_CLKL: Complement of Back_end Clock High.

56. DGND2: Digital ground.

57. FE_CLKH: Differential output, Front End Clock High,

58. FE_CLKL: Complement of Front End Clock High.

59. DRV_EN: Driver Enable.

60. VREF_IN1: Input, Voltage reference for Op. Amp. connected to non-inverting terminal.

61. AGND: Analog Ground. Connect directly to the analog ground plane.

62. V1_GATE: Voltage Base 1 is output of Op. Amp.

63. VREF_IN2: Input, Voltage reference for Op. Amp. connected to non-inverting terminal.

64-66. ADDR[0:2]: Digital input (ADDR[0]=LSB) to select one specific DDR chip (one of five). They have internal pull-up resistors connected to DVDD. In order to select specific DDR, one needs to select proper DDR address and set DDR[1-5].

67. CAL_OUT: Output, Calibration Reset Output. Different analog voltages are driven in this line (DAC output and three voltage dividers).

68. DVDD2: +5V digital power supply.

There are 6 pads which are placed inside the chip and are listed below:

PGS, PGM PBG: Programmable output driver resistor. Can be jumped to SGND to adjust the output current.

SGND: Output driver ground.

CAT: Cathode of the series diodes.

ANODE: Anode of the series diodes.

15. REFERENCES

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[3] Zimmermann, S., "Port Card", Fermilab document.

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[5] Barsotti, E. and Zimmermann, S., "Low Current Differential Signals", Fermilab Document.

[6] Siliconix Data Book

[7] Barsotti, E. and Zimmermann, S., "Changes to the BE CHip of the SVX 3 Chip Set", Doc. # ESE-SVX-960411, Fermilab, 1996.

[8] E-mails and conversations with Jeff Spalding, 1995.

16. CHANGES IN RELATION TO ORIGINAL SPECIFICATIONS

1. The block diagram in Figure 2 and the circuit in Figure A.1 were updated.
2. The command codes in Table 2 was updated.
3. Section 5: add the Front End Clock enable and disable feature.
4. Upgrade Section 8, Digital to Analog Converter.
5. Change the name V1_BASE to V1_GATE and V2_BASE to V2_GATE (Section 9, Figure 2 AND Figure A.1).
6. Upgrade Section 9 to observe that just one voltage regulator may be used. Other minor upgrades.
7. Comments about C_R in Section 9.
8. The output TN_EN and associated FF was deleted (Section 14, Figure 2 and Figure A.1).
9. Add pads for V_{REF} and all inputs of the pre-amplifiers (Figure A.1).

10. An inverter was included in the EN (enable) input of the FF that controls the tri-state of the OBDVH and OBDVL lines.
11. Analog buffer between the output of the multiplexer and the output CAL_OUT was added.
12. Timing tables were upgraded.
13. Section 14 includes the picture of the die. The pin sequence and dimensions of the chip was added

17. APPENDIX A

Figure A.1 shows the schematic of the DDR chip.

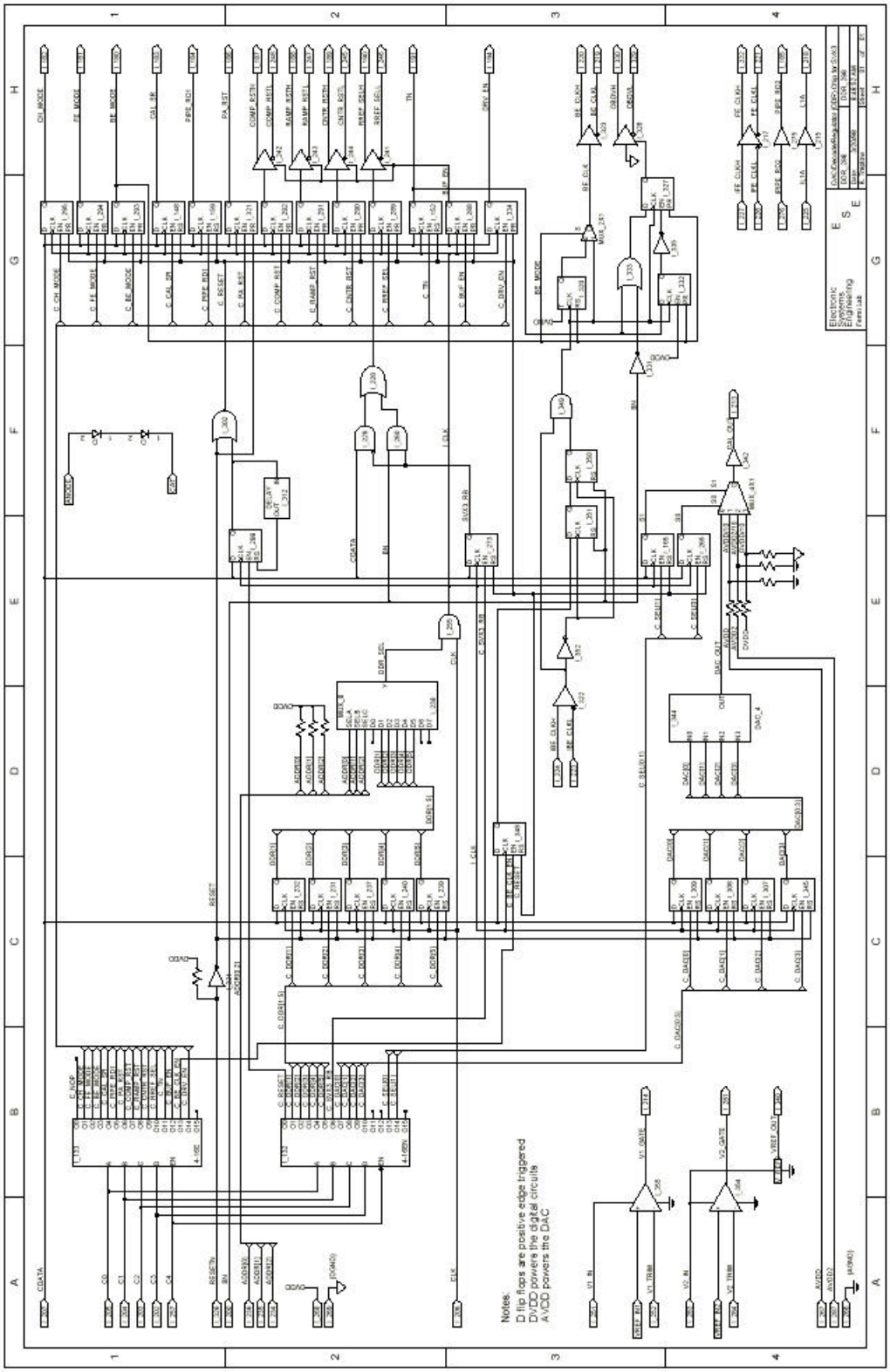

Figure A.1. Schematics of the DDR Chip