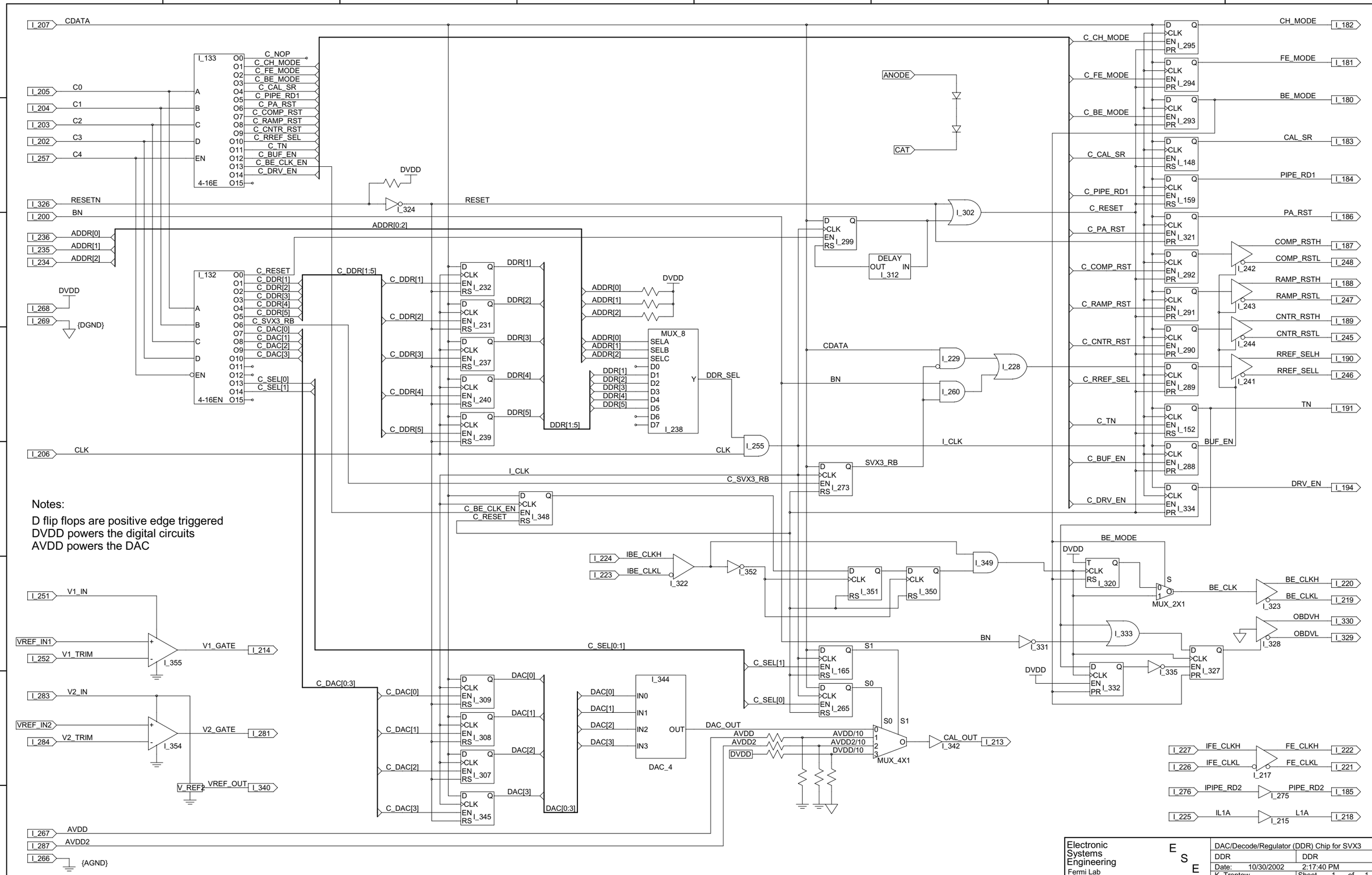
I_207 CDATA
I_205 C0
I_204 C1
I_203 C2
I_202 C3
I_257 C4
I_133 4-16E
C_NOP
C_CH_MODE
C_FE_MODE
C_BE_MODE
C_CAL_SR
C_PIPE_RD1
C_PA_RST
C_COMP_RST
C_RAMP_RST
C_CNTR_RST
C_RREF_SEL
C_TN
C_BUF_EN
C_BE_CLK_EN
C_DRV_EN
DVDD
I_324
I_326 RESETN
I_200 BN
RESET
ADDR[0:2]
I_236 ADDR[0]
I_235 ADDR[1]
I_234 ADDR[2]
I_132 4-16EN
C_RESET
C_DDR[1]
C_DDR[2]
C_DDR[3]
C_DDR[4]
C_DDR[5]
C_SVX3_RB
C_DAC[0]
C_DAC[1]
C_DAC[2]
C_DAC[3]
C_SEL[0]
C_SEL[1]
I_268 DVDD
I_269 {DGND}
C_DDR[1:5]
I_232
I_231
I_237
I_240
I_239
DDR[1]
DDR[2]
DDR[3]
DDR[4]
DDR[5]
DDR[1:5]
MUX_8
SELA
SELB
SELC
D0
D1
D2
D3
D4
D5
D6
D7
Y
I_238
DDR_SEL
I_255
I_206 CLK
I_CLK
C_SVX3_RB
I_348
C_BE_CLK_EN
C_RESET
I_273
SVX3_RB
ANODE
CAT
I_299
DELAY
OUT IN
I_312
I_302
CDATA
BN
I_229
I_260
I_228
I_295
I_294
I_293
I_148
I_159
I_321
I_292
I_291
I_290
I_289
I_152
I_288
I_334
CH_MODE
FE_MODE
BE_MODE
CAL_SR
PIPE_RD1
PA_RST
COMP_RSTH
COMP_RSTL
RAMP_RSTH
RAMP_RSTL
CNTR_RSTH
CNTR_RSTL
RREF_SELH
RREF_SELL
TN
BUF_EN
DRV_EN
I_182
I_181
I_180
I_183
I_184
I_186
I_187
I_248
I_188
I_247
I_189
I_245
I_190
I_246
I_191
I_194
I_242
I_243
I_244
I_241
Notes:
D flip flops are positive edge triggered
DVDD powers the digital circuits
AVDD powers the DAC
I_224 IBE_CLKH
I_223 IBE_CLKL
I_322
I_352
I_351
I_350
I_349
BE_MODE
I_320
MUX_2X1
BE_CLK
I_323
BE_CLKH
BE_CLKL
I_220
I_219
I_333
I_328
OBDVH
OBDVL
I_330
I_329
I_331
I_327
I_332
I_335
I_251 V1_IN
VREF_IN1
I_252 V1_TRIM
I_355
V1_GATE
I_214
I_283 V2_IN
VREF_IN2
I_284 V2_TRIM
I_354
V2_GATE
I_281
V_REF2
VREF_OUT
I_340
C_SEL[0:1]
C_DAC[0:3]
I_309
I_308
I_307
I_345
DAC[0]
DAC[1]
DAC[2]
DAC[3]
DAC[0:3]
I_344
IN0
IN1
IN2
IN3
OUT
DAC_4
DAC_OUT
I_165
I_265
S1
S0
AVDD
AVDD2
DVDD
AVDD/10
AVDD2/10
DVDD/10
MUX_4X1
CAL_OUT
I_342
I_213
I_227 IFE_CLKH
I_226 IFE_CLKL
I_217
FE_CLKH
FE_CLKL
I_222
I_221
I_276 IPIPE_RD2
I_275
PIPE_RD2
I_185
I_225 IL1A
I_215
L1A
I_218
I_267 AVDD
I_287 AVDD2
I_266 {AGND}
Electronic
Systems
Engineering
Fermi Lab
DAC/Decode/Regulator (DDR) Chip for SVX3
DDR
DDR
Date: 10/30/2002
2:17:40 PM
K. Treptow
Sheet 1 of 1