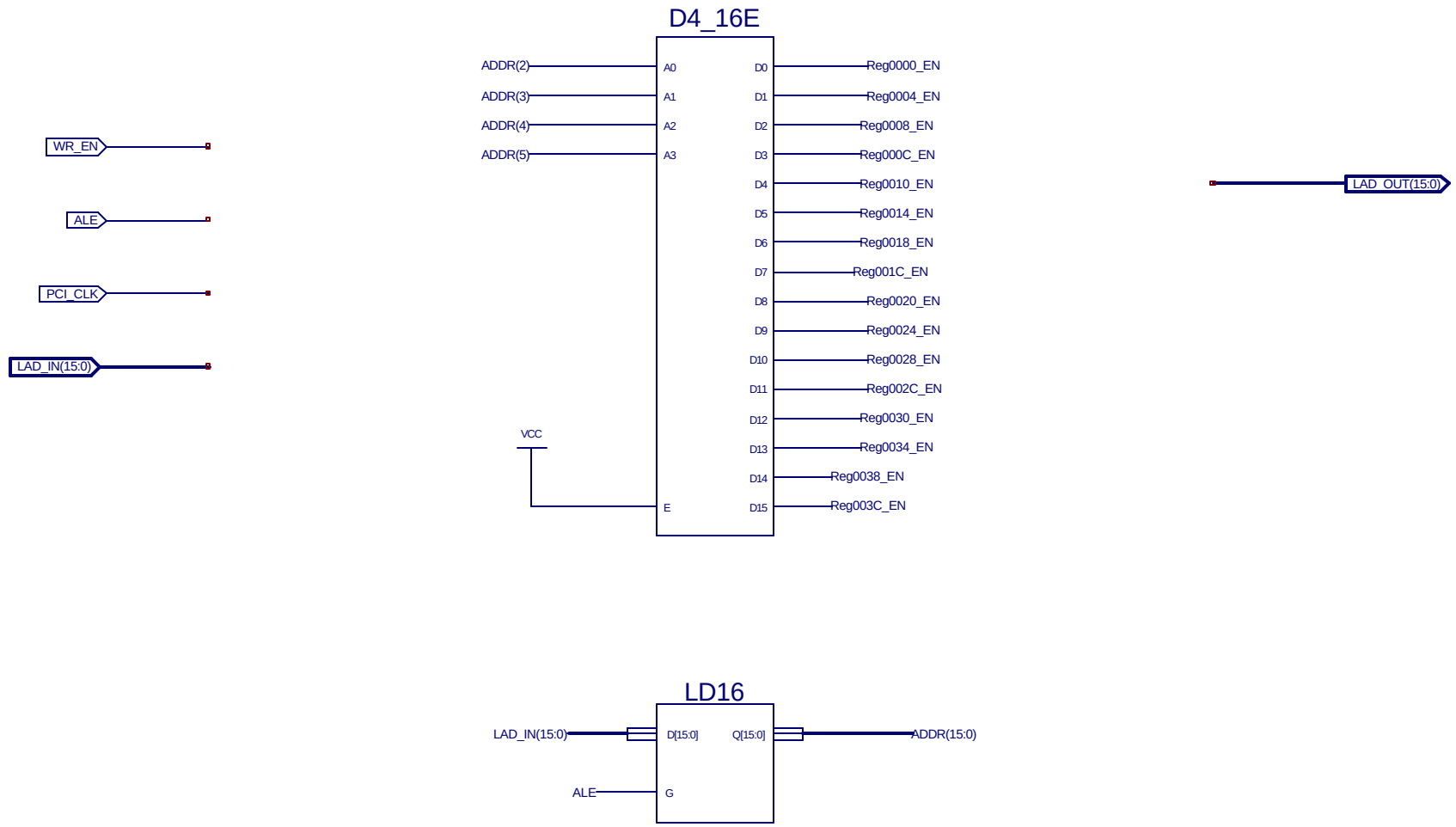
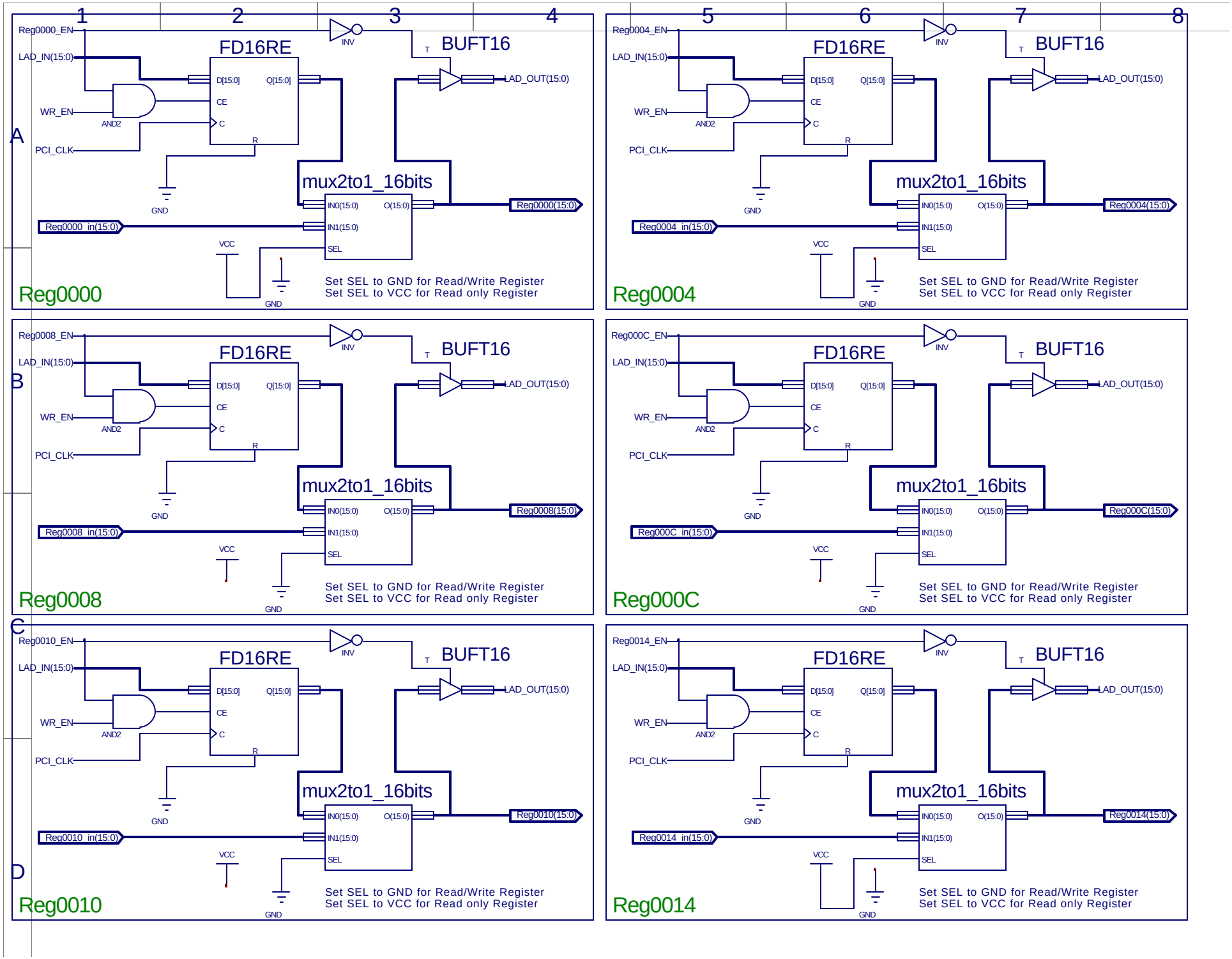
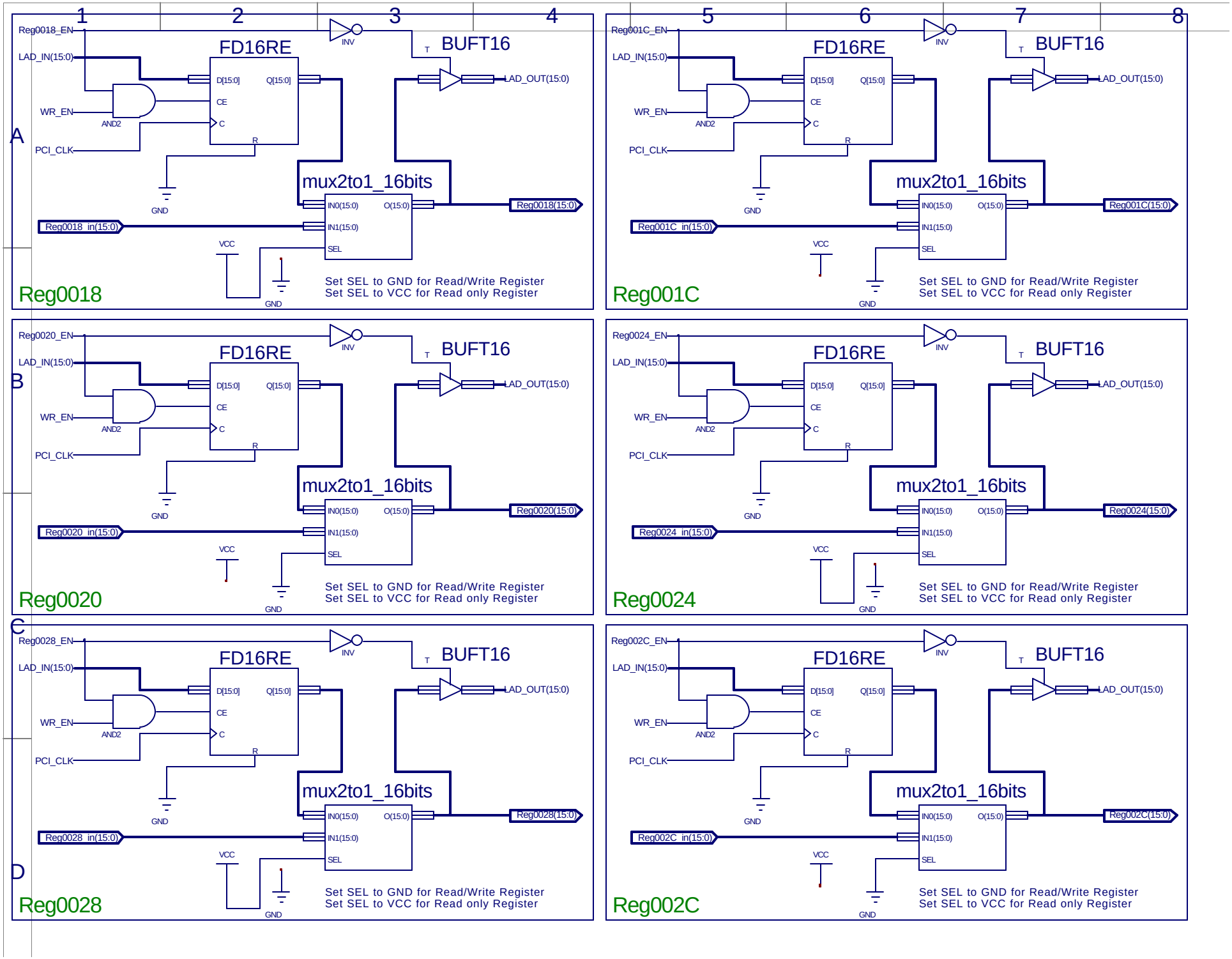
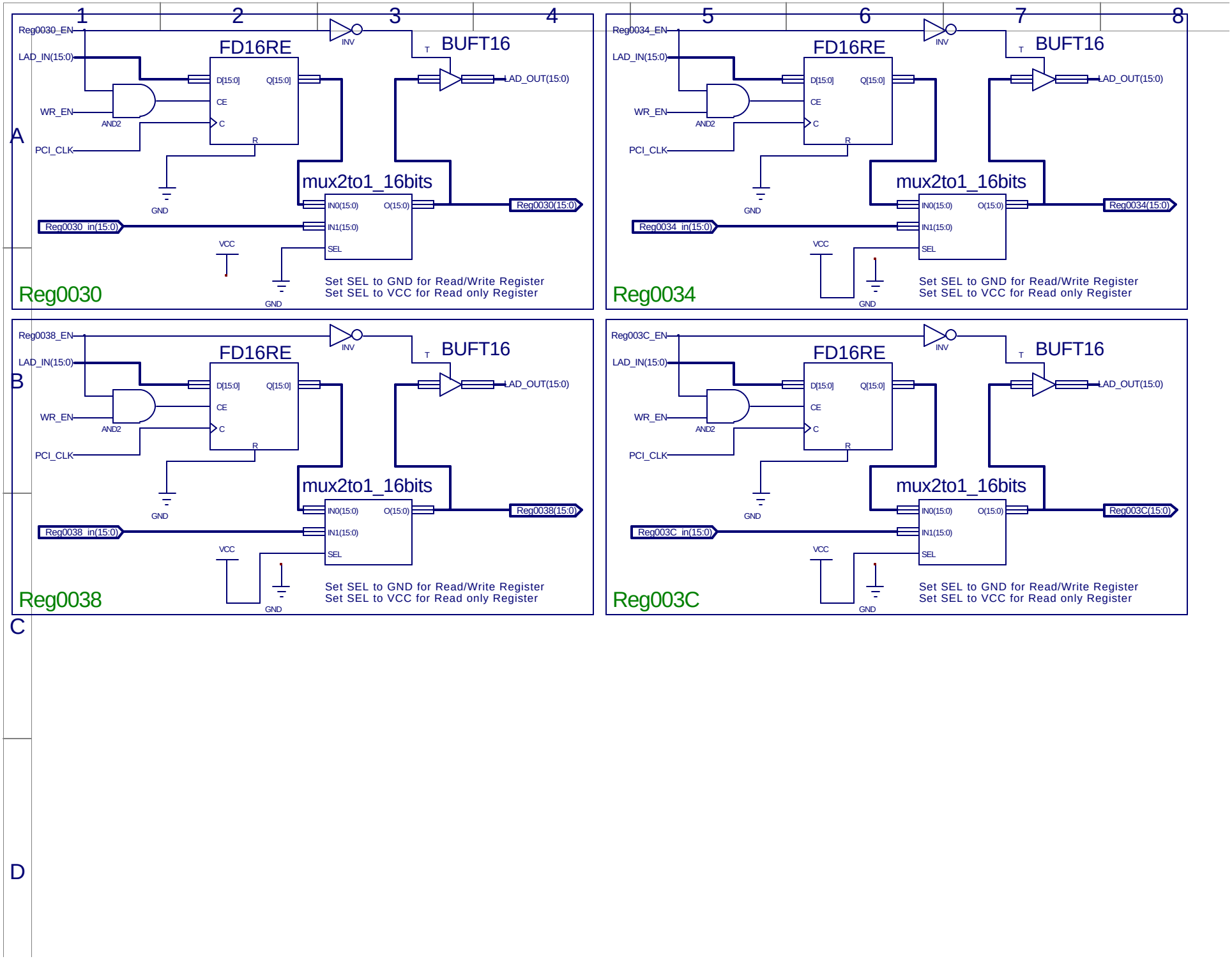


XILINX

Title:	PMC Registers for Loop Back Test
Name:	Bradley Hall Cable Loop Back Test Rev1.0
Date:	Feb 19, 2002
Sheet	1 of 4


1
2
3
4
5
6
7
8
A
B
C
D
Reg0000_EN
LAD_IN(15:0)
WR_EN
PCI_CLK
FD16RE
D[15:0]
Q[15:0]
CE
C
R
AND2
INV
BUFT16
T
LAD_OUT(15:0)
GND
mux2to1_16bits
IN0(15:0)
O(15:0)
IN1(15:0)
SEL
Reg0000(15:0)
Reg0000_in(15:0)
VCC
Reg0000
Set SEL to GND for Read/Write Register
Set SEL to VCC for Read only Register
Reg0004_EN
Reg0004(15:0)
Reg0004_in(15:0)
Reg0004
Reg0008_EN
Reg0008(15:0)
Reg0008_in(15:0)
Reg0008
Reg000C_EN
Reg000C(15:0)
Reg000C_in(15:0)
Reg000C
Reg0010_EN
Reg0010(15:0)
Reg0010_in(15:0)
Reg0010
Reg0014_EN
Reg0014(15:0)
Reg0014_in(15:0)
Reg0014


1
2
3
4
5
6
7
8
A
B
C
D
Reg0018_EN
LAD_IN(15:0)
WR_EN
PCI_CLK
FD16RE
D[15:0]
Q[15:0]
CE
C
R
AND2
INV
BUFT16
T
LAD_OUT(15:0)
GND
mux2to1_16bits
IN0(15:0)
O(15:0)
IN1(15:0)
SEL
Reg0018(15:0)
Reg0018_in(15:0)
VCC
Reg0018
Set SEL to GND for Read/Write Register
Set SEL to VCC for Read only Register
Reg001C_EN
Reg001C(15:0)
Reg001C_in(15:0)
Reg001C
Reg0020_EN
Reg0020(15:0)
Reg0020_in(15:0)
Reg0020
Reg0024_EN
Reg0024(15:0)
Reg0024_in(15:0)
Reg0024
Reg0028_EN
Reg0028(15:0)
Reg0028_in(15:0)
Reg0028
Reg002C_EN
Reg002C(15:0)
Reg002C_in(15:0)
Reg002C


1
2
3
4
5
6
7
8
A
B
C
D
Reg0030_EN
LAD_IN(15:0)
WR_EN
PCI_CLK
AND2
INV
FD16RE
D[15:0]
Q[15:0]
CE
C
R
GND
BUFT16
T
LAD_OUT(15:0)
mux2to1_16bits
IN0(15:0)
O(15:0)
IN1(15:0)
SEL
Reg0030(15:0)
Reg0030_in(15:0)
VCC
Reg0030
Set SEL to GND for Read/Write Register
Set SEL to VCC for Read only Register
Reg0034_EN
Reg0034(15:0)
Reg0034_in(15:0)
Reg0034
Reg0038_EN
Reg0038(15:0)
Reg0038_in(15:0)
Reg0038
Reg003C_EN
Reg003C(15:0)
Reg003C_in(15:0)
Reg003C