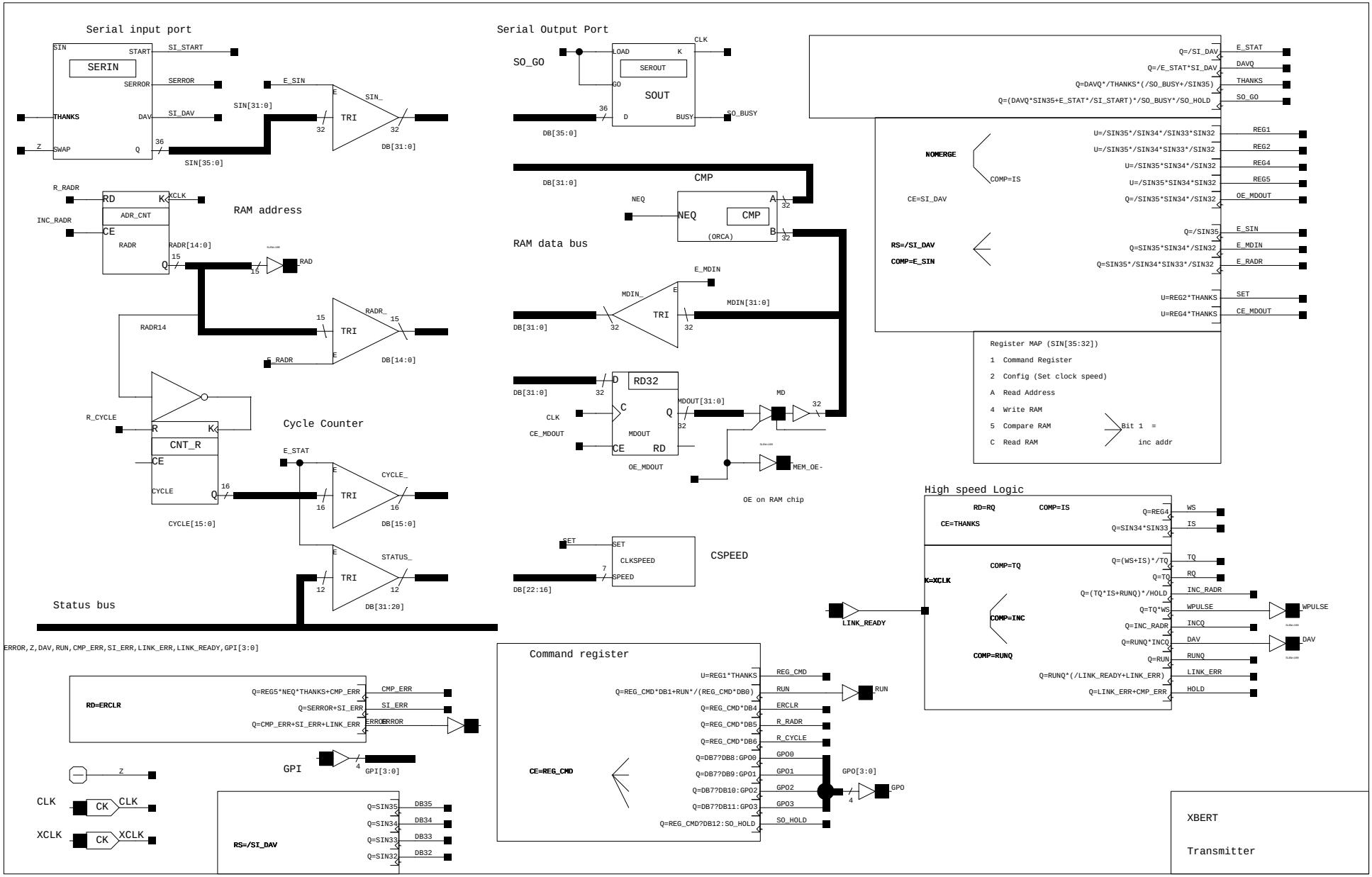
Serial input port
SERIN
SIN
START
SI_START
SERROR
THANKS
DAV
SI_DAV
Z
SWAP
Q
36
SIN[35:0]
SIN[31:0]
E_SIN
TRI
SIN_
32
DB[31:0]
R_RADR
RD
K
CLK
ADR_CNT
INC_RADR
CE
RADR
RADR[14:0]
15
RAD
RAM address
RADR14
RADR_
DB[14:0]
E_RADR
R_CYCLE
R
CNT_R
CYCLE
16
CYCLE[15:0]
Cycle Counter
E_STAT
CYCLE_
DB[15:0]
STATUS_
12
DB[31:20]
Status bus
ERROR,Z,DAV,RUN,CMP_ERR,SI_ERR,LINK_ERR,LINK_READY,GPI[3:0]
RD=ERCLR
Q=REG5*NEQ*THANKS+CMP_ERR
Q=SERROR+SI_ERR
Q=CMP_ERR+SI_ERR+LINK_ERR
CMP_ERR
SI_ERR
ERROR
GPI
4
GPI[3:0]
CLK
CK
XCLK
RS=/SI_DAV
Q=SIN35
Q=SIN34
Q=SIN33
Q=SIN32
DB35
DB34
DB33
DB32
Serial Output Port
SO_GO
LOAD
SEROUT
GO
SOUT
D
BUSY
SO_BUSY
DB[35:0]
CMP
NEQ
A
B
(ORCA)
RAM data bus
E_MDIN
MDIN_
MDIN[31:0]
RD32
MDOUT[31:0]
MD
MDOUT
RD
OE_MDOUT
MEM_OE-
OE on RAM chip
SET
CLKSPEED
SPEED
DB[22:16]
CSPEED
Command register
U=REG1*THANKS
Q=REG_CMD*DB1+RUN*/(REG_CMD*DB0)
Q=REG_CMD*DB4
Q=REG_CMD*DB5
Q=REG_CMD*DB6
Q=DB7?DB8:GPO0
Q=DB7?DB9:GPO1
Q=DB7?DB10:GPO2
Q=DB7?DB11:GPO3
Q=REG_CMD?DB12:SO_HOLD
REG_CMD
RUN
ERCLR
R_RADR
R_CYCLE
GPO0
GPO1
GPO2
GPO3
SO_HOLD
CE=REG_CMD
GPO[3:0]
GPO
Q=/SI_DAV
Q=/E_STAT*SI_DAV
Q=DAVQ*/THANKS*(/SO_BUSY+/SIN35)
Q=(DAVQ*SIN35+E_STAT*/SI_START)*/SO_BUSY*/SO_HOLD
E_STAT
DAVQ
THANKS
SO_GO
NOMERGE
COMP=IS
CE=SI_DAV
U=/SIN35*/SIN34*/SIN33*SIN32
U=/SIN35*/SIN34*SIN33*/SIN32
U=/SIN35*SIN34*/SIN32
U=/SIN35*SIN34*SIN32
Q=/SIN35*SIN34*/SIN32
REG1
REG2
REG4
REG5
OE_MDOUT
RS=/SI_DAV
COMP=E_SIN
Q=/SIN35
Q=SIN35*SIN34*/SIN32
Q=SIN35*/SIN34*SIN33*/SIN32
E_SIN
E_MDIN
E_RADR
U=REG2*THANKS
U=REG4*THANKS
SET
CE_MDOUT
Register MAP (SIN[35:32])
1 Command Register
2 Config (Set clock speed)
A Read Address
4 Write RAM
5 Compare RAM
C Read RAM
Bit 1 =
inc addr
High speed Logic
RD=RQ
COMP=IS
CE=THANKS
Q=REG4
Q=SIN34*SIN33
WS
IS
COMP=TQ
K=XCLK
Q=(WS+IS)*/TQ
Q=TQ
Q=(TQ*IS+RUNQ)*/HOLD
Q=TQ*WS
Q=INC_RADR
Q=RUNQ*INCQ
Q=RUN
Q=RUNQ*(/LINK_READY+LINK_ERR)
Q=LINK_ERR+CMP_ERR
TQ
RQ
INC_RADR
WPULSE
INCQ
DAV
RUNQ
LINK_ERR
HOLD
LINK_READY
COMP=INC
COMP=RUNQ
XBERT
Transmitter