



Fermi National Accelerator Laboratory

SNAP

Programmable Mezzanine Card (PMC) Firmware for
SNAP Memory Board Test.

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Document Revision History

Rev	Date	Author	Comments
1.0	7/23/03	B. Hall	Original
1.1	8/14/03	B. Hall	Changed directional signal for I/O bus from being a function of ALE_LVDS to being a function of TR_LVDS (Section 4).
1.2	8/27/03	B. Hall	Corrected typo in section 5.7 – Register 0x0018 (not 0x0014)
1.3	9/10/03	B. Hall	Added registers for connectors C, D, and E. Consistent with PMC firmware revisions 1.3.
1.4	9/11/03	B. Hall	Corrected register addressed for “D”

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1 Introduction

This document describes the hardware required and the functionality of the Programmable Mezzanine Card (PMC) firmware for connecting up to four SNAP Flash Memory RAD Test Board.

2 Hardware

In addition to the Memory Board under test, the following hardware is needed:

- PC with PTA (PCI Test Adapter) card and appropriated software to communicate with PTA card.
- PMC (Programmable Mezzanine Card) loaded with “SNAP Memory Board” firmware and appropriate termination resistor arrangement as described in the next section.
- One 25 mil pitch Hitachi cable (Hitachi Part #23195-050) with SAMTEC IDC terminations (SAMTEC Part #FFSD-25-01-N) to connect the Memory board to the PMC SAMTEC “A” header.

3 PMC Termination Resistors

All signals between the PMC and the Memory Board are LVDS. LVDS signals on the PMC are terminated via a parallel 100Ohm resistor. The table below describes the appropriate termination resistor configuration on the PMC:

PMC Resistor Configuration for “A” Connector

<i>Resistor</i>	<i>Action</i>	<i>Signal Direction</i>	<i>Signal</i>
R75	Remove	O	TR_LVDS
R55	Remove	O	CE_LVDS
R59	Remove	O	CLE_LVDS
R71	Remove	O	ALE_LVDS
R76	Remove	O	RE_LVDS
R56	Remove	O	WE_LVDS
R72	Remove	O	WP_LVDS
R60	Install	I	RB_LVDS
R57	Install	I/O	IO_LVDS(0)
R73	Install	I/O	IO_LVDS(1)
R77	Install	I/O	IO_LVDS(2)
R74	Install	I/O	IO_LVDS(3)
R61	Install	I/O	IO_LVDS(4)
R58	Install	I/O	IO_LVDS(5)
R78	Install	I/O	IO_LVDS(6)
R62	Install	I/O	IO_LVDS(7)

PMC Resistor Configuration for “B” Connector

<i>Resistor</i>	<i>Action</i>	<i>Signal Direction</i>	<i>Signal</i>
R67	Remove	O	TR_LVDS
R70	Remove	O	CE_LVDS
R66	Remove	O	CLE_LVDS
R69	Remove	O	ALE_LVDS
R82	Remove	O	RE_LVDS
R47	Remove	O	WE_LVDS
R68	Remove	O	WP_LVDS
R65	Install	I	RB_LVDS
R86	Install	I/O	IO_LVDS(0)
R81	Install	I/O	IO_LVDS(1)
R48	Install	I/O	IO_LVDS(2)
R85	Install	I/O	IO_LVDS(3)
R64	Install	I/O	IO_LVDS(4)
R54	Install	I/O	IO_LVDS(5)
R84	Install	I/O	IO_LVDS(6)
R80	Install	I/O	IO_LVDS(7)

PMC Resistor Configuration for “C” Connector

<i>Resistor</i>	<i>Action</i>	<i>Signal Direction</i>	<i>Signal</i>
R3	Remove	O	TR_LVDS
R24	Remove	O	CE_LVDS
R23	Remove	O	CLE_LVDS
R11	Remove	O	ALE_LVDS
R31	Remove	O	RE_LVDS
R6	Remove	O	WE_LVDS
R10	Remove	O	WP_LVDS
R29	Install	I	RB_LVDS
R9	Install	I/O	IO_LVDS(0)
R32	Install	I/O	IO_LVDS(1)
R5	Install	I/O	IO_LVDS(2)
R8	Install	I/O	IO_LVDS(3)
R30	Install	I/O	IO_LVDS(4)
R7	Install	I/O	IO_LVDS(5)
R34	Install	I/O	IO_LVDS(6)
R4	Install	I/O	IO_LVDS(7)

PMC Resistor Configuration for “D” Connector

<i>Resistor</i>	<i>Action</i>	<i>Signal Direction</i>	<i>Signal</i>
R52	Remove	O	TR_LVDS
R50	Remove	O	CE_LVDS
R46	Remove	O	CLE_LVDS
R51	Remove	O	ALE_LVDS
R43	Remove	O	RE_LVDS
R45	Remove	O	WE_LVDS
R40	Remove	O	WP_LVDS
R49	Install	I	RB_LVDS
R41	Install	I/O	IO_LVDS(0)
R42	Install	I/O	IO_LVDS(1)
R35	Install	I/O	IO_LVDS(2)
R36	Install	I/O	IO_LVDS(3)
R39	Install	I/O	IO_LVDS(4)
R33	Install	I/O	IO_LVDS(5)
R37	Install	I/O	IO_LVDS(6)
R38	Install	I/O	IO_LVDS(7)

4 General Description

The PMC firmware contains both read only registers and read/write registers that are accessible via software. Signals for each of the four Memory Boards are connected to bits on four separate PMC registers (sixteen total). The seven control signals from the PMC to the Memory Board (TR_LVDS, CE_LVDS, CLE_LVDS, ALE_LVDS, RE_LVDS, WE_LVDS, and WP_LVDS) are connected to seven bits on a read/write register. The one control signal from the Memory Board to the PMC (RB_LVDS) is connected to a bit on a read only register.

The seven bit data bus is bidirectional. The direction of the I/O drivers on the PMC are controlled through an internal direction signal that is a function of the TR_LVDS signal and a delay signal. On the Memory Board, the U1 LVDS Transceiver drives or receives the eight-bit IO_LVDS data bus. When TR_LVDS is a logic '0' The Transceiver_T/R signal on the Memory board is a logic '0' resulting in U1 being configured to receive signals from the PMC. Conversely, when TR_LVDS is a logic '1', U1 is configured to drive signals to the PMC.

Logic in the PMC switches the PMC I/O bus to “receive” as soon as the TR_LVDS signal is a logic '1'. In this state, the Memory Board is driving the IO_LVDS signals to the PMC. When the TR_LVDS signal switches to a logic “0”, the PMC I/O bus stays in the “receive” direction and starts a delay counter. At this point, both the PMC and the Memory board are in “receive” mode. When the delay counter reaches the count that is set in the delay count register (this is a read-only register with a value hardwired in the firmware), the PMC I/O switches to a “drive” direction. The purpose of this delay is to eliminate possible bus contention during the bus turnaround.

5 Registers

5.1 PMC Firmware Type

This is a read only register that contains the PMC firmware type. The value of this register for the SNAP Memory Test application should always read 0x0011.

<i>Register 0x0000 (Read Only)</i>	
<i>Bit #</i>	<i>Meaning</i>
15..0	PMC Type: 0x0000 = Undefined 0x0001 = Cable loop back test 0x0002 = FPIX0 test beam '02 0x0003 = FPIX1 test beam '02 0x0004 = preFPIX2 test beam '02 0x0005 = preFPIX2 old innerboard 0x0008 = FPIX2 Periphery BERT 0x0010 = SSR Chip 0x0011 = SNAP Memory Test

5.2 PMC Firmware Revision

This is a read only register that contains the PMC firmware revision. The lower 8 bits are the minor revision number while the upper 8 bits are the major revision.

<i>Register 0x0004 (Read Only)</i>	
<i>Bit #</i>	<i>Meaning</i>
7..0	Firmware Minor Revision
15..8	Firmware Major Revision

5.3 Delay Magnitude

This is a read only register that contains the magnitude of the delay. The delay signal is used as part of the IO signal direction to avoid bus contention during bus turnarounds. The value of the delay is 80ns * value in the Delay Register. The value of the delay can range from 0s to ~5.24ms.

<i>Register 0x0008 (Read Only) – Delay</i>	
<i>Bit #</i>	<i>Meaning</i>
15..0	Delay

5.4 Memory Board “A”

Memory board “A” should connect to the connector labeled SAMTEC “A” on the PMC.

5.4.1 Memory Board “A” Control - Outputs

The MemBrdCtlOUT register contains all control signals that are driven to the Memory Board. In addition, four bits in this register (bits 8 through 11) are sent to pins on the PMC TTL header for user defined purposes.

Register 0x000C (Read/Write) – MemBrdCtlOUT - A	
Bit #	Meaning
0	TR_LVDS
1	CE_LVDS
2	CLE_LVDS
3	ALE_LVDS
4	RE_LVDS
5	WE_LVDS
6	WP_LVDS
7	<i>Not Used</i>
8	TTL output J5 pin 1
9	TTL output J5 pin 3
10	TTL output J5 pin 5
11	TTL output J5 pin 7
15..12	<i>Not Used</i>

5.4.2 Memory Board “A” Control - Inputs

The MemBrdCtrlIN register contains the one control signal that is driven from the Memory Board to the PMC. In addition, four bits in this register (bits 8 through 11) are connected to pins on the PMC TTL header for user defined purposes.

Register 0x0010 (Read Only) – MemBrdCtrlIN - A	
Bit #	Meaning
0	RB_LVDS
7..1	<i>Not Used</i>
8	TTL input J5 pin 9
9	TTL input J5 pin 11
10	TTL input J5 pin 13
11	TTL input J5 pin 15
15..12	<i>Not Used</i>

5.4.3 Memory Board “A” IO Data - OUT

This register contains the eight bit data that is driven from the PMC to the Memory Board.

Register 0x0014 (Read/Write) – IO_OUT_LVDS - A	
Bit #	Meaning
0	IO_LVDS(0) - Output to Memory Board
1	IO_LVDS(1) - Output to Memory Board
2	IO_LVDS(2) - Output to Memory Board
3	IO_LVDS(3) - Output to Memory Board
4	IO_LVDS(4) - Output to Memory Board
5	IO_LVDS(5) - Output to Memory Board
6	IO_LVDS(6) - Output to Memory Board
7	IO_LVDS(7) - Output to Memory Board
15..8	<i>Not Used</i>

5.4.4 Memory Board “A” IO Data - IN

This register contains the eight bit data that is driven from the Memory Board to the PMC.

Register 0x0018 (Read Only) – IO_IN_LVDS- A	
Bit #	Meaning
0	IO_LVDS(0) - Input from Memory Board
1	IO_LVDS(1) - Input from Memory Board
2	IO_LVDS(2) - Input from Memory Board
3	IO_LVDS(3) - Input from Memory Board
4	IO_LVDS(4) - Input from Memory Board
5	IO_LVDS(5) - Input from Memory Board
6	IO_LVDS(6) - Input from Memory Board
7	IO_LVDS(7) - Input from Memory Board
15..8	<i>Not Used</i>

5.5 Memory Board “B”

Memory board “B” should connect to the connector labeled SAMTEC “B” on the PMC.

5.5.1 Memory Board “B” Control - Outputs

The MemBrdCtlOUT register contains all control signals that are driven to the Memory Board.

Register 0x0100 (Read/Write) – MemBrdCtlOUT - B	
Bit #	Meaning
0	TR_LVDS
1	CE_LVDS
2	CLE_LVDS
3	ALE_LVDS
4	RE_LVDS
5	WE_LVDS
6	WP_LVDS
15..7	<i>Not Used</i>

5.5.2 Memory Board “B” Control - Inputs

The MemBrdCtrlIN register contains the one control signal that is driven from the Memory Board to the PMC.

Register 0x0104 (Read Only) – MemBrdCtrlIN - B	
Bit #	Meaning
0	RB_LVDS
15..1	<i>Not Used</i>

5.5.3 Memory Board “B” IO Data - OUT

This register contains the eight bit data that is driven from the PMC to the Memory Board.

Register 0x0108 (Read/Write) – IO_OUT_LVDS - B	
Bit #	Meaning
0	IO_LVDS(0) - Output to Memory Board
1	IO_LVDS(1) - Output to Memory Board
2	IO_LVDS(2) - Output to Memory Board
3	IO_LVDS(3) - Output to Memory Board
4	IO_LVDS(4) - Output to Memory Board
5	IO_LVDS(5) - Output to Memory Board
6	IO_LVDS(6) - Output to Memory Board
7	IO_LVDS(7) - Output to Memory Board
15..8	<i>Not Used</i>

5.5.4 Memory Board “B” IO Data - IN

This register contains the eight bit data that is driven from the Memory Board to the PMC.

Register 0x010C (Read Only) – IO_IN_LVDS - B	
Bit #	Meaning
0	IO_LVDS(0) - Input from Memory Board
1	IO_LVDS(1) - Input from Memory Board
2	IO_LVDS(2) - Input from Memory Board
3	IO_LVDS(3) - Input from Memory Board
4	IO_LVDS(4) - Input from Memory Board
5	IO_LVDS(5) - Input from Memory Board
6	IO_LVDS(6) - Input from Memory Board
7	IO_LVDS(7) - Input from Memory Board
15..8	<i>Not Used</i>

5.6 Memory Board “C”

Memory board “C” should connect to the connector labeled SAMTEC “C” on the PMC.

5.6.1 Memory Board “C” Control - Outputs

The MemBrdCtlOUT register contains all control signals that are driven to the Memory Board.

Register 0x0110 (Read/Write) – MemBrdCtlOUT - C	
Bit #	Meaning
0	TR_LVDS
1	CE_LVDS
2	CLE_LVDS
3	ALE_LVDS
4	RE_LVDS
5	WE_LVDS
6	WP_LVDS
15..7	<i>Not Used</i>

5.6.2 Memory Board “C” Control - Inputs

The MemBrdCtrlIN register contains the one control signal that is driven from the Memory Board to the PMC.

Register 0x0114 (Read Only) – MemBrdCtrlIN - C	
Bit #	Meaning
0	RB_LVDS
15..1	<i>Not Used</i>

5.6.3 Memory Board “C” IO Data - OUT

This register contains the eight bit data that is driven from the PMC to the Memory Board.

Register 0x0118 (Read/Write) – IO_OUT_LVDS - C	
Bit #	Meaning
0	IO_LVDS(0) - Output to Memory Board
1	IO_LVDS(1) - Output to Memory Board
2	IO_LVDS(2) - Output to Memory Board
3	IO_LVDS(3) - Output to Memory Board
4	IO_LVDS(4) - Output to Memory Board
5	IO_LVDS(5) - Output to Memory Board
6	IO_LVDS(6) - Output to Memory Board
7	IO_LVDS(7) - Output to Memory Board
15..8	<i>Not Used</i>

5.6.4 Memory Board “C” IO Data - IN

This register contains the eight bit data that is driven from the Memory Board to the PMC.

Register 0x011C (Read Only) – IO_IN_LVDS - C	
Bit #	Meaning
0	IO_LVDS(0) - Input from Memory Board
1	IO_LVDS(1) - Input from Memory Board
2	IO_LVDS(2) - Input from Memory Board
3	IO_LVDS(3) - Input from Memory Board
4	IO_LVDS(4) - Input from Memory Board
5	IO_LVDS(5) - Input from Memory Board
6	IO_LVDS(6) - Input from Memory Board
7	IO_LVDS(7) - Input from Memory Board
15..8	<i>Not Used</i>

5.7 Memory Board “D”

Memory board “D” should connect to the connector labeled SAMTEC “D” on the PMC.

5.7.1 Memory Board “D” Control - Outputs

The MemBrdCtlOUT register contains all control signals that are driven to the Memory Board.

Register 0x0120 (Read/Write) – MemBrdCtlOUT - D	
Bit #	Meaning
0	TR_LVDS
1	CE_LVDS
2	CLE_LVDS
3	ALE_LVDS
4	RE_LVDS
5	WE_LVDS
6	WP_LVDS
15..7	<i>Not Used</i>

5.7.2 Memory Board “D” Control - Inputs

The MemBrdCtrlIN register contains the one control signal that is driven from the Memory Board to the PMC.

Register 0x0124 (Read Only) – MemBrdCtrlIN - D	
Bit #	Meaning
0	RB_LVDS
15..1	<i>Not Used</i>

5.7.3 Memory Board “D” IO Data - OUT

This register contains the eight bit data that is driven from the PMC to the Memory Board.

Register 0x0128 (Read/Write) – IO_OUT_LVDS - D	
Bit #	Meaning
0	IO_LVDS(0) - Output to Memory Board
1	IO_LVDS(1) - Output to Memory Board
2	IO_LVDS(2) - Output to Memory Board
3	IO_LVDS(3) - Output to Memory Board
4	IO_LVDS(4) - Output to Memory Board
5	IO_LVDS(5) - Output to Memory Board
6	IO_LVDS(6) - Output to Memory Board
7	IO_LVDS(7) - Output to Memory Board
15..8	<i>Not Used</i>

5.7.4 Memory Board “D” IO Data - IN

This register contains the eight bit data that is driven from the Memory Board to the PMC.

Register 0x012C (Read Only) – IO_IN_LVDS - D	
Bit #	Meaning
0	IO_LVDS(0) - Input from Memory Board
1	IO_LVDS(1) - Input from Memory Board
2	IO_LVDS(2) - Input from Memory Board
3	IO_LVDS(3) - Input from Memory Board
4	IO_LVDS(4) - Input from Memory Board
5	IO_LVDS(5) - Input from Memory Board
6	IO_LVDS(6) - Input from Memory Board
7	IO_LVDS(7) - Input from Memory Board
15..8	<i>Not Used</i>

6 General Comments

As a sanity check, try reading Register 0x0000 and 0x0004. These are hardwired read-only register that should read 0x0011 and 0x0100, respectively. If not, there is a problem with the PMC/PTA interface. Try the reset button on the PMC or power down and re-connect the PMC to the PTA card.