SNAP
PMC Firmware for controlling Flash Memory RAD Test Board
PAC top level. JN2 Outputs.

Title: Bradley Hall - SNAP Memory Test
Name: October 14, 2003
When LVDS_TRX_DE is '1', then the LVDS Transceiver on the Memory Board is driving signals to the PMC.

The equivalent equation is:

$$LVDS_{TRX\_DE} = TR_{LVDS}$$

LVDS_TRX_DE is a copy of the Transceiver_T/R signal on the SNAP Memory Board schematic.

When LVDS_TRX_DE = '1', the Memory Board is driving LVDS_IO signals to the PMC.

Delay is to account for bus turnaround time and avoid bus contention.

Delay is determined by DelayCount(15:0) value * DelayCntrCLK period

$$~5.24\text{m sec}$$

IO_Direction

When IO_Direction = '1', PMC is receiving.

When IO_Direction = '0', PMC is driving.

Desired waveforms.
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\[ \text{LVDS_TRX_DE} = \text{TR_LVDS} \]

When LVDS_TRX_DE = '1', the Memory Board is driving LVDS IO signals to the PMC.

When IO_Direction = '1', PMC is receiving. When IO_Direction = '0', PMC is driving.

Delay is to account for bus turnaround time and avoid bus contention. Delay is determined by DelayCount(15:0) value * DelayCntrCLK period ~5.24m sec

This is emulating what is on the memory board.

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Delay, C

\[ \approx 5.24 \text{m sec} \]

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**C**
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