Firmware Type = SNAP Memory Board
Firmware Rev = 1.3

SNAP
PMC Firmware for controlling Flash Memory RAD Test Board
PMC top level. Registers for B, C, and D.

Title: PMC top level. Registers for B, C, and D.
Date: September 10, 2003
Name: Bradley Hall - SNAP Memory Test

Sheet 2 of 8
XTAL_CLK is a 50MHz Oscillator

DelayCntrCLK is a 12.5MHz Clock

IO_OUT_LVDS_A(b)
IO_IN_LVDS_A(b)
GND

IO_OUT_LVDS_B(b)
IO_IN_LVDS_B(b)
GND

IO_OUT_LVDS_C(b)
IO_IN_LVDS_C(b)
GND

IO_OUT_LVDS_D(b)
IO_IN_LVDS_D(b)
GND

IO_IN_LVDS_A(0)
IO_DIR_LVDS_A(0)
GND

IO_IN_LVDS_B(0)
IO_DIR_LVDS_B(0)
GND

IO_IN_LVDS_C(0)
IO_DIR_LVDS_C(0)
GND

IO_IN_LVDS_D(0)
IO_DIR_LVDS_D(0)
GND

CB2CE
DelayCntrCLK

Title: PMC top level. Periphery I/O and LEDs
Name: Bradley Hall - SNAP Memory Test
Date: September 10, 2003
When LVDS_TRX_DE is '1', then the LVDS Transceiver on the Memory Board is driving signals to the PMC.

The equivalent equation is:

\[ \text{LVDS_TRX_DE} = \text{TR_LVDS} \]
When LVDS_TRX_DE is '1', then the LVDS Transceiver on the Memory Board is driving signals to the PMC.

The equivalent equation is:

$$LVDS_{TRX\_DE} = TR_{LVDS}$$

LVDS_TRX_DE is a copy of the Transceiver_T/R signal on the SNAP Memory Board schematic.

This is emulating what is on the memory board.

Desired waveforms.
When LVDS_TRX_DE is '1', then the LVDS Transceiver on the Memory Board is driving signals to the PMC.

The equivalent equation is:

\[ \text{LVDS_TRX_DE} = \text{TR_LVDS} \]

When LVDS_TRX_DE is a copy of the Transceiver_T/T signal on the SNAP Memory Board schematic.

When LVDS_TRX_DE = '1', the Memory Board is driving LVDS_IO signals to the PMC.

Delay is to account for bus turnaround time and avoid bus contention.

Delay is determined by DelayCount(15:0) value * DelayCnt_CLK period

-5.24m sec

Desired waveforms.
When LVDS_TRX_DE is '1', then the LVDS Transceiver on the Memory Board is driving signals to the PMC.

The equivalent equation is:

\[
LVDS_TRX_DE = TR_LVDS
\]

This is emulating what is on the memory board.

Desired waveforms.

Delay is to account for bus turnaround time and avoid bus contention. Delay is determined by DelayCount(15:0) value * DelayCntCLK period ~5.24m sec