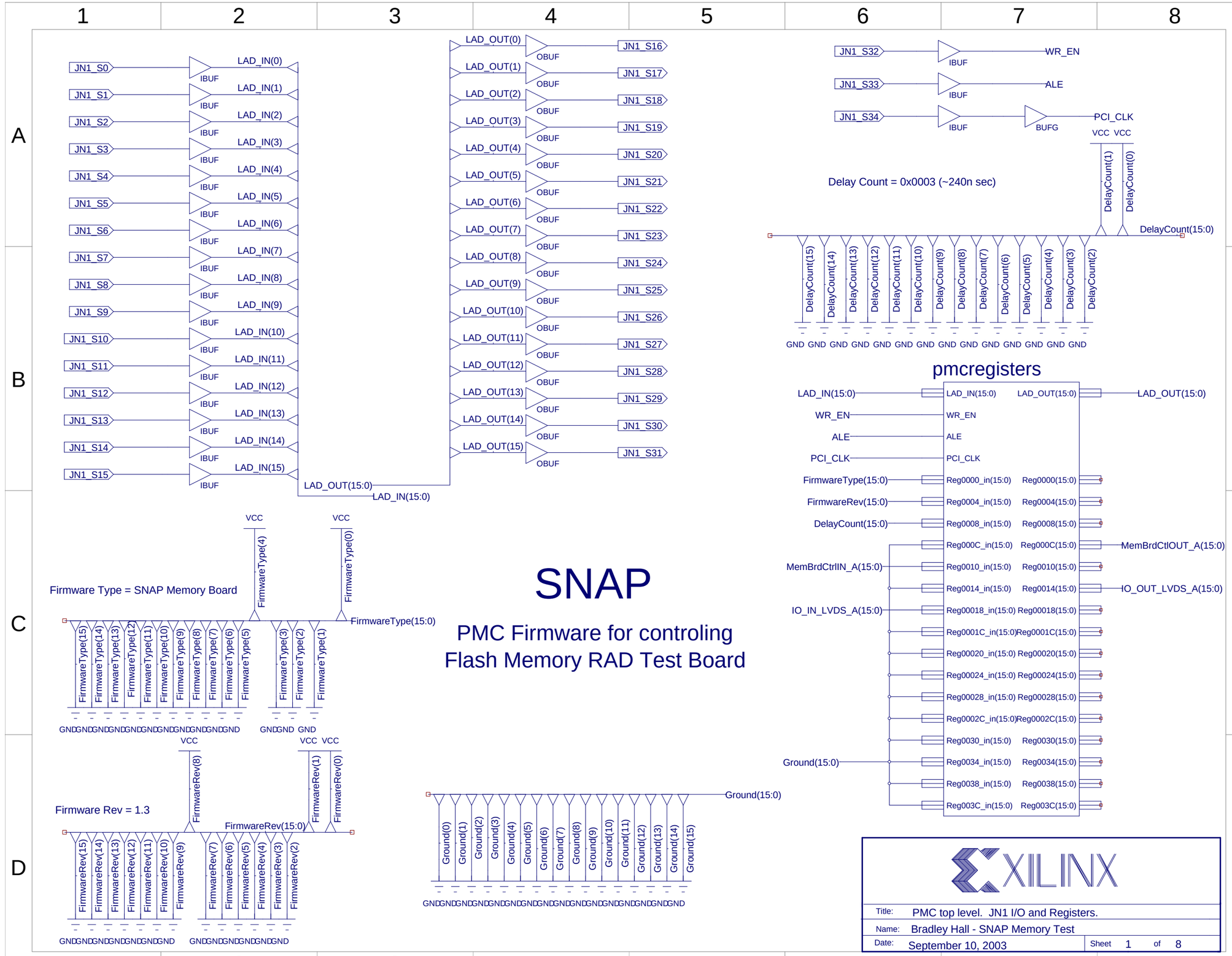
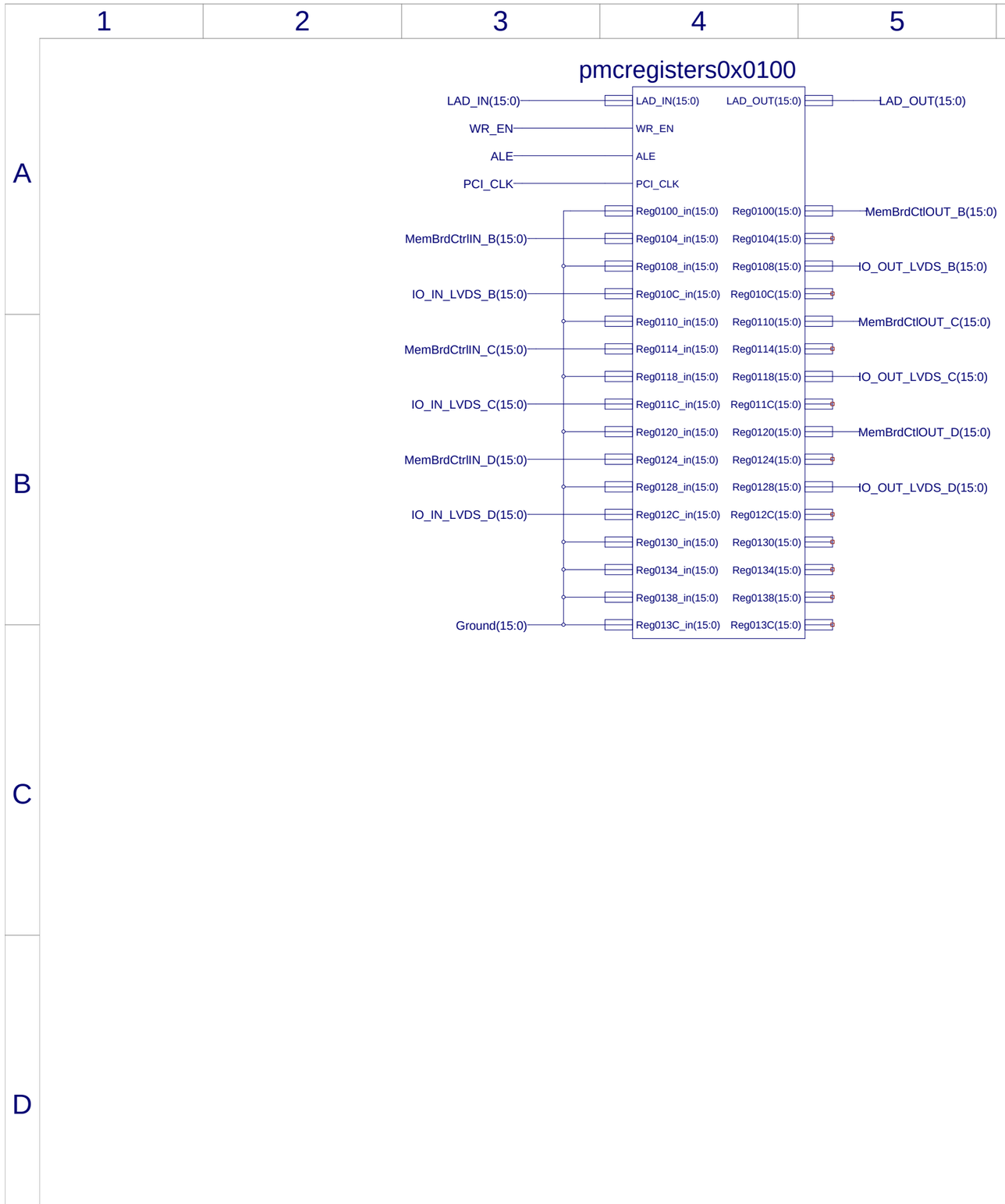
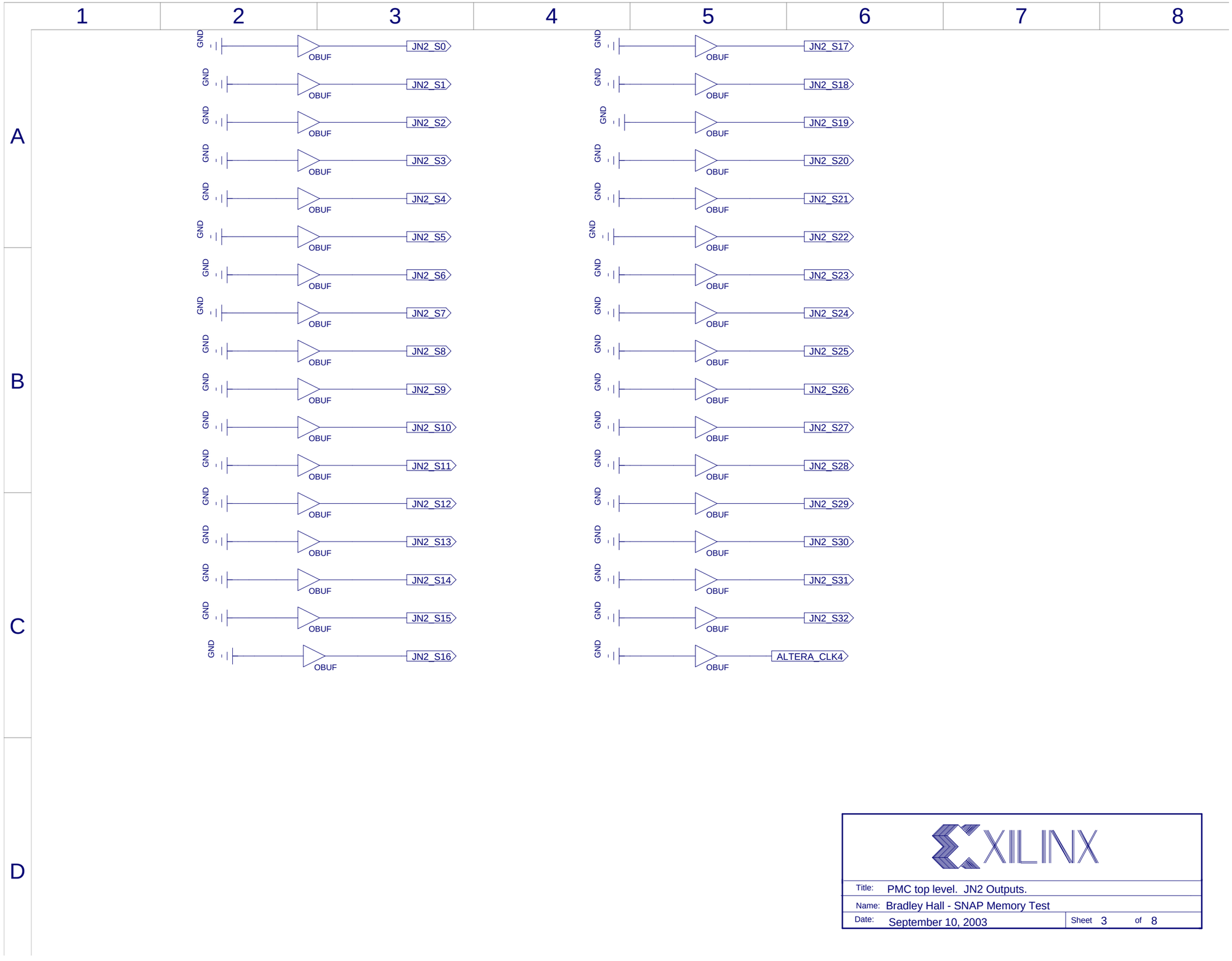
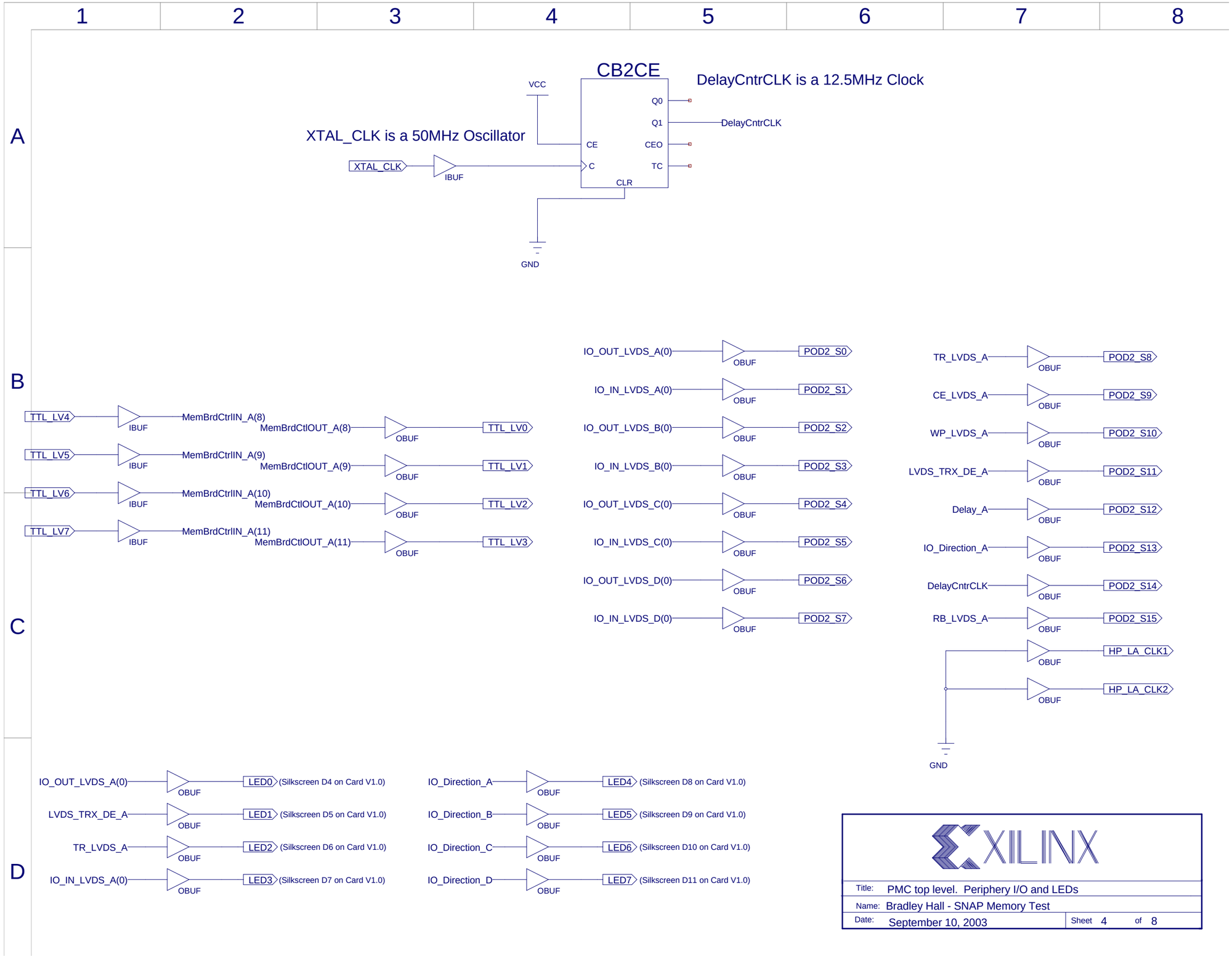

SNAP
PMC Firmware for controling
Flash Memory RAD Test Board
JN1_S0 JN1_S1 JN1_S2 JN1_S3 JN1_S4 JN1_S5 JN1_S6 JN1_S7 JN1_S8 JN1_S9 JN1_S10 JN1_S11 JN1_S12 JN1_S13 JN1_S14 JN1_S15
IBUF
LAD_IN(0) LAD_IN(1) LAD_IN(2) LAD_IN(3) LAD_IN(4) LAD_IN(5) LAD_IN(6) LAD_IN(7) LAD_IN(8) LAD_IN(9) LAD_IN(10) LAD_IN(11) LAD_IN(12) LAD_IN(13) LAD_IN(14) LAD_IN(15)
LAD_OUT(15:0)
LAD_IN(15:0)
LAD_OUT(0) LAD_OUT(1) LAD_OUT(2) LAD_OUT(3) LAD_OUT(4) LAD_OUT(5) LAD_OUT(6) LAD_OUT(7) LAD_OUT(8) LAD_OUT(9) LAD_OUT(10) LAD_OUT(11) LAD_OUT(12) LAD_OUT(13) LAD_OUT(14) LAD_OUT(15)
OBUF
JN1_S16 JN1_S17 JN1_S18 JN1_S19 JN1_S20 JN1_S21 JN1_S22 JN1_S23 JN1_S24 JN1_S25 JN1_S26 JN1_S27 JN1_S28 JN1_S29 JN1_S30 JN1_S31
JN1_S32 JN1_S33 JN1_S34
WR_EN
ALE
PCI_CLK
BUFG
VCC
Delay Count = 0x0003 (~240n sec)
DelayCount(1) DelayCount(0)
DelayCount(15:0)
DelayCount(15) DelayCount(14) DelayCount(13) DelayCount(12) DelayCount(11) DelayCount(10) DelayCount(9) DelayCount(8) DelayCount(7) DelayCount(6) DelayCount(5) DelayCount(4) DelayCount(3) DelayCount(2)
GND
pmcregisters
LAD_IN(15:0)
LAD_OUT(15:0)
WR_EN
ALE
PCI_CLK
FirmwareType(15:0)
FirmwareRev(15:0)
DelayCount(15:0)
MemBrdCtrlIN_A(15:0)
IO_IN_LVDS_A(15:0)
Ground(15:0)
Reg0000_in(15:0) Reg0000(15:0)
Reg0004_in(15:0) Reg0004(15:0)
Reg0008_in(15:0) Reg0008(15:0)
Reg000C_in(15:0) Reg000C(15:0)
Reg0010_in(15:0) Reg0010(15:0)
Reg0014_in(15:0) Reg0014(15:0)
Reg00018_in(15:0) Reg00018(15:0)
Reg0001C_in(15:0) Reg0001C(15:0)
Reg00020_in(15:0) Reg00020(15:0)
Reg00024_in(15:0) Reg00024(15:0)
Reg00028_in(15:0) Reg00028(15:0)
Reg0002C_in(15:0) Reg0002C(15:0)
Reg0030_in(15:0) Reg0030(15:0)
Reg0034_in(15:0) Reg0034(15:0)
Reg0038_in(15:0) Reg0038(15:0)
Reg003C_in(15:0) Reg003C(15:0)
MemBrdCtlOUT_A(15:0)
IO_OUT_LVDS_A(15:0)
Firmware Type = SNAP Memory Board
FirmwareType(4) FirmwareType(0)
FirmwareType(15:0)
FirmwareType(15) FirmwareType(14) FirmwareType(13) FirmwareType(12) FirmwareType(11) FirmwareType(10) FirmwareType(9) FirmwareType(8) FirmwareType(7) FirmwareType(6) FirmwareType(5) FirmwareType(3) FirmwareType(2) FirmwareType(1)
Firmware Rev = 1.3
FirmwareRev(8) FirmwareRev(1) FirmwareRev(0)
FirmwareRev(15:0)
FirmwareRev(15) FirmwareRev(14) FirmwareRev(13) FirmwareRev(12) FirmwareRev(11) FirmwareRev(10) FirmwareRev(9) FirmwareRev(7) FirmwareRev(6) FirmwareRev(5) FirmwareRev(4) FirmwareRev(3) FirmwareRev(2)
Ground(15:0)
Ground(0) Ground(1) Ground(2) Ground(3) Ground(4) Ground(5) Ground(6) Ground(7) Ground(8) Ground(9) Ground(10) Ground(11) Ground(12) Ground(13) Ground(14) Ground(15)
XILINX
Title: PMC top level. JN1 I/O and Registers.
Name: Bradley Hall - SNAP Memory Test
Date: September 10, 2003
Sheet 1 of 8

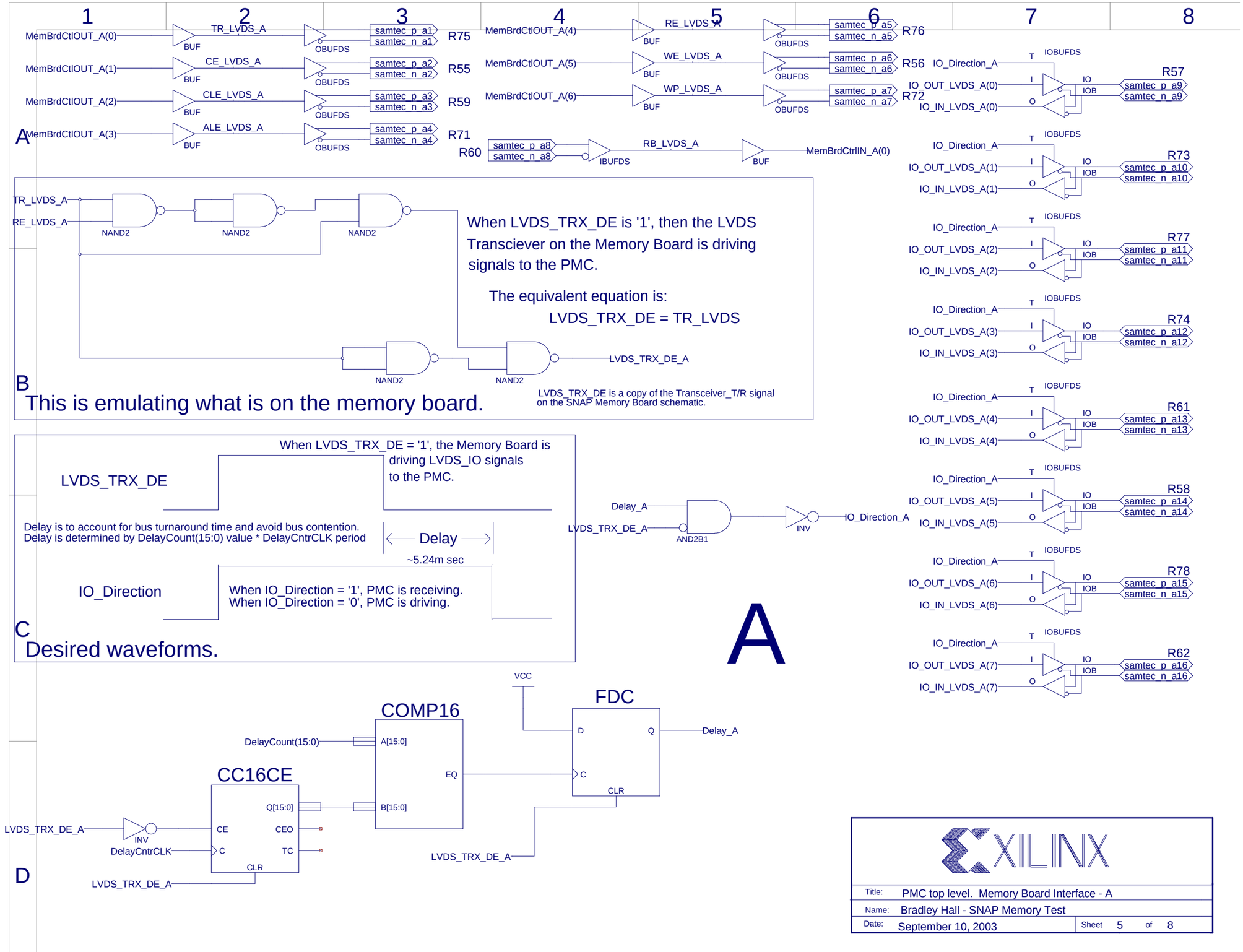


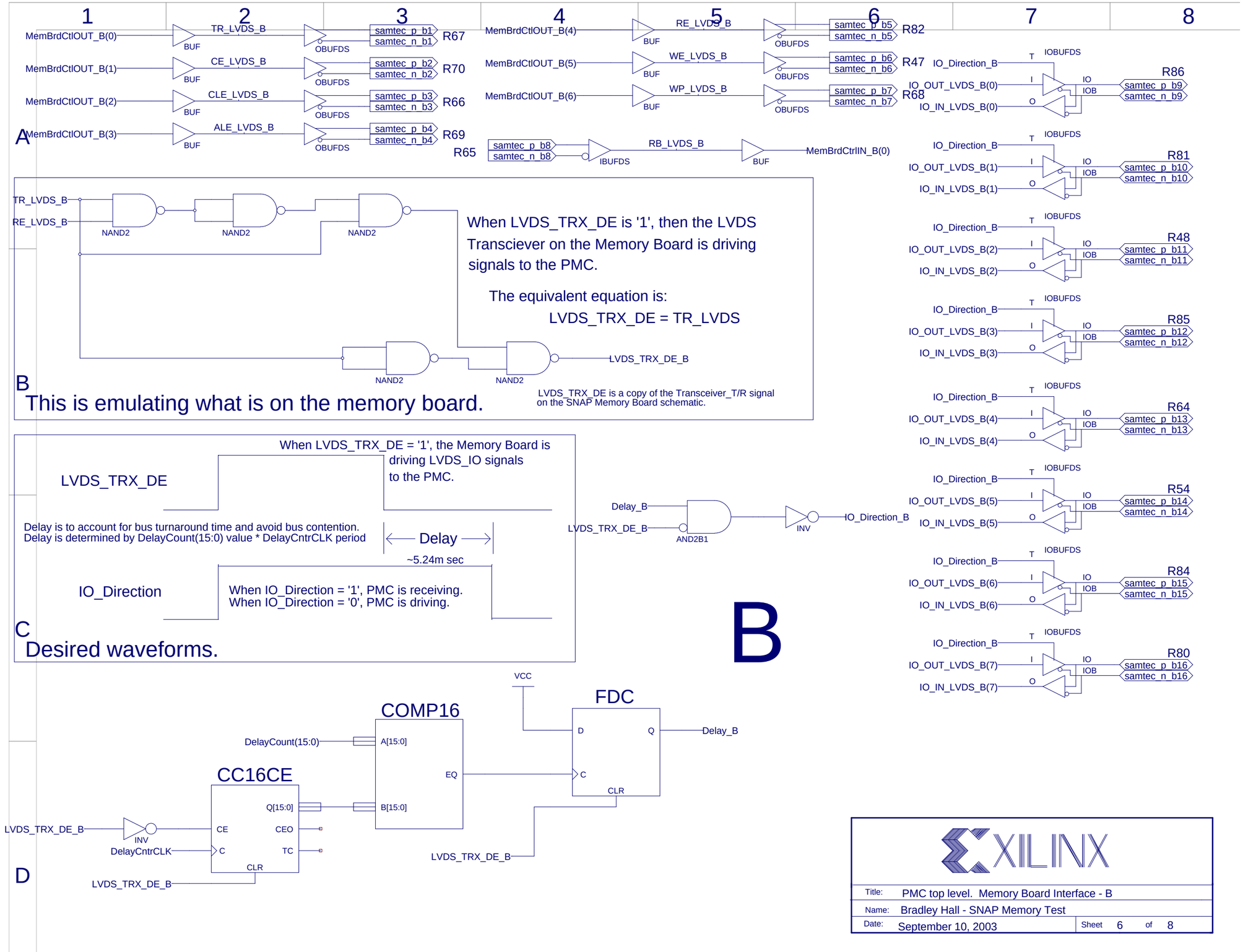
XILINX

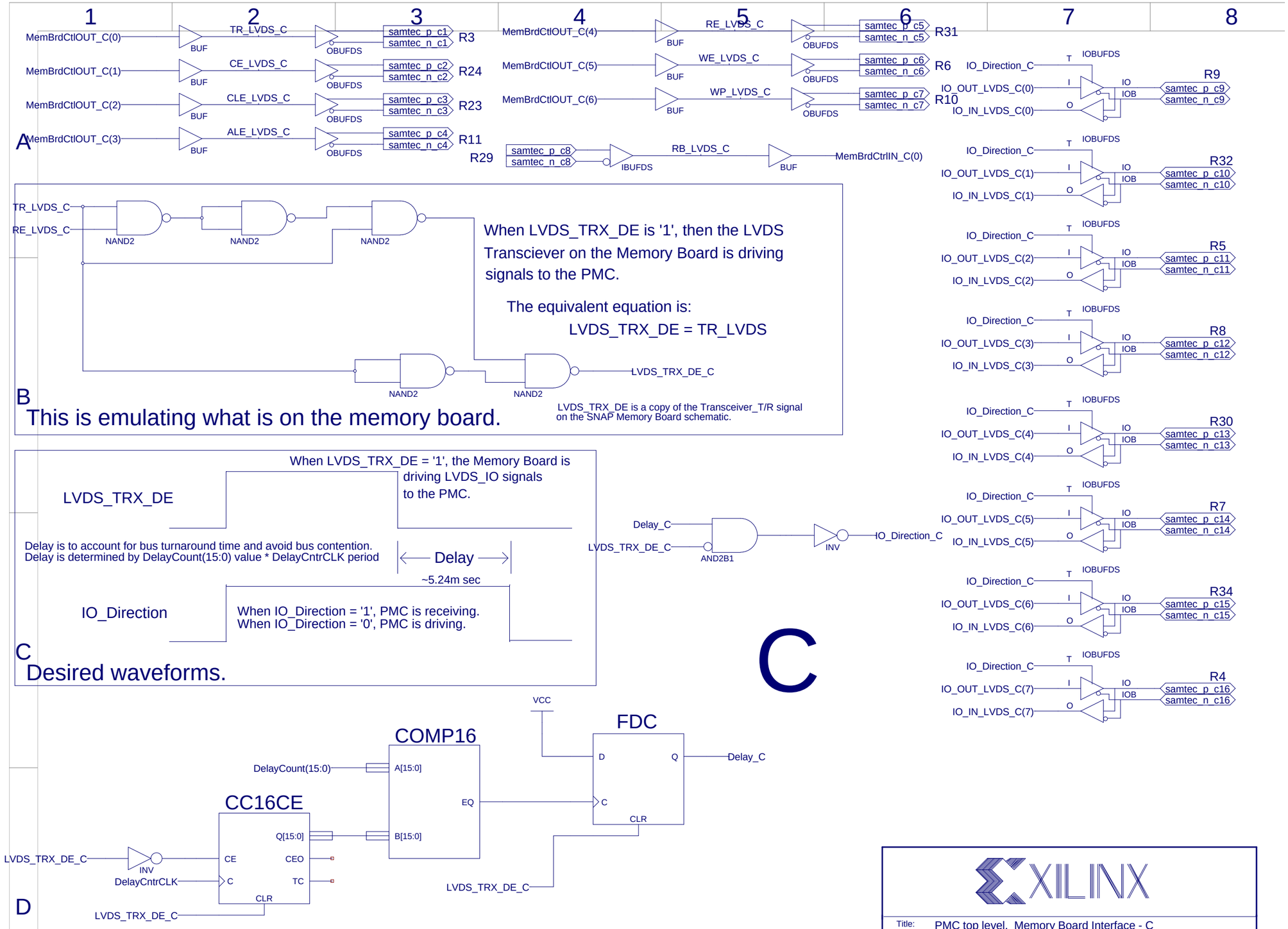
Title:	PMC top level. Registers for B, C, and D.
Name:	Bradley Hall - SNAP Memory Test
Date:	September 10, 2003
Sheet	2 of 8

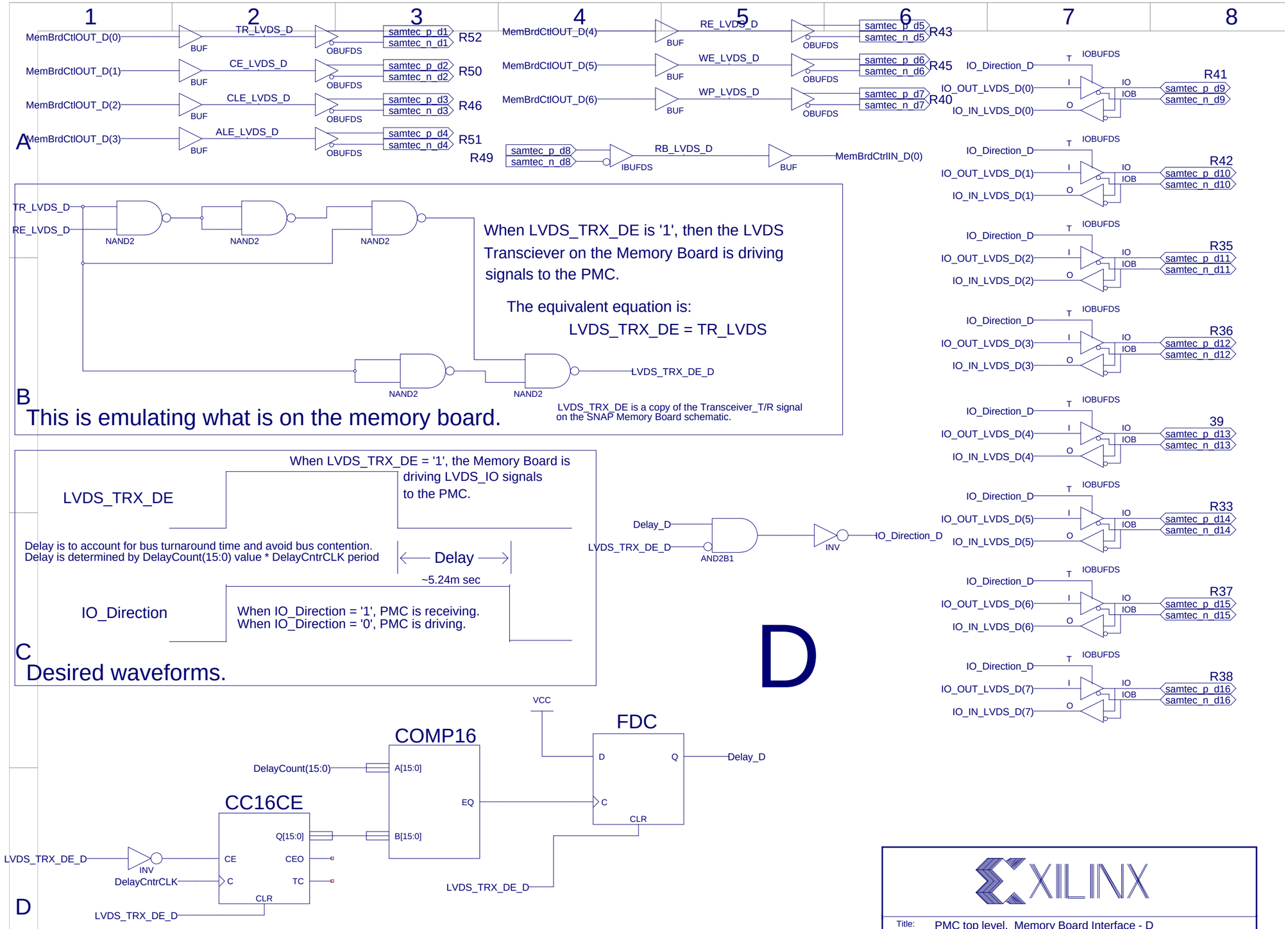

1
2
3
4
5
6
7
8
A
B
C
D
GND
OBUF
JN2_S0
JN2_S1
JN2_S2
JN2_S3
JN2_S4
JN2_S5
JN2_S6
JN2_S7
JN2_S8
JN2_S9
JN2_S10
JN2_S11
JN2_S12
JN2_S13
JN2_S14
JN2_S15
JN2_S16
JN2_S17
JN2_S18
JN2_S19
JN2_S20
JN2_S21
JN2_S22
JN2_S23
JN2_S24
JN2_S25
JN2_S26
JN2_S27
JN2_S28
JN2_S29
JN2_S30
JN2_S31
JN2_S32
ALTERA_CLK4
XILINX
Title: PMC top level. JN2 Outputs.
Name: Bradley Hall - SNAP Memory Test
Date: September 10, 2003
Sheet 3 of 8


CB2CE
DelayCntrCLK is a 12.5MHz Clock
VCC
Q0
Q1
DelayCntrCLK
XTAL_CLK is a 50MHz Oscillator
CE
CEO
XTAL_CLK
IBUF
C
TC
CLR
GND
IO_OUT_LVDS_A(0)
OBUF
POD2_S0
IO_IN_LVDS_A(0)
POD2_S1
IO_OUT_LVDS_B(0)
POD2_S2
IO_IN_LVDS_B(0)
POD2_S3
IO_OUT_LVDS_C(0)
POD2_S4
IO_IN_LVDS_C(0)
POD2_S5
IO_OUT_LVDS_D(0)
POD2_S6
IO_IN_LVDS_D(0)
POD2_S7
TR_LVDS_A
POD2_S8
CE_LVDS_A
POD2_S9
WP_LVDS_A
POD2_S10
LVDS_TRX_DE_A
POD2_S11
Delay_A
POD2_S12
IO_Direction_A
POD2_S13
DelayCntrCLK
POD2_S14
RB_LVDS_A
POD2_S15
HP_LA_CLK1
HP_LA_CLK2
GND
TTL_LV4
MemBrdCtrlIN_A(8)
MemBrdCtlOUT_A(8)
TTL_LV0
TTL_LV5
MemBrdCtrlIN_A(9)
MemBrdCtlOUT_A(9)
TTL_LV1
TTL_LV6
MemBrdCtrlIN_A(10)
MemBrdCtlOUT_A(10)
TTL_LV2
TTL_LV7
MemBrdCtrlIN_A(11)
MemBrdCtlOUT_A(11)
TTL_LV3
IO_OUT_LVDS_A(0)
LED0 (Silkscreen D4 on Card V1.0)
LVDS_TRX_DE_A
LED1 (Silkscreen D5 on Card V1.0)
TR_LVDS_A
LED2 (Silkscreen D6 on Card V1.0)
IO_IN_LVDS_A(0)
LED3 (Silkscreen D7 on Card V1.0)
IO_Direction_A
LED4 (Silkscreen D8 on Card V1.0)
IO_Direction_B
LED5 (Silkscreen D9 on Card V1.0)
IO_Direction_C
LED6 (Silkscreen D10 on Card V1.0)
IO_Direction_D
LED7 (Silkscreen D11 on Card V1.0)
XILINX
Title: PMC top level. Periphery I/O and LEDs
Name: Bradley Hall - SNAP Memory Test
Date: September 10, 2003
Sheet 4 of 8


1
2
3
4
5
6
7
8
MemBrdCtlOUT_A(0)
TR_LVDS_A
BUF
OBUFDS
samtec_p_a1
samtec_n_a1
R75
MemBrdCtlOUT_A(1)
CE_LVDS_A
samtec_p_a2
samtec_n_a2
R55
MemBrdCtlOUT_A(2)
CLE_LVDS_A
samtec_p_a3
samtec_n_a3
R59
MemBrdCtlOUT_A(3)
ALE_LVDS_A
samtec_p_a4
samtec_n_a4
R71
A
MemBrdCtlOUT_A(4)
RE_LVDS_A
samtec_p_a5
samtec_n_a5
R76
MemBrdCtlOUT_A(5)
WE_LVDS_A
samtec_p_a6
samtec_n_a6
R56
MemBrdCtlOUT_A(6)
WP_LVDS_A
samtec_p_a7
samtec_n_a7
R72
samtec_p_a8
samtec_n_a8
R60
IBUFDS
RB_LVDS_A
MemBrdCtrlIN_A(0)
IO_Direction_A
IO_OUT_LVDS_A(0)
IO_IN_LVDS_A(0)
IO_OUT_LVDS_A(1)
IO_IN_LVDS_A(1)
IO_OUT_LVDS_A(2)
IO_IN_LVDS_A(2)
IO_OUT_LVDS_A(3)
IO_IN_LVDS_A(3)
IO_OUT_LVDS_A(4)
IO_IN_LVDS_A(4)
IO_OUT_LVDS_A(5)
IO_IN_LVDS_A(5)
IO_OUT_LVDS_A(6)
IO_IN_LVDS_A(6)
IO_OUT_LVDS_A(7)
IO_IN_LVDS_A(7)
T
I
O
IO
IOB
IOBUFDS
R57
samtec_p_a9
samtec_n_a9
R73
samtec_p_a10
samtec_n_a10
R77
samtec_p_a11
samtec_n_a11
R74
samtec_p_a12
samtec_n_a12
R61
samtec_p_a13
samtec_n_a13
R58
samtec_p_a14
samtec_n_a14
R78
samtec_p_a15
samtec_n_a15
R62
samtec_p_a16
samtec_n_a16
TR_LVDS_A
RE_LVDS_A
NAND2
When LVDS_TRX_DE is '1', then the LVDS Transciever on the Memory Board is driving signals to the PMC.
The equivalent equation is:
LVDS_TRX_DE = TR_LVDS
LVDS_TRX_DE_A
B
This is emulating what is on the memory board.
LVDS_TRX_DE is a copy of the Transceiver_T/R signal on the SNAP Memory Board schematic.
Delay_A
LVDS_TRX_DE_A
AND2B1
INV
IO_Direction_A
A
When LVDS_TRX_DE = '1', the Memory Board is driving LVDS_IO signals to the PMC.
LVDS_TRX_DE
Delay is to account for bus turnaround time and avoid bus contention.
Delay is determined by DelayCount(15:0) value * DelayCntrCLK period
Delay
~5.24m sec
IO_Direction
When IO_Direction = '1', PMC is receiving.
When IO_Direction = '0', PMC is driving.
C
Desired waveforms.
VCC
FDC
D
Q
C
CLR
Delay_A
COMP16
DelayCount(15:0)
A[15:0]
EQ
B[15:0]
CC16CE
LVDS_TRX_DE_A
INV
CE
C
DelayCntrCLK
Q[15:0]
CEO
TC
CLR
LVDS_TRX_DE_A
D
XILINX
Title: PMC top level. Memory Board Interface - A
Name: Bradley Hall - SNAP Memory Test
Date: September 10, 2003
Sheet 5 of 8


1
2
3
4
5
6
7
8
MemBrdCtlOUT_B(0)
MemBrdCtlOUT_B(1)
MemBrdCtlOUT_B(2)
MemBrdCtlOUT_B(3)
BUF
TR_LVDS_B
CE_LVDS_B
CLE_LVDS_B
ALE_LVDS_B
OBUFDS
samtec_p_b1
samtec_n_b1
samtec_p_b2
samtec_n_b2
samtec_p_b3
samtec_n_b3
samtec_p_b4
samtec_n_b4
R67
R70
R66
R69
A
MemBrdCtlOUT_B(4)
MemBrdCtlOUT_B(5)
MemBrdCtlOUT_B(6)
RE_LVDS_B
WE_LVDS_B
WP_LVDS_B
samtec_p_b5
samtec_n_b5
samtec_p_b6
samtec_n_b6
samtec_p_b7
samtec_n_b7
R82
R47
R68
samtec_p_b8
samtec_n_b8
R65
IBUFDS
RB_LVDS_B
MemBrdCtrlIN_B(0)
IO_Direction_B
IO_OUT_LVDS_B(0)
IO_IN_LVDS_B(0)
IO_OUT_LVDS_B(1)
IO_IN_LVDS_B(1)
IO_OUT_LVDS_B(2)
IO_IN_LVDS_B(2)
IO_OUT_LVDS_B(3)
IO_IN_LVDS_B(3)
IO_OUT_LVDS_B(4)
IO_IN_LVDS_B(4)
IO_OUT_LVDS_B(5)
IO_IN_LVDS_B(5)
IO_OUT_LVDS_B(6)
IO_IN_LVDS_B(6)
IO_OUT_LVDS_B(7)
IO_IN_LVDS_B(7)
IOBUFDS
T
I
O
IO
IOB
R86
samtec_p_b9
samtec_n_b9
R81
samtec_p_b10
samtec_n_b10
R48
samtec_p_b11
samtec_n_b11
R85
samtec_p_b12
samtec_n_b12
R64
samtec_p_b13
samtec_n_b13
R54
samtec_p_b14
samtec_n_b14
R84
samtec_p_b15
samtec_n_b15
R80
samtec_p_b16
samtec_n_b16
B
TR_LVDS_B
RE_LVDS_B
NAND2
When LVDS_TRX_DE is '1', then the LVDS Transciever on the Memory Board is driving signals to the PMC.
The equivalent equation is:
LVDS_TRX_DE = TR_LVDS
LVDS_TRX_DE_B
LVDS_TRX_DE is a copy of the Transceiver_T/R signal on the SNAP Memory Board schematic.
This is emulating what is on the memory board.
When LVDS_TRX_DE = '1', the Memory Board is driving LVDS_IO signals to the PMC.
LVDS_TRX_DE
Delay is to account for bus turnaround time and avoid bus contention.
Delay is determined by DelayCount(15:0) value * DelayCntrCLK period
Delay
~5.24m sec
IO_Direction
When IO_Direction = '1', PMC is receiving.
When IO_Direction = '0', PMC is driving.
C
Desired waveforms.
Delay_B
LVDS_TRX_DE_B
AND2B1
INV
IO_Direction_B
VCC
COMP16
DelayCount(15:0)
A[15:0]
EQ
B[15:0]
FDC
D
Q
C
CLR
Delay_B
CC16CE
LVDS_TRX_DE_B
INV
DelayCntrCLK
CE
C
Q[15:0]
CEO
TC
CLR
LVDS_TRX_DE_B
D
XILINX
Title: PMC top level. Memory Board Interface - B
Name: Bradley Hall - SNAP Memory Test
Date: September 10, 2003
Sheet 6 of 8


1
2
3
4
5
6
7
8
MemBrdCtlOUT_C(0)
MemBrdCtlOUT_C(1)
MemBrdCtlOUT_C(2)
MemBrdCtlOUT_C(3)
MemBrdCtlOUT_C(4)
MemBrdCtlOUT_C(5)
MemBrdCtlOUT_C(6)
BUF
TR_LVDS_C
CE_LVDS_C
CLE_LVDS_C
ALE_LVDS_C
RE_LVDS_C
WE_LVDS_C
WP_LVDS_C
OBUFDS
samtec_p_c1
samtec_n_c1
samtec_p_c2
samtec_n_c2
samtec_p_c3
samtec_n_c3
samtec_p_c4
samtec_n_c4
samtec_p_c5
samtec_n_c5
samtec_p_c6
samtec_n_c6
samtec_p_c7
samtec_n_c7
R3
R24
R23
R11
R31
R6
R10
A
samtec_p_c8
samtec_n_c8
IBUFDS
RB_LVDS_C
MemBrdCtrlIN_C(0)
R29
TR_LVDS_C
RE_LVDS_C
NAND2
LVDS_TRX_DE_C
When LVDS_TRX_DE is '1', then the LVDS Transciever on the Memory Board is driving signals to the PMC.
The equivalent equation is:
LVDS_TRX_DE = TR_LVDS
LVDS_TRX_DE is a copy of the Transceiver_T/R signal on the SNAP Memory Board schematic.
B
This is emulating what is on the memory board.
When LVDS_TRX_DE = '1', the Memory Board is driving LVDS_IO signals to the PMC.
LVDS_TRX_DE
Delay is to account for bus turnaround time and avoid bus contention.
Delay is determined by DelayCount(15:0) value * DelayCntrCLK period
Delay
~5.24m sec
IO_Direction
When IO_Direction = '1', PMC is receiving.
When IO_Direction = '0', PMC is driving.
C
Desired waveforms.
Delay_C
LVDS_TRX_DE_C
AND2B1
INV
IO_Direction_C
IOBUFDS
T
I
O
IO
IOB
IO_OUT_LVDS_C(0)
IO_IN_LVDS_C(0)
IO_OUT_LVDS_C(1)
IO_IN_LVDS_C(1)
IO_OUT_LVDS_C(2)
IO_IN_LVDS_C(2)
IO_OUT_LVDS_C(3)
IO_IN_LVDS_C(3)
IO_OUT_LVDS_C(4)
IO_IN_LVDS_C(4)
IO_OUT_LVDS_C(5)
IO_IN_LVDS_C(5)
IO_OUT_LVDS_C(6)
IO_IN_LVDS_C(6)
IO_OUT_LVDS_C(7)
IO_IN_LVDS_C(7)
R9
R32
R5
R8
R30
R7
R34
R4
samtec_p_c9
samtec_n_c9
samtec_p_c10
samtec_n_c10
samtec_p_c11
samtec_n_c11
samtec_p_c12
samtec_n_c12
samtec_p_c13
samtec_n_c13
samtec_p_c14
samtec_n_c14
samtec_p_c15
samtec_n_c15
samtec_p_c16
samtec_n_c16
C
VCC
COMP16
FDC
DelayCount(15:0)
A[15:0]
EQ
B[15:0]
D
Q
CLR
Delay_C
CC16CE
LVDS_TRX_DE_C
INV
DelayCntrCLK
CE
C
Q[15:0]
CEO
TC
CLR
LVDS_TRX_DE_C
D
XILINX
Title: PMC top level. Memory Board Interface - C
Name: Bradley Hall - SNAP Memory Test
Date: September 10, 2003
Sheet 7 of 8


1
2
3
4
5
6
7
8
MemBrdCtlOUT_D(0)
MemBrdCtlOUT_D(1)
MemBrdCtlOUT_D(2)
MemBrdCtlOUT_D(3)
BUF
TR_LVDS_D
CE_LVDS_D
CLE_LVDS_D
ALE_LVDS_D
OBUFDS
samtec_p_d1
samtec_n_d1
R52
samtec_p_d2
samtec_n_d2
R50
samtec_p_d3
samtec_n_d3
R46
samtec_p_d4
samtec_n_d4
R51
A
MemBrdCtlOUT_D(4)
MemBrdCtlOUT_D(5)
MemBrdCtlOUT_D(6)
RE_LVDS_D
WE_LVDS_D
WP_LVDS_D
samtec_p_d5
samtec_n_d5
R43
samtec_p_d6
samtec_n_d6
R45
samtec_p_d7
samtec_n_d7
R40
samtec_p_d8
samtec_n_d8
R49
IBUFDS
RB_LVDS_D
MemBrdCtrlIN_D(0)
IO_Direction_D
IO_OUT_LVDS_D(0)
IO_IN_LVDS_D(0)
IO_OUT_LVDS_D(1)
IO_IN_LVDS_D(1)
IO_OUT_LVDS_D(2)
IO_IN_LVDS_D(2)
IO_OUT_LVDS_D(3)
IO_IN_LVDS_D(3)
IO_OUT_LVDS_D(4)
IO_IN_LVDS_D(4)
IO_OUT_LVDS_D(5)
IO_IN_LVDS_D(5)
IO_OUT_LVDS_D(6)
IO_IN_LVDS_D(6)
IO_OUT_LVDS_D(7)
IO_IN_LVDS_D(7)
IOBUFDS
T
I
O
IO
IOB
R41
samtec_p_d9
samtec_n_d9
R42
samtec_p_d10
samtec_n_d10
R35
samtec_p_d11
samtec_n_d11
R36
samtec_p_d12
samtec_n_d12
39
samtec_p_d13
samtec_n_d13
R33
samtec_p_d14
samtec_n_d14
R37
samtec_p_d15
samtec_n_d15
R38
samtec_p_d16
samtec_n_d16
D
TR_LVDS_D
RE_LVDS_D
NAND2
When LVDS_TRX_DE is '1', then the LVDS Transciever on the Memory Board is driving signals to the PMC.
The equivalent equation is:
LVDS_TRX_DE = TR_LVDS
LVDS_TRX_DE_D
B
This is emulating what is on the memory board.
LVDS_TRX_DE is a copy of the Transceiver_T/R signal on the SNAP Memory Board schematic.
When LVDS_TRX_DE = '1', the Memory Board is driving LVDS_IO signals to the PMC.
LVDS_TRX_DE
Delay is to account for bus turnaround time and avoid bus contention.
Delay is determined by DelayCount(15:0) value * DelayCntrCLK period
Delay
~5.24m sec
IO_Direction
When IO_Direction = '1', PMC is receiving.
When IO_Direction = '0', PMC is driving.
C
Desired waveforms.
Delay_D
LVDS_TRX_DE_D
AND2B1
INV
IO_Direction_D
VCC
COMP16
DelayCount(15:0)
A[15:0]
EQ
B[15:0]
FDC
D
Q
C
CLR
Delay_D
CC16CE
LVDS_TRX_DE_D
INV
DelayCntrCLK
CE
C
Q[15:0]
CEO
TC
CLR
LVDS_TRX_DE_D
D
XILINX
Title: PMC top level. Memory Board Interface - D
Name: Bradley Hall - SNAP Memory Test
Date: September 10, 2003
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