

ADC Interface Card User's Guide

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7/27/2005

Card Description

The ADC Interface Card uses the Maxim MAX105ECS dual channel 6 bit analog to digital converter (ADC) which has a maximum sampling speed of 800Msps. Each channel has differential inputs that can also be used single ended. Each channel has two sets of 6 bit differential LVDS outputs. The card is designed for flexibility with several options determined by which resistors or capacitors are assembled.

Overall Printed Circuit Board Description

The ADC Interface Card PCB layout is shown in figure 1.

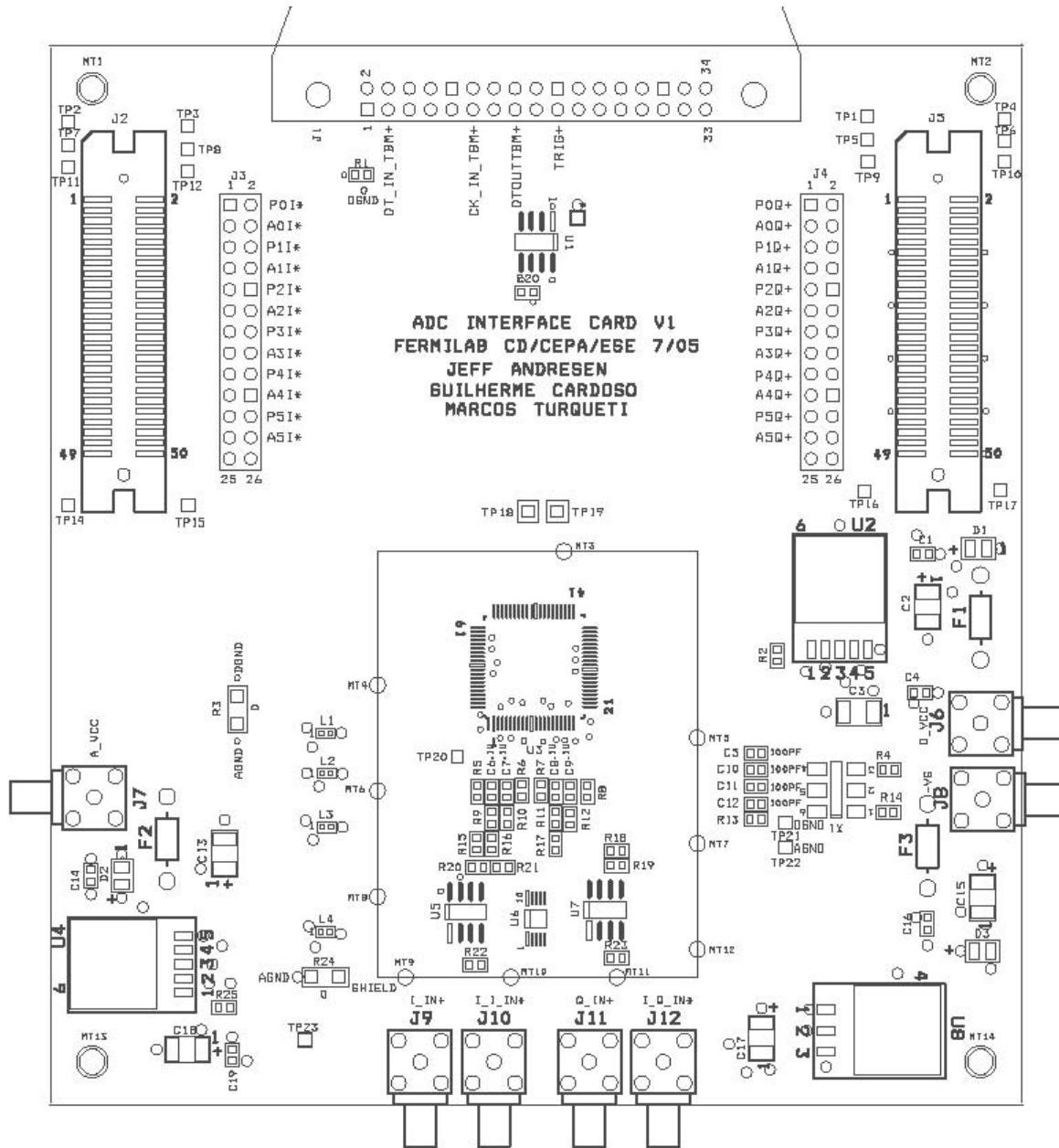


Figure 1: ADC Interface Card PCB Layout

The ADC Interface card is 4.6" x 5.0". U3 is the ADC I.C. J9 is the positive analog input and J10 is the negative analog input for the ADC I channel. J11 is the positive analog input and is the negative analog input for the ADC Q channel. The channels can be used single ended by only using the positive inputs. J2 is a 3M 50 pin connector with the I channel digital signals. J3 is a 100 mil pitch header for probing the I channel signals. J5 is a 3M 50 pin connector with the Q channel digital signals. J4 is a 100 mil pitch header for probing the Q channel signals. These 3M connectors can interface with the PTA.

U5 and U6 are Analog Devices AD8001 amplifiers for the positive analog inputs. U6 is a Maxim Max5450EUB digital potentiometer that is remotely controlled by control signals coming from connector J5. The clock can either come from the X1 crystal oscillator or from the J5 PTA connector.

J1 is a 34 pin right angle ribbon connector that interfaces with the TBM. U1 is a National Semiconductor DS90LV001 LVDS buffer that buffers the signals DT_OUT_TBM and DT_IN_TBM going between the TBM and the PTA. J6, J7, and J8 are used to power the PCB.

There is a 1.5" x 2" area with mounting holes for a Leader Tech EMI noise shield to cover the ADC and the analog signals. The shield cover is ventilated and may be removed. Mounting a 0 ohm resistor for R24 connects the shield to analog ground (AGND).

The PCB has four layers. Layer 1 has most of the signal traces which have a 100 ohm edge coupled differential impedance. Layer 2 is a split ground plane with digital ground under the digital signals and over digital power. Layer 2 also has analog ground which is under the analog signals and over the analog powers. Layer 3 is a split power plane. Digital power is under digital ground and the analog powers are under analog ground. Layer 4 is the PCB bottom and has the remaining 100 ohm differential edge coupled traces. Mounting a 0 ohm resistor for R3 or connecting TP21 to TP22 connects digital ground to analog ground.

ADC Operation

The Maxim MAX105 ADC is a two channel ADC that has a maximum sampling rate of 800Msps with 6 bit digital LVDS outputs. The analog inputs can be differential or single ended with a +/- 400mV full scale input range. Each channel has two sets of digital outputs. The I channel has outputs P0I:P5I and A0I:A5I. The Q channel has outputs P0Q:P5Q and A0Q:A5Q.

The ADC Interface Card is designed for flexibility for the analog ADC inputs and ADC clocking. For single ended inputs through the amplifier, use 0 ohm resistors for R10 and R12. Use 0 ohm resistors for R15 and R19 to bypass the amplifier. The gain of the amplifier can be remotely controlled from the PTA with the MAX5450EUB dual digital potentiometer. INC* increments the pot to the next value. CS1* and CS2* enables that pot to have its value changed. U/D* controls whether the incremental change is up or down.

Assemble C10 and C11, and do not assemble C5 and C12 to clock the ADC from the crystal oscillator. The frequency will be determined by the speed of the oscillator. Assemble C5 and C12, and do not assemble C10 and C11 to clock the ADC using a clock from the PTA. The ADC can use clock signal levels that can be a sine wave from 500mVpp to 2Vpp, LVDS, ECL, or PECL. When the clock is being received from the PTA, the X1 crystal oscillator can have its power disabled to minimize clock PCB noise by not assembling either R14 or R4.

The P outputs are the primary outputs. The A outputs are the auxiliary outputs. The data in the A outputs is delayed by one clock cycle from the data in the P outputs.

ADC Interface Card Powering

The ADC Interface card requires three power supplies. The ADC requires analog +5V (A_VCCIN) for the input section and digital +3.3V (D_VCC) for the LVDS outputs. The amplifiers also use A_VCCIN and analog -5V (-VS). These voltages are supplied through on board regulators. J7 supplies A_VCCIN and should be +5.5V to supply the U4 regulator. J6 supplies D_VCC and should be +3.8V to supply the U2 regulator. J8 supplies -VS and should be -5.6V to supply the U8 regulator. The powers are listed in table 1.

Voltage	Lemo Connector	PCB Input Voltage	Regulator Output Voltage
A_VCCIN	J7	+5.5V	+5.0V
D_VCC	J6	+3.8V	+3.3V
-VS	J8	-5.6V	-5.0V

Table 1: ADC Interface Card Powers

The ADC has four analog power pins. AVCCIN leaves the U4 regulator output. Each analog power pin on the ADC is then supplied by separate power plane splits (A_VCC, A_VCCR, A_VCCI, and A_VCCQ). Each of these four analog powers are separated from AVCCIN with ferrite beads.

Connector Pinouts

J2 PTA Connector Pinout			
1	J2_TP1	2	J2_TP2
3	J2_TP3	4	J2_TP4
5	J2_TP5	6	J2_TP6
7	P0I+	8	P0I*
9	A0I+	10	A0I*
11	DGND	12	DGND
13	P1I+	14	P1I*
15	A1I+	16	A1I*
17	P2I+	18	P2I*
19	A2I+	20	A2I*
21	DGND	22	DGND
23	P3I+	24	P3I*
25	A3I+	26	A3I*
27	P4I+	28	P4I*
29	A4I+	30	A4I*
31	DGND	32	DGND
33	P5I+	34	P5I*
35	A5I+	36	A5I*
37	J2_TP37	38	J2_TP38
39	TRIG+	40	TRIG*
41	DGND	42	DGND
43	DT_OUT_TBM+	44	DT_OUT_TBM*
45	DT_IN_TBM+	46	DT_IN_TBM*
47	CK_IN_TBM+	48	CK_IN_TBM*
49	DGND	50	DGND

J5 PTA Connector

1	J1_TP1	2	J1_TP2
3	J1_TP3	4	J1_TP4
5	J1_TP5	6	J1_TP6
7	CK_OUT_ADC+	8	CK_OUT_OUT*
9	P0Q+	10	P0Q*
11	DGND	12	DGND
13	A0Q+	14	A0Q*
15	P1Q+	16	P1Q*
17	A1Q+	18	A1Q*
19	P2Q+	20	P2Q*
21	DGND	22	DGND
23	A2Q+	24	A2Q*
25	P3Q+	26	P3Q*
27	A3Q+	28	A3Q*
29	P4Q+	30	P4Q*
31	DGND	32	DGND
33	A4Q+	34	A4Q*
35	P5Q+	36	P5Q*
37	A5Q+	38	A5Q*
39	CS1*	40	CS2*
41	DGND	42	DGND
43	U/D*	44	INC*
45	J1_TP45	46	J1_TP46
47	CK_IN_ADC+	48	CK_IN_ADC*
49	DGND	50	DGND

J1 TBM 34 Pin Connector

1	DGND	2	DGND
3	DT_IN_TBM+	4	DT_IN_TBM*
5	DGND	6	DGND
7	NC	8	NC
9	DGND	10	DGND
11	CK_IN_TBM+	12	CK_IN_TBM*
13	DGND	14	DGND
15	DT_OUT_TBM+	16	DT_OUT_TBM*
17	DGND	18	DGND
19	TRIG+	20	TRIG*
21	DGND	22	DGND
23	NC	24	NC
25	NC	26	NC
27	NC	28	NC
29	NC	30	NC
31	NC	32	NC
33	NC	34	NC

Safety

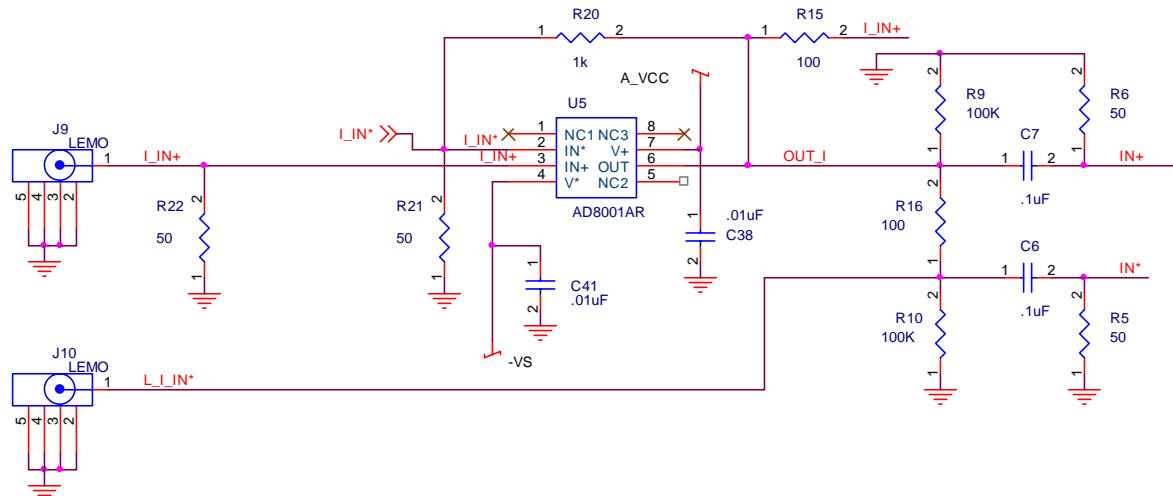
The three input powers are protected from over current with 1 amp socketed Pico fuses. AVX TransGuard transient voltage suppressors protect the three power inputs from over voltage.

Parts List

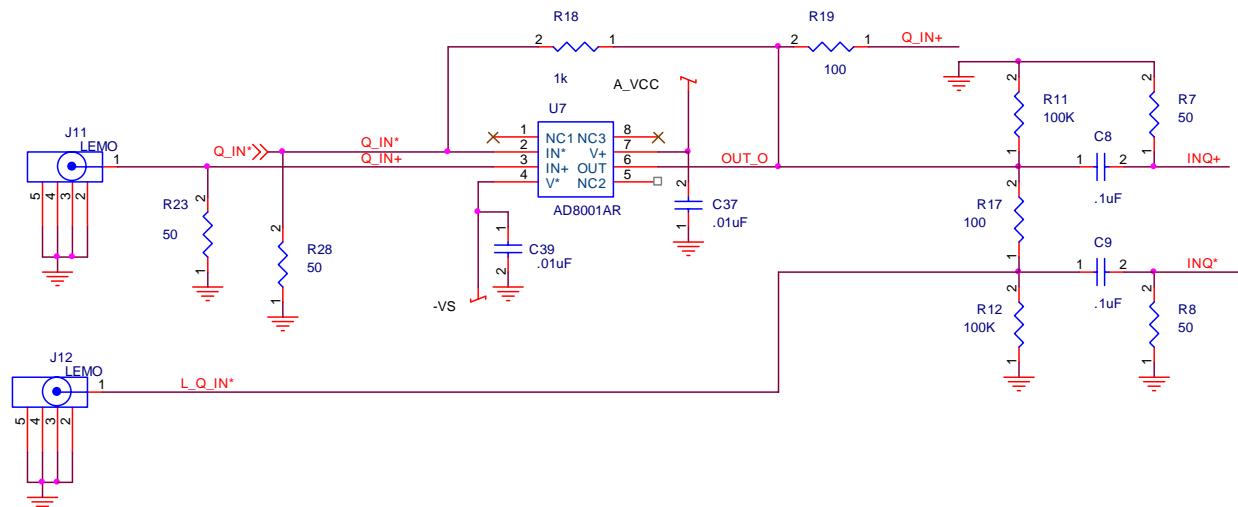
Part	Description	Quantity	Ref. Designators
Panasonic Digikey PCC1784CT-ND	0603 .01uF cap	23	C1,C4,C14,C16,C19,C20,C21,C22,C25,C27,C29,C31,C33,C34,C35,C36,C37,C38,C39,C40,C41,C42,C43
Nichicon Digikey 493-2357-1-ND	22uF, 10V size B cap	6	C2,C3,C13,C15,C17,C18
Panasonic Digikey PCC101ACVCT-ND	0603 100pF cap	4	C5,C10,C11,C12
Panasonic Digikey PCC1762CT-ND	0603 .1uF cap	4	C6,C7,C8,C9
Panasonic Digikey PCC470ACVCT-ND	0603 47pF cap	6	C23,C24,C26,C28,C30,C32
AVX Digikey 478-2505-1-ND	0805 3.3V TVS	1	D1
AVX Digikey 478-2506-1-ND	0805 5V TVX	2	D2, D3
Pico Fuse	1 A Pico fuse	3	F1, F2, F3
Amp 2-331272-2	fuse sockets	6	
3M Fermilab Stockroom 1435-710500	34 pin RT header with ejectors	1	J1
3M P50LE-050P1-SML-TGF	50 pin PTA conn	2	J2, J5
Samtec TSW-150-07-G-S	header strips	2	J3, J4
Lemo Fermilab Stockroom 1435-4400	RT PCB Lemo conn	7	J6,J7,J8,J9,J10,J11,J12
Digikey 490-1006-1-ND	0402 ferrite bead	4	L1, L2, L3, L4
0603 0 ohm resistor	0 ohm 0603	3	R1,R4,R14
1206 0 ohm resistor	0 ohm 1206	2	R3, R24
Digikey P51GCT-ND	50 ohm 0603	8	R5,R6,R7,R8,R21,R22,R23,R28
Digikey P100KHCT-ND	100k 0603	4	R9,R10,R11,R12
Digikey P100HCT-ND	100 ohm 0603	5	R13,R15,R16,R17,R19
Digikey P1.00KHCT-ND	1k ohm 0603	2	R18, R20
Digikey P10.0KHCT-ND	10k ohm 0603	2	R2, R25
Digikey P2.00KHCT-ND	2k ohm 0603	2	R27, R30
National Digikey DS90LV00TM-ND	3.3V LVDS buffer	1	U1
National Digikey LP387ES-3.3-ND	3.3V regulator	1	U2
Maxim MAX105ECS	ADC	1	U3
National Digikey LP3874ES-5.0-ND	5V regulator	1	U4
Analog Devices Digikey AD800ART-REEL7CT-ND	Amp	2	U5, U7
Maxim MAX5450EUB	digital pot	1	U6
National Digikey LM2990S-5.0-ND	-5V regulator	1	U8
Epson Digikey SE361CT-ND	250MHz xtal if used	1	X1
Epson Digikey SE3610CT-ND	125MHz xtal if used	1	X1
Leader Tech 24-CBSFSV-1.5x2.0x.2	EMI shield if used	1	

Schematic

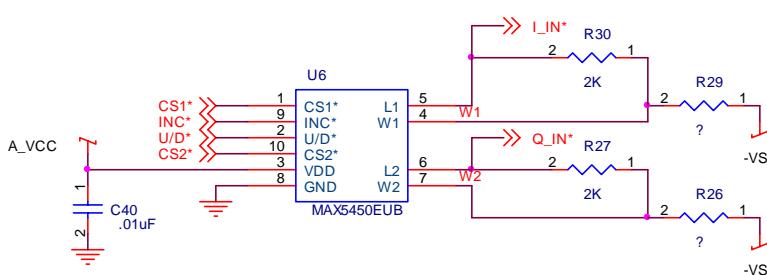
The following is the schematic in sectional format.



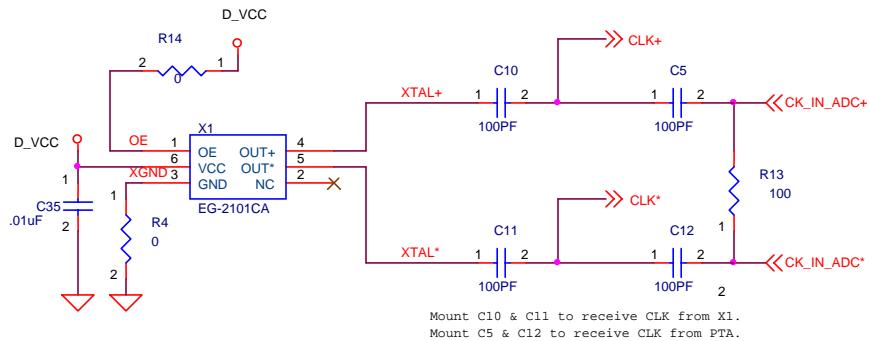
I Channel Inputs and Amplifier



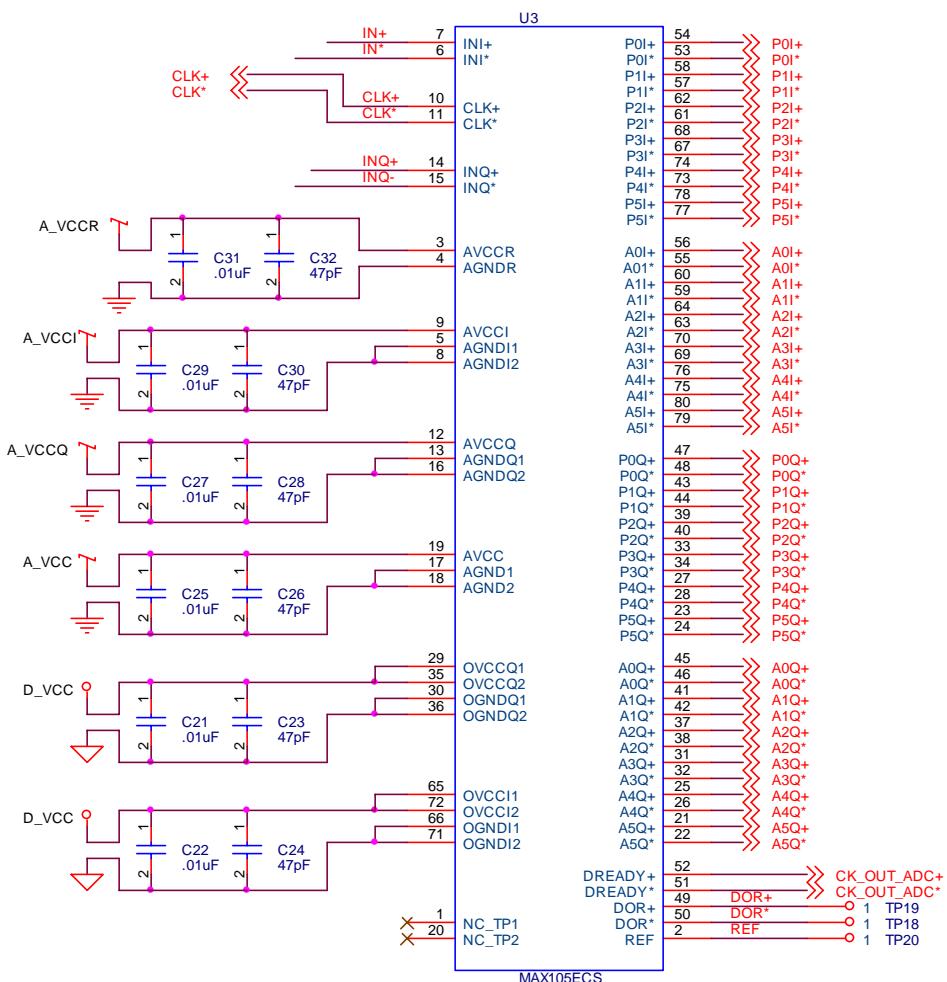
Q Channel Inputs and Amplifier



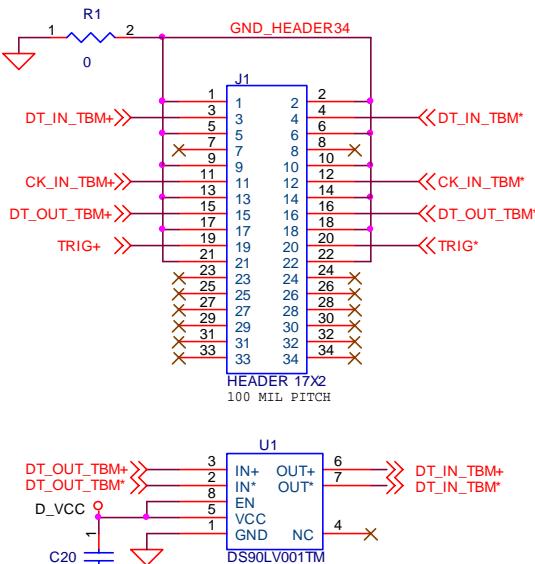
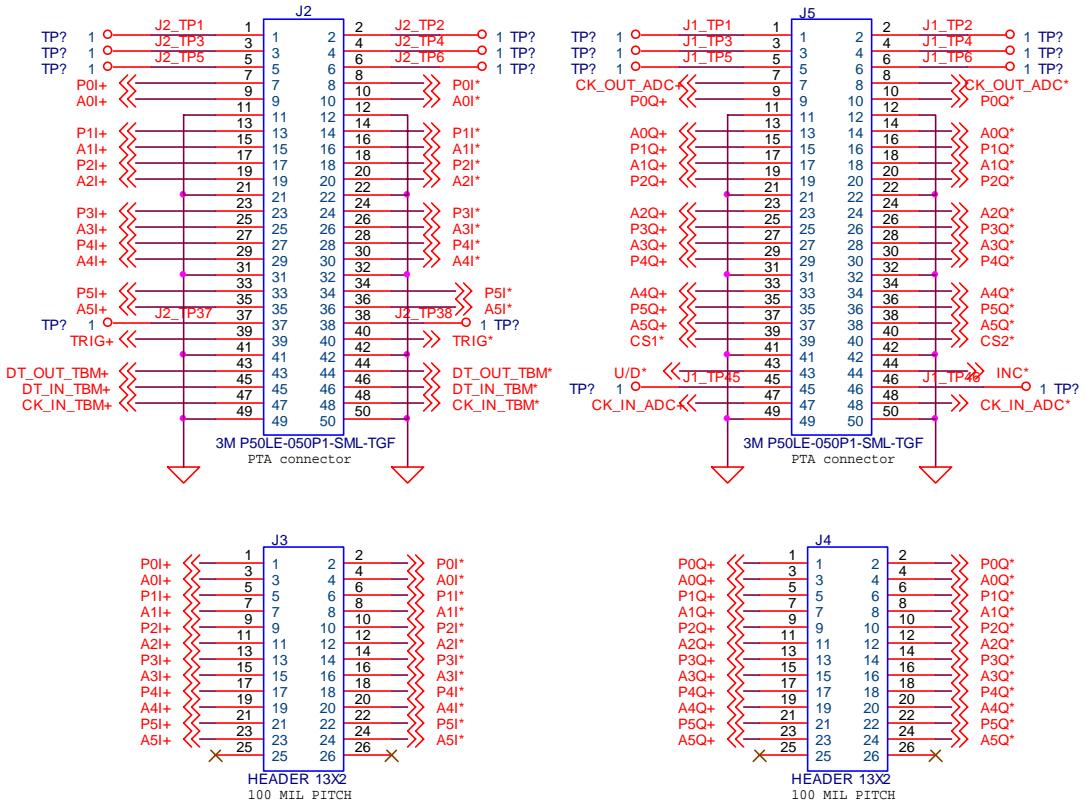
Maxim Max5450EUB Digital Potentiometer



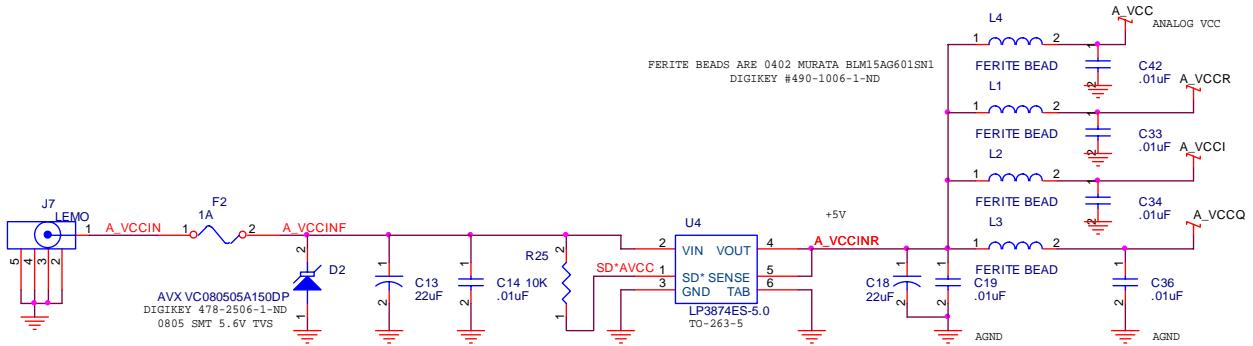
Epson Crystal Oscillator and PTA Clock Selection Circuit



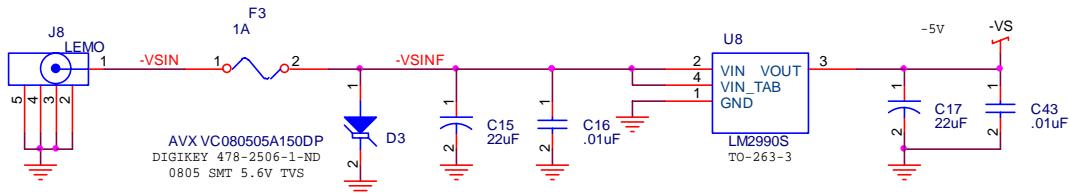
Maxim Max105ECS ADC Circuit



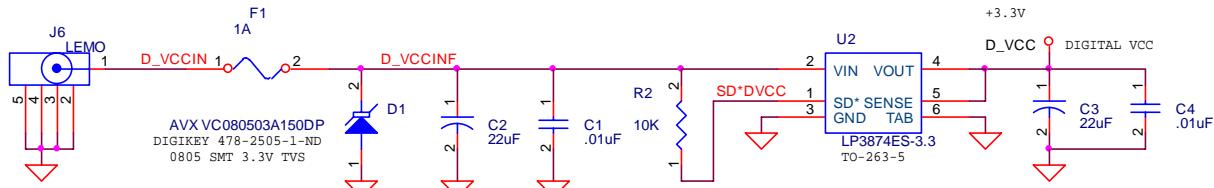
TBM Connector and LVDS Buffer

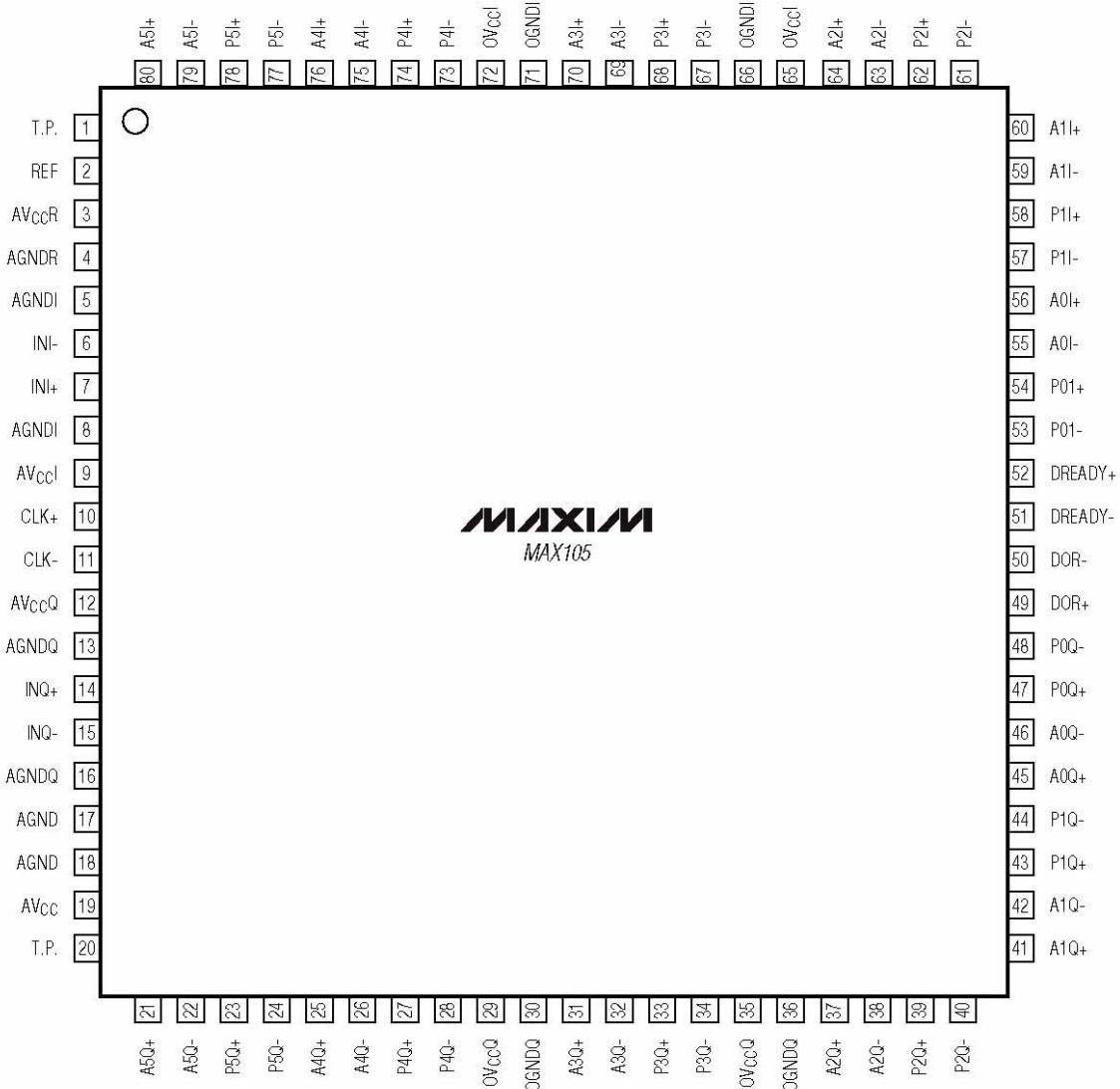


Positive Analog Voltage Supply Circuit



Negative Analog Voltage Supply Circuit





Maxim MAX105 Pinout