

## **Notes on the trigger circuit for the CMS Pixel Test Stand:**

**VHDL Code:** pta\_L1\_trig\_7.vhd

The trigger circuit has been implemented as a state machine using the Aldec Active-HDL 6.3 development tools. The VHDL code is automatically generated from the corresponding state diagram (pta\_L1\_trig\_7.asf).

### **Block Inputs:**

#### ***clock\_40\_0:***

Type: std\_logic (clock)

Description: This is the state machine clock for the block. The nominal frequency for this clock is 40 Mhz. The state machine transitions are in response to a rising edge on this clock.

#### ***mode:***

Type: std\_logic

Description: This input is used to select the mode of operation of the trigger block:

- mode = '0' selects coincidence triggered operation. In this mode, the trigger circuit output, trig\_out, is generated in response to the arrival of a signal on the input, co\_in.
- mode = '1' selects periodic triggered operation. In this mode, the trigger output, trig\_out, is generated periodically according to the settings of other timing inputs (see count\_in[11:0] and

#### ***reset\_n:***

Type: std\_logic

Description: This is the block reset input for this firmware. The reset is synchronous with the state machine clock and the signal is active low (reset\_n = '0' results in a reset of the block).

#### ***co\_in:***

Type: std\_logic

Description: This input is used to signal that a coincidence has occurred and that a trigger is to be delivered in response to this input. A response will be requested if co\_in = '1'.

#### ***burst\_in[7:0]:***

Type: std\_logic\_vector

Description: In either periodic mode or triggered mode, if more than one encoded trigger is desired at the appropriate time (in response to co\_in or at the periodically scheduled time), a value greater than "00000000" on this input will result in the production of the corresponding number of encoded trigger sequences.

#### ***cal\_in[7:0]:***

Type: std\_logic\_vector

Description: Since calibration triggers actually generate a pair of encoded triggers (“100” followed by “110”), there needs to be a control which specifies how much time passes between the two encoded trigger triplets. This is controlled by cal\_in[7:0]. The setting on this input controls the number of 25 nsec intervals that elapse between the two trigger sequences.

***count\_in[11:0]:***

Type: std\_logic\_vector

Description: This input is used to adjust the frequency between trigger outputs when the block is operated in periodic mode. The value on this input is used as a divisor on the maximum periodic clock frequency of 2 MHz. For example, a value of “00000100” on this input will mean that 4 cycles at 2 Mhz will elapse between adjacent triggers, resulting in a periodic trigger signal at 500 kHz.

***trig\_in[1:0]:***

Type: std\_logic

Description: This vector is used to encode the desired trigger output which appears as a three bit code on the trig\_out output. The following choices are available:

“00” – this results in a trigger output of “100”

“10” – this results in a trigger output of “110”

“11” – this results in a trigger output of “111”

“01” – this input is reserved to generate a calibration trigger output. In this case, the trigger output is a pair of three bit codes, “100” followed by “110”. The number of 25 ns intervals between the “100” code and the “110” code is determined by the setting on the control input, cal\_in[7:0].

**Block Outputs:**

***trig\_out:***

Type: std\_logic

Description: This is the output signal that is sent out of the PMC FPGA and is delivered as an input to the TBM board. The signal is always encoded as three consecutive bits. These bits have a bit period of 25 ns (corresponding to a 40 MHz clock). This timing is derived from the use of the 40 Mhz clock\_40\_0 as the state machine clock for the block.

***busy:***

Type: std\_logic

Description: This output can be used to indicate that, when the block is in the triggered mode (mode = ‘0’), the block is currently active processing the output in response to a coincidence trigger input. No changes to the mode or other settings will be accepted while the block is busy.

**Internal Registers:**

Note that the user of this block does not need to be concerned with the details of these internal registers. They are transparent to the inputs and outputs.

***burst\_count [7:0]:***

Type: std\_logic\_vector

Description: When burst\_in[7:0] is not equal to “00000000”, this register is used as a count down register to increment the number of triggers left to complete a burst.

***cal\_count[7:0]:***

Type: std\_logic\_vector

Description: This register is used as a down counter to implement the time interval between the “100” part of a calibration trigger pair and the following “110” portion of the pair.

***base\_count[11:0]:***

Type: std\_logic\_vector

Description: This register is used as a down counter to implement the maximum 2 MHz periodic frequency by counting modulo(base\_val) on the 40 MHz state machine clock.

***count\_down[11:0]:***

Type: std\_logic\_vector

Description: This register is used as a down counter to implement the requested periodic frequency for periodic mode operation. The counter implements a modulo(count\_in) counter on the base frequency of 2 MHz.

**Constants:**

***base\_val[11:0] = “000000010100”***

Type: std\_logic\_vector

Description: This value has the effect of making the maximum clock frequency for periodic trigger operation equal to 2 MHz. It is used as a divisor on the 40 MHz state machine clock (40 MHz/20 = 2 MHz).

***zero\_8[7:0] = “00000000”***

Type: std\_logic\_vector

Description: This is just a constant of convenience for writing code.

***one\_8[7:0] = “00000001”***

Type: std\_logic

Description: This is just a constant of convenience for writing code.

***zero\_12[11:0] = “000000000000”***

Type: std\_logic\_vector

Description: This is just a constant of convenience for writing code.

***one\_12[11:0] = “000000000001”***

Type: std\_logic\_vector

Description:

***three\_8[7:0] = "00000011"***

Type: std\_logic

Description: This is used to adjust the offset of the cal\_count internal register which is used to control the number of 25 nsec intervals between the end of the "100" code and the beginning of the "110" code in a calibration trigger output pair.

### **Description of Operation:**

There are three modes of operation for this block:

1. Periodic mode
2. Coincidence Standard Mode
3. Coincidence Calibration Mode

#### ***Periodic Mode:***

In this mode, the trigger code selected (according to the trig\_in[1:0] settings) will be output with a fixed repetition frequency. The repetition frequency is controlled by the setting on the input count\_in[11:0].

The following controls must be specified for this mode:

reset\_n = '1'

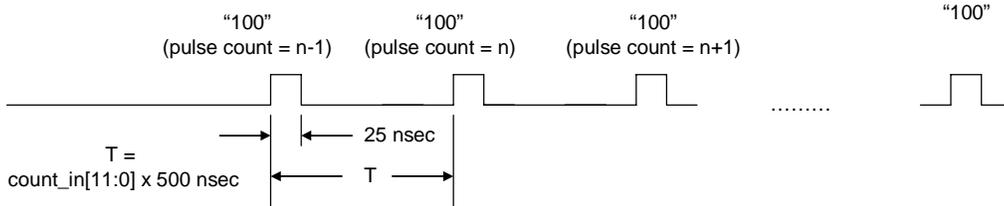
mode = '1'

count\_in[11:0]

trig\_in[1:0]

cal\_in[11:0] (for trig\_in = "01" only)

Figure 1 illustrates the timing for an example of periodic mode:



Trigger Timing (Periodic Mode)  
Example: trig\_in = "00"

**Figure 1**

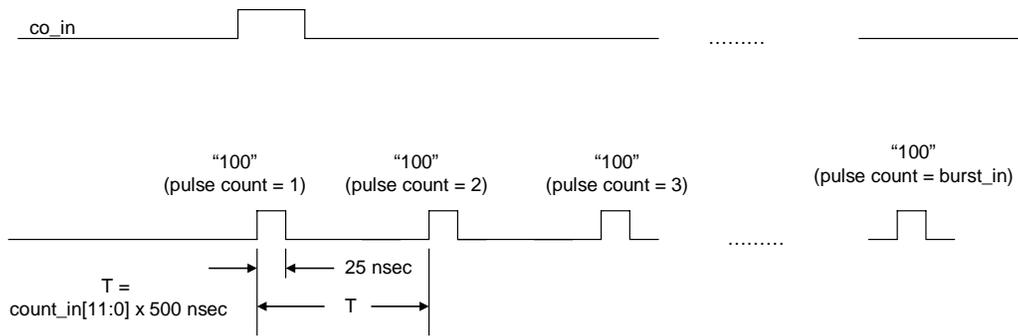
***Coincidence Triggered Standard Mode:***

In this mode, a trigger sequence (as determined by the setting of trig\_in[1:0]) will be output only in response to the arrival of a co\_in input. Multiple trigger sequences will be output if burst\_in is not equal to "00000000". In this case, the time between successive triggers is set by 25 nsec times the value on count\_in[11:0]. The number of multiple triggers is set by burst\_in[7:0].

The following controls must be specified for this mode:

- reset\_n = '1'
- mode = '0'
- count\_in[11:0] (if burst\_in[7:0] is not equal to "00000000")
- trig\_in[1:0] (Not equal to "01")

Figure 2 illustrates the timing for an example of coincidence triggered standard mode:



Burst Trigger Timing (Triggered Mode)  
 Example: trig\_in = "00"

**Figure 2**

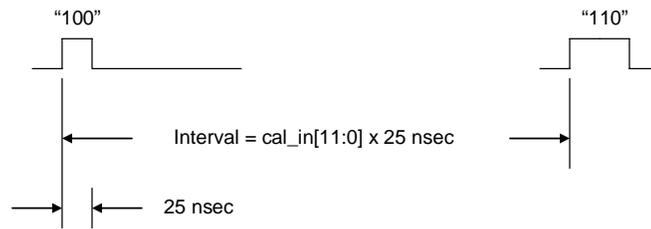
***Coincidence Triggered Calibration Mode:***

In this mode, a calibration trigger pair will be output only in response to the arrival of a co\_in input. Multiple trigger sequences will be output if burst\_in is not equal to "00000000". In this case, the time between successive triggers is set by 25 nsec times the value on count\_in[11:0]. The number of multiple triggers is set by burst\_in[7:0].

The following controls must be specified for this mode:

- reset\_n = '1'
- mode = '0'
- burst\_in[7:0]
- count\_in[11:0] (if burst\_in[7:0] is not equal to "00000000")
- trig\_in[1:0] (Must be equal to "01")
- cal\_in[11:0]

Figure 3 illustrates the timing for an example of coincidence triggered standard mode. In particular, it illustrates the use of cal\_in[11:0] to control the delay between the sequences that make up a calibration trigger:



Calibration Trigger Timing  
Interval Between "100" and "110" Sequences

**Figure 3**