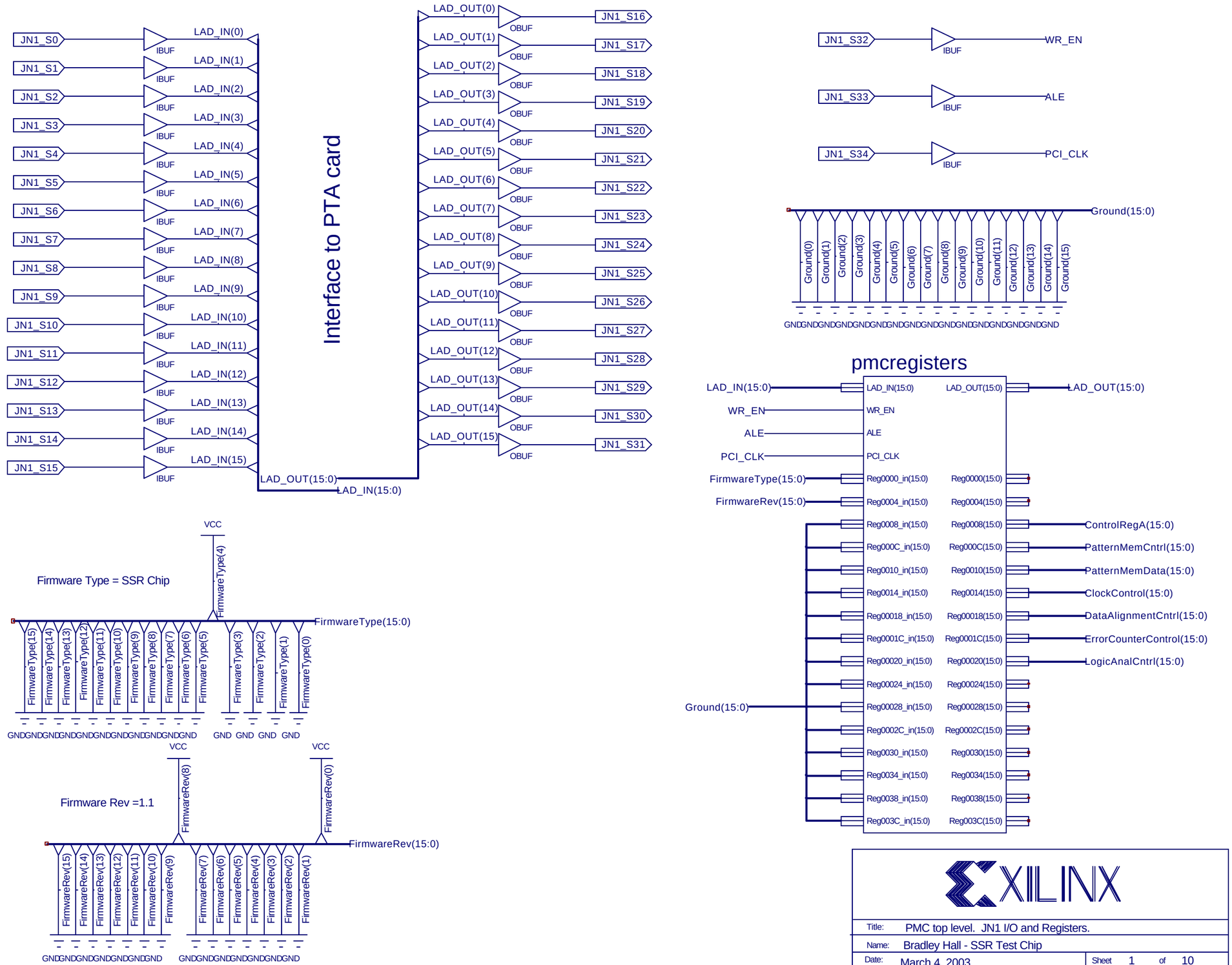
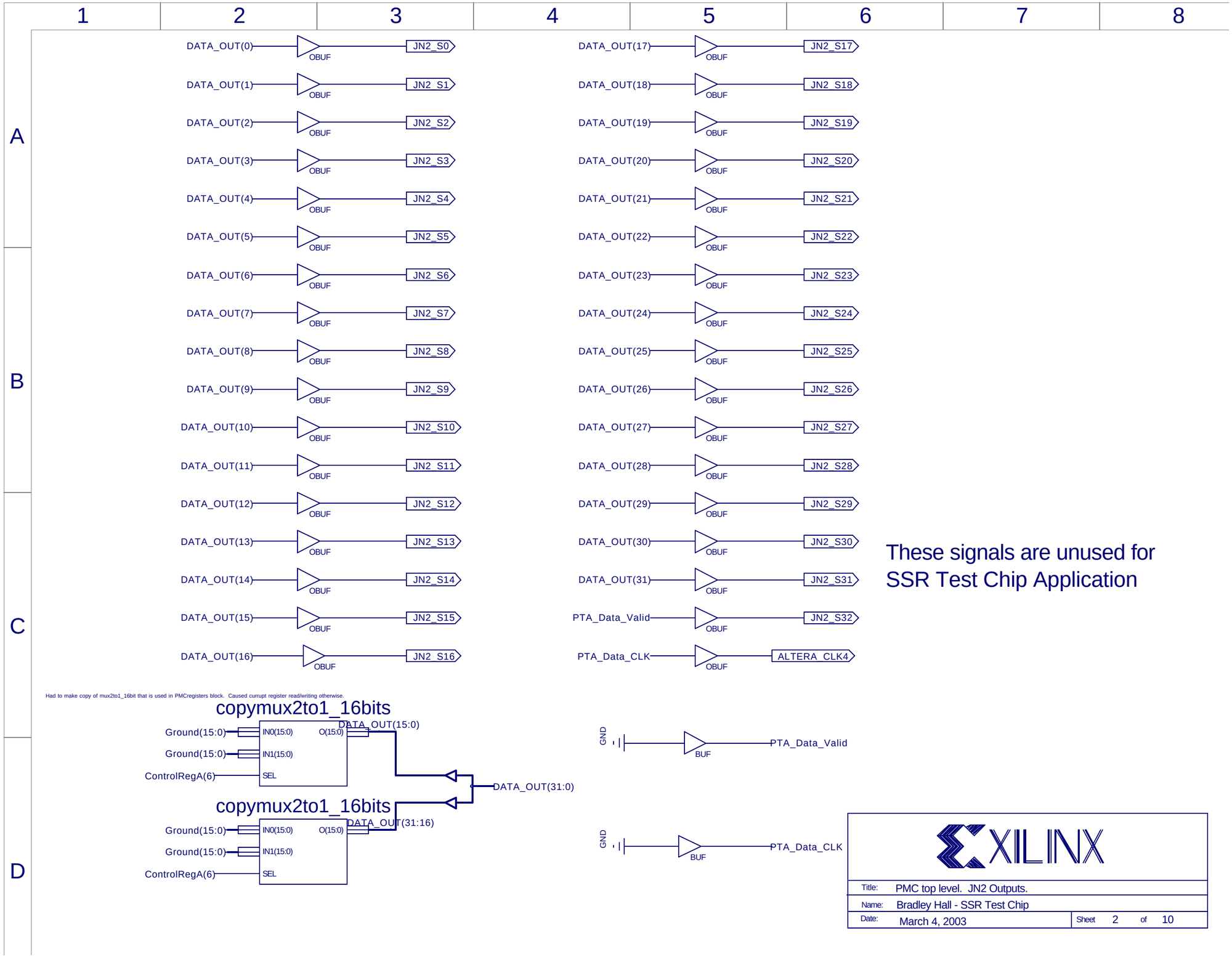
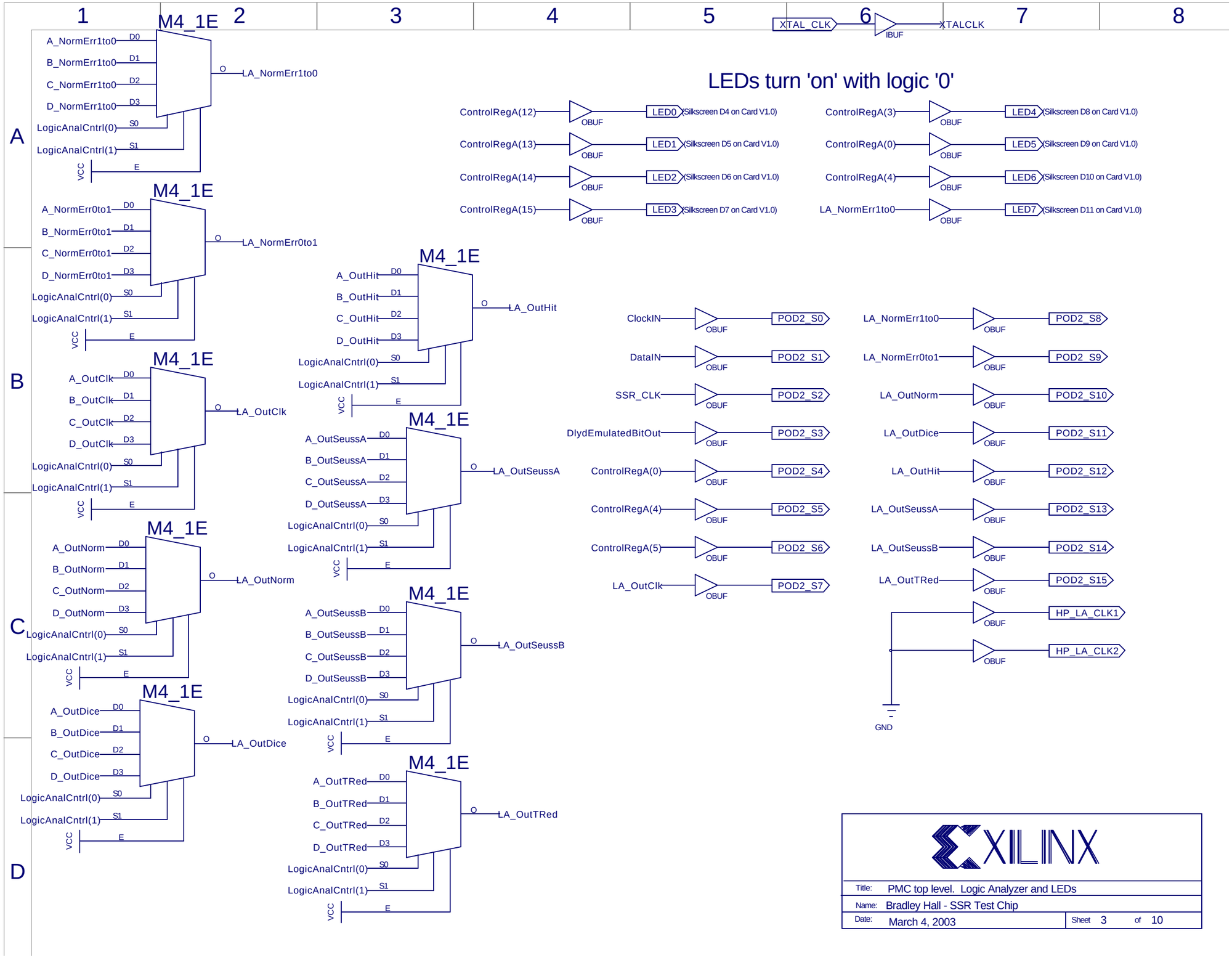
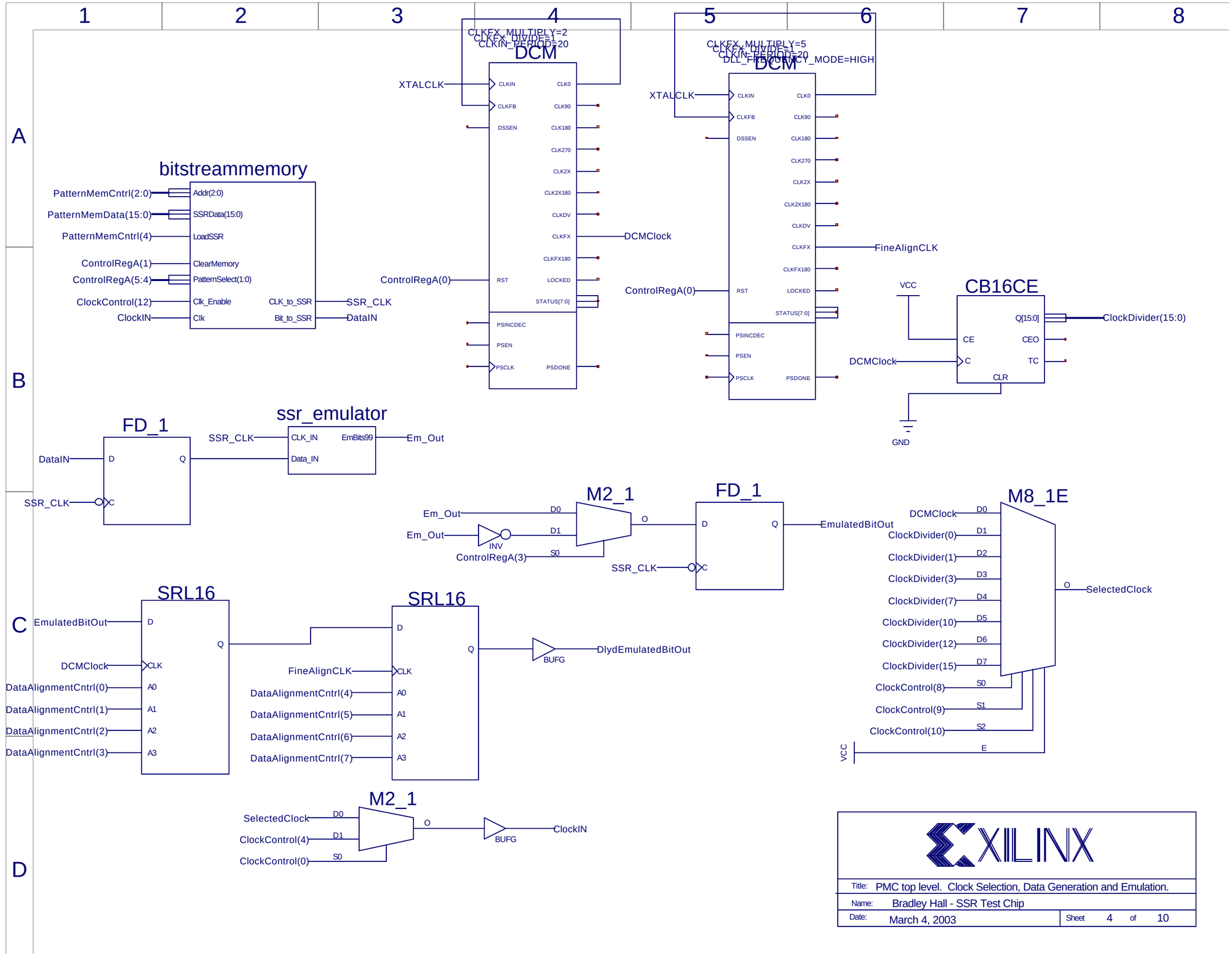

Interface to PTA card
JN1_S0
JN1_S1
JN1_S2
JN1_S3
JN1_S4
JN1_S5
JN1_S6
JN1_S7
JN1_S8
JN1_S9
JN1_S10
JN1_S11
JN1_S12
JN1_S13
JN1_S14
JN1_S15
IBUF
LAD_IN(0)
LAD_IN(1)
LAD_IN(2)
LAD_IN(3)
LAD_IN(4)
LAD_IN(5)
LAD_IN(6)
LAD_IN(7)
LAD_IN(8)
LAD_IN(9)
LAD_IN(10)
LAD_IN(11)
LAD_IN(12)
LAD_IN(13)
LAD_IN(14)
LAD_IN(15)
LAD_OUT(15:0)
LAD_IN(15:0)
OBUF
LAD_OUT(0)
LAD_OUT(1)
LAD_OUT(2)
LAD_OUT(3)
LAD_OUT(4)
LAD_OUT(5)
LAD_OUT(6)
LAD_OUT(7)
LAD_OUT(8)
LAD_OUT(9)
LAD_OUT(10)
LAD_OUT(11)
LAD_OUT(12)
LAD_OUT(13)
LAD_OUT(14)
LAD_OUT(15)
JN1_S16
JN1_S17
JN1_S18
JN1_S19
JN1_S20
JN1_S21
JN1_S22
JN1_S23
JN1_S24
JN1_S25
JN1_S26
JN1_S27
JN1_S28
JN1_S29
JN1_S30
JN1_S31
JN1_S32
JN1_S33
JN1_S34
WR_EN
ALE
PCI_CLK
Ground(15:0)
Ground(0)
Ground(1)
Ground(2)
Ground(3)
Ground(4)
Ground(5)
Ground(6)
Ground(7)
Ground(8)
Ground(9)
Ground(10)
Ground(11)
Ground(12)
Ground(13)
Ground(14)
Ground(15)
GND
pmcregisters
LAD_IN(15:0)
WR_EN
ALE
PCI_CLK
FirmwareType(15:0)
FirmwareRev(15:0)
Ground(15:0)
LAD_OUT(15:0)
Reg0000_in(15:0)
Reg0004_in(15:0)
Reg0008_in(15:0)
Reg000C_in(15:0)
Reg0010_in(15:0)
Reg0014_in(15:0)
Reg00018_in(15:0)
Reg0001C_in(15:0)
Reg00020_in(15:0)
Reg00024_in(15:0)
Reg00028_in(15:0)
Reg0002C_in(15:0)
Reg0030_in(15:0)
Reg0034_in(15:0)
Reg0038_in(15:0)
Reg003C_in(15:0)
Reg0000(15:0)
Reg0004(15:0)
Reg0008(15:0)
Reg000C(15:0)
Reg0010(15:0)
Reg0014(15:0)
Reg00018(15:0)
Reg0001C(15:0)
Reg00020(15:0)
Reg00024(15:0)
Reg00028(15:0)
Reg0002C(15:0)
Reg0030(15:0)
Reg0034(15:0)
Reg0038(15:0)
Reg003C(15:0)
ControlRegA(15:0)
PatternMemCntrl(15:0)
PatternMemData(15:0)
ClockControl(15:0)
DataAlignmentCntrl(15:0)
ErrorCounterControl(15:0)
LogicAnalCntrl(15:0)
Firmware Type = SSR Chip
VCC
FirmwareType(4)
FirmwareType(15:0)
FirmwareType(15)
FirmwareType(14)
FirmwareType(13)
FirmwareType(12)
FirmwareType(11)
FirmwareType(10)
FirmwareType(9)
FirmwareType(8)
FirmwareType(7)
FirmwareType(6)
FirmwareType(5)
FirmwareType(3)
FirmwareType(2)
FirmwareType(1)
FirmwareType(0)
GND
Firmware Rev =1.1
FirmwareRev(8)
FirmwareRev(0)
FirmwareRev(15:0)
FirmwareRev(15)
FirmwareRev(14)
FirmwareRev(13)
FirmwareRev(12)
FirmwareRev(11)
FirmwareRev(10)
FirmwareRev(9)
FirmwareRev(7)
FirmwareRev(6)
FirmwareRev(5)
FirmwareRev(4)
FirmwareRev(3)
FirmwareRev(2)
FirmwareRev(1)
GND
XILINX
Title: PMC top level. JN1 I/O and Registers.
Name: Bradley Hall - SSR Test Chip
Date: March 4, 2003
Sheet 1 of 10

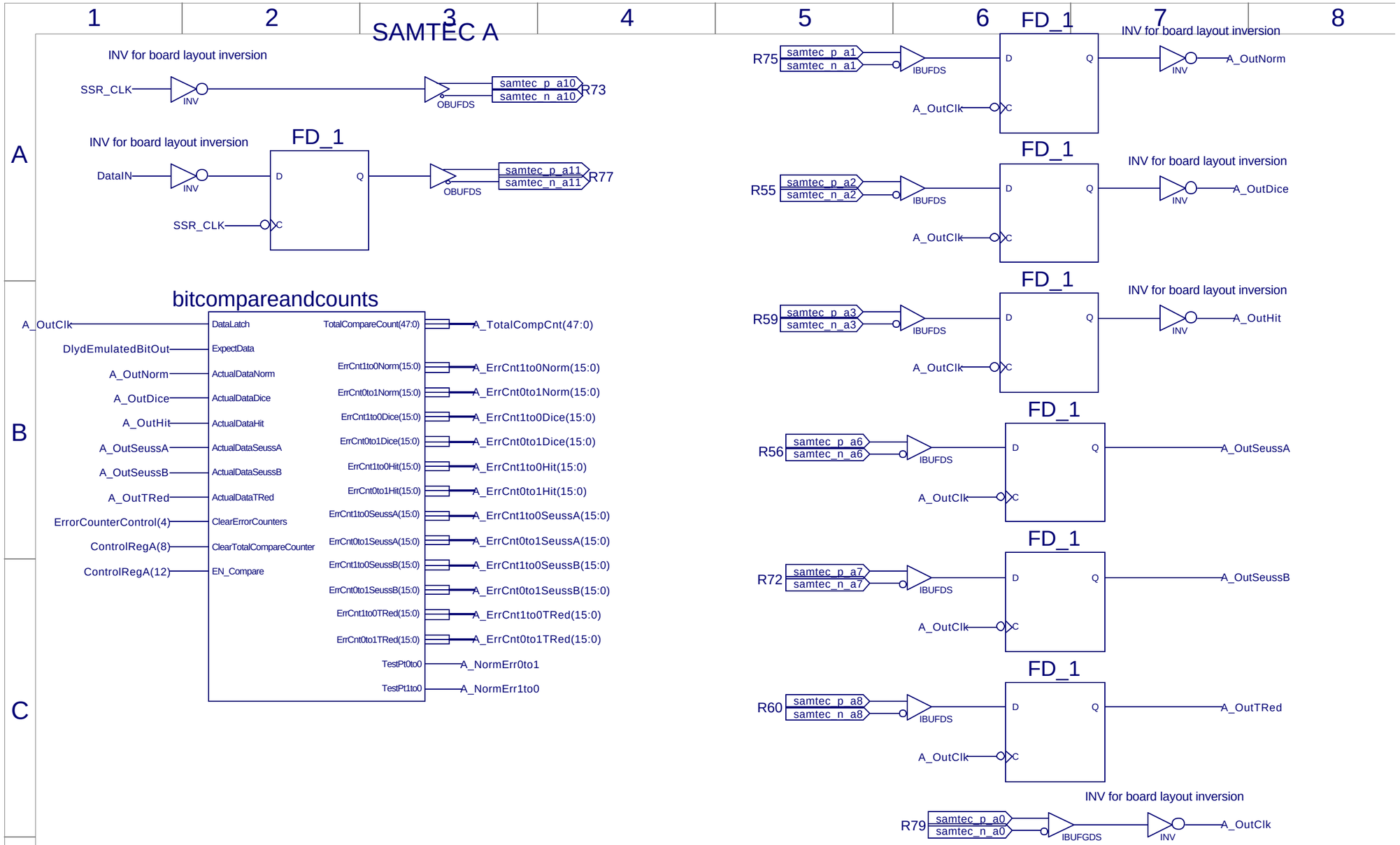


These signals are unused for SSR Test Chip Application


1
2
3
4
5
6
7
8
A
B
C
D
XTAL_CLK
IBUF
XTALCLK
LEDs turn 'on' with logic '0'
M4_1E
A_NormErr1to0
B_NormErr1to0
C_NormErr1to0
D_NormErr1to0
LogicAnalCntrl(0)
LogicAnalCntrl(1)
VCC
D0
D1
D2
D3
S0
S1
E
O
LA_NormErr1to0
A_NormErr0to1
B_NormErr0to1
C_NormErr0to1
D_NormErr0to1
LA_NormErr0to1
A_OutClk
B_OutClk
C_OutClk
D_OutClk
LA_OutClk
A_OutNorm
B_OutNorm
C_OutNorm
D_OutNorm
LA_OutNorm
A_OutDice
B_OutDice
C_OutDice
D_OutDice
LA_OutDice
A_OutHit
B_OutHit
C_OutHit
D_OutHit
LA_OutHit
A_OutSeussA
B_OutSeussA
C_OutSeussA
D_OutSeussA
LA_OutSeussA
A_OutSeussB
B_OutSeussB
C_OutSeussB
D_OutSeussB
LA_OutSeussB
A_OutTRed
B_OutTRed
C_OutTRed
D_OutTRed
LA_OutTRed
ControlRegA(12)
ControlRegA(13)
ControlRegA(14)
ControlRegA(15)
OBUF
LED0
LED1
LED2
LED3
(Silkscreen D4 on Card V1.0)
(Silkscreen D5 on Card V1.0)
(Silkscreen D6 on Card V1.0)
(Silkscreen D7 on Card V1.0)
ControlRegA(3)
ControlRegA(0)
ControlRegA(4)
LA_NormErr1to0
LED4
LED5
LED6
LED7
(Silkscreen D8 on Card V1.0)
(Silkscreen D9 on Card V1.0)
(Silkscreen D10 on Card V1.0)
(Silkscreen D11 on Card V1.0)
ClockIN
DataIN
SSR_CLK
DlydEmulatedBitOut
ControlRegA(0)
ControlRegA(4)
ControlRegA(5)
LA_OutClk
POD2_S0
POD2_S1
POD2_S2
POD2_S3
POD2_S4
POD2_S5
POD2_S6
POD2_S7
LA_NormErr1to0
LA_NormErr0to1
LA_OutNorm
LA_OutDice
LA_OutHit
LA_OutSeussA
LA_OutSeussB
LA_OutTRed
POD2_S8
POD2_S9
POD2_S10
POD2_S11
POD2_S12
POD2_S13
POD2_S14
POD2_S15
HP_LA_CLK1
HP_LA_CLK2
GND
XILINX
Title: PMC top level. Logic Analyzer and LEDs
Name: Bradley Hall - SSR Test Chip
Date: March 4, 2003
Sheet 3 of 10

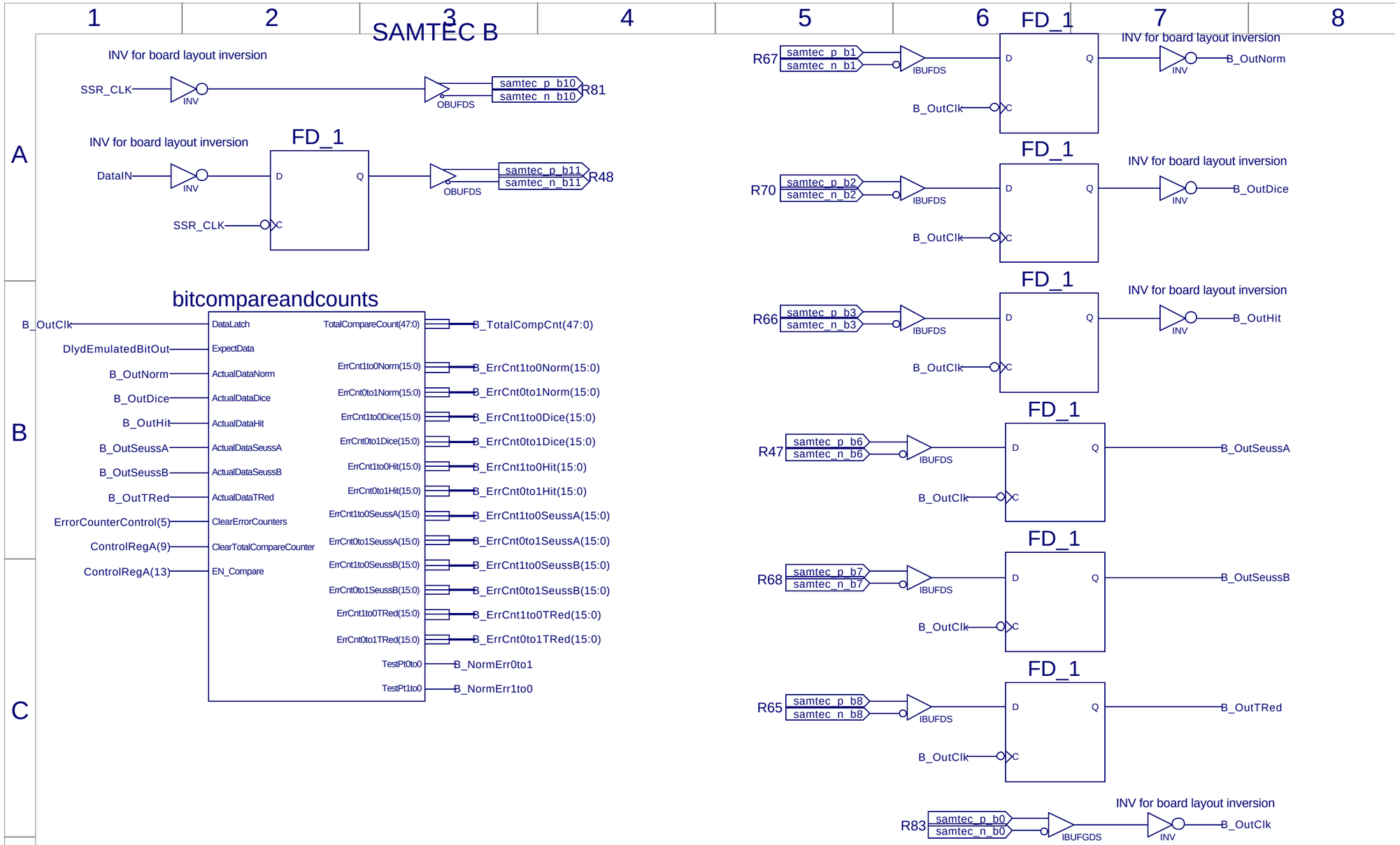

1
2
3
4
5
6
7
8
A
B
C
D
DCM
CLKFX_MULTIPLY=2
CLKFX_DIVIDE=1
CLKIN_PERIOD=20
XTALCLK
CLKIN
CLKFB
DSSEN
CLK0
CLK90
CLK180
CLK270
CLK2X
CLK2X180
CLKDV
CLKFX
CLKFX180
LOCKED
STATUS[7:0]
RST
PSINCDEC
PSEN
PSCLK
PSDONE
DCMClock
ControlRegA(0)
DCM
CLKFX_MULTIPLY=5
CLKFX_DIVIDE=1
CLKIN_PERIOD=20
DLL_FREQUENCY_MODE=HIGH
FineAlignCLK
bitstreammemory
PatternMemCntrl(2:0)
PatternMemData(15:0)
PatternMemCntrl(4)
ControlRegA(1)
ControlRegA(5:4)
ClockControl(12)
ClockIN
Addr(2:0)
SSRData(15:0)
LoadSSR
ClearMemory
PatternSelect(1:0)
Clk_Enable
Clk
CLK_to_SSR
Bit_to_SSR
SSR_CLK
DataIN
CB16CE
VCC
Q[15:0]
CE
CEO
TC
C
CLR
GND
ClockDivider(15:0)
FD_1
DataIN
D
Q
SSR_CLK
C
ssr_emulator
CLK_IN
EmBits99
Data_IN
Em_Out
M2_1
Em_Out
INV
ControlRegA(3)
D0
D1
S0
O
FD_1
EmulatedBitOut
M8_1E
DCMClock
ClockDivider(0)
ClockDivider(1)
ClockDivider(3)
ClockDivider(7)
ClockDivider(10)
ClockDivider(12)
ClockDivider(15)
ClockControl(8)
ClockControl(9)
ClockControl(10)
D2
D3
D4
D5
D6
D7
S1
S2
E
SelectedClock
SRL16
EmulatedBitOut
DCMClock
CLK
DataAlignmentCntrl(0)
DataAlignmentCntrl(1)
DataAlignmentCntrl(2)
DataAlignmentCntrl(3)
A0
A1
A2
A3
SRL16
FineAlignCLK
DataAlignmentCntrl(4)
DataAlignmentCntrl(5)
DataAlignmentCntrl(6)
DataAlignmentCntrl(7)
BUFG
DlydEmulatedBitOut
M2_1
SelectedClock
ClockControl(4)
ClockControl(0)
BUFG
ClockIN
XILINX
Title: PMC top level. Clock Selection, Data Generation and Emulation.
Name: Bradley Hall - SSR Test Chip
Date: March 4, 2003
Sheet 4 of 10

SAMTEC A



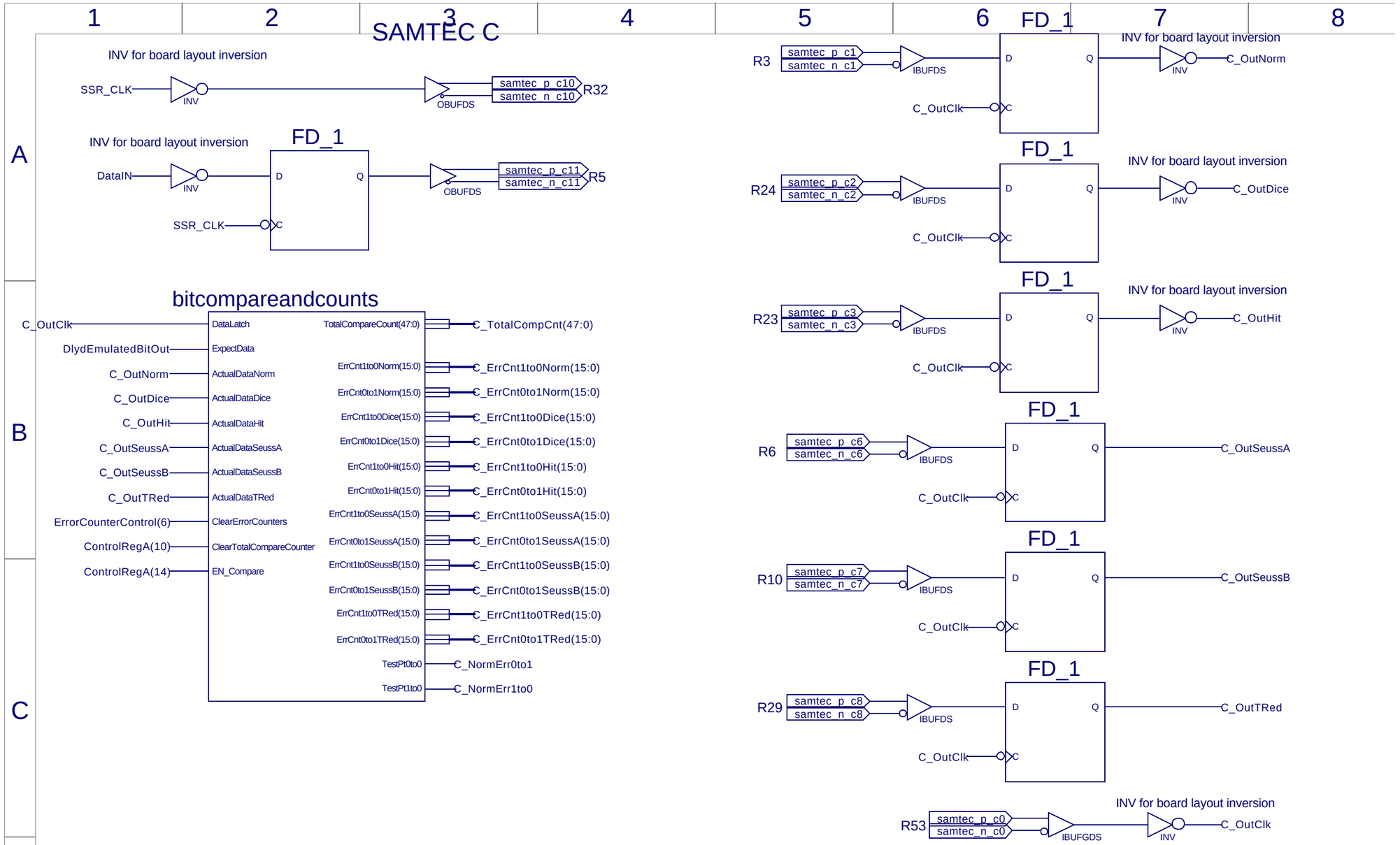
Title:	PMC top level. SSR A interface.
Name:	Bradley Hall - SSR Test Chip
Date:	March 4, 2003
Sheet	5 of 10

SAMTEC B

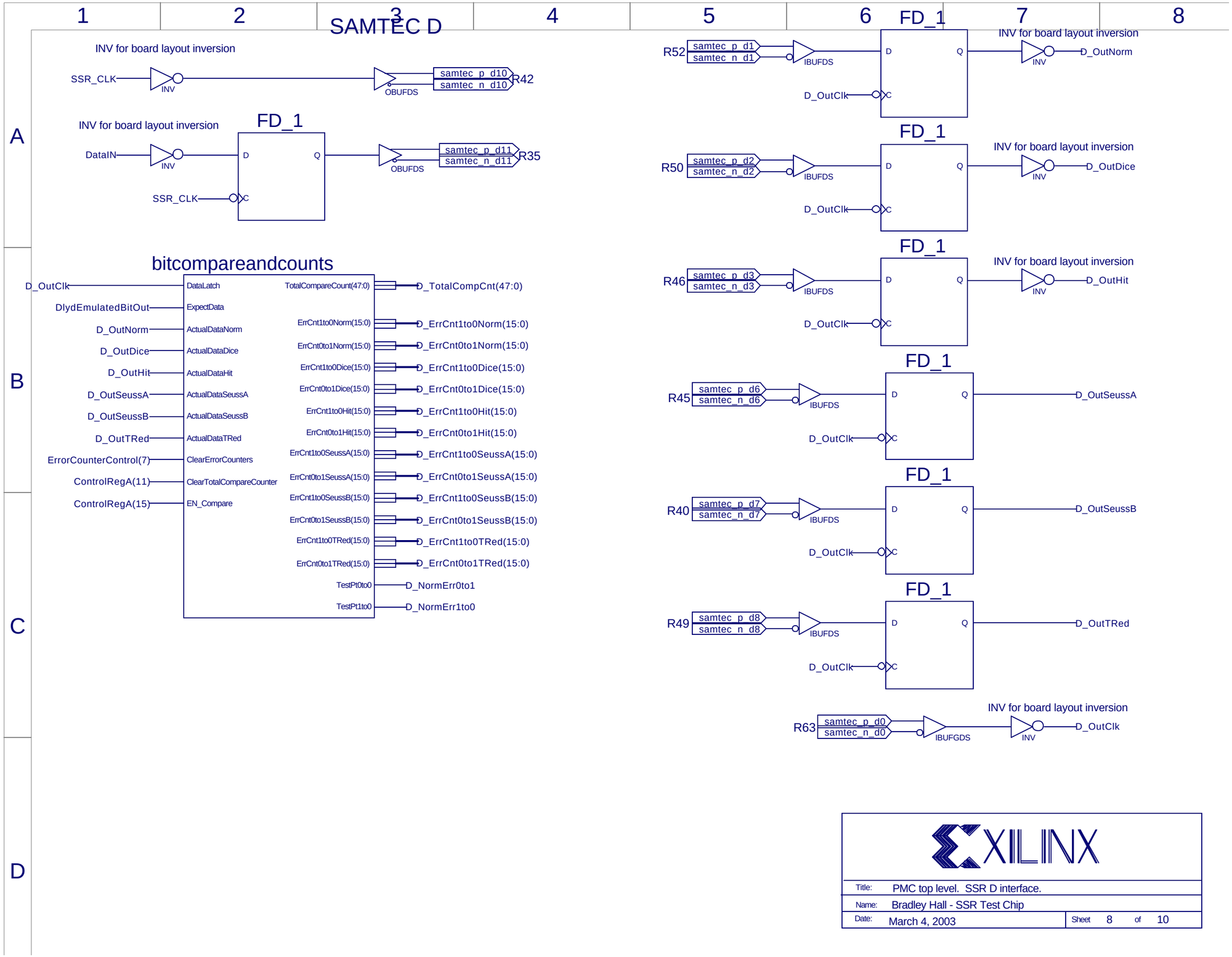


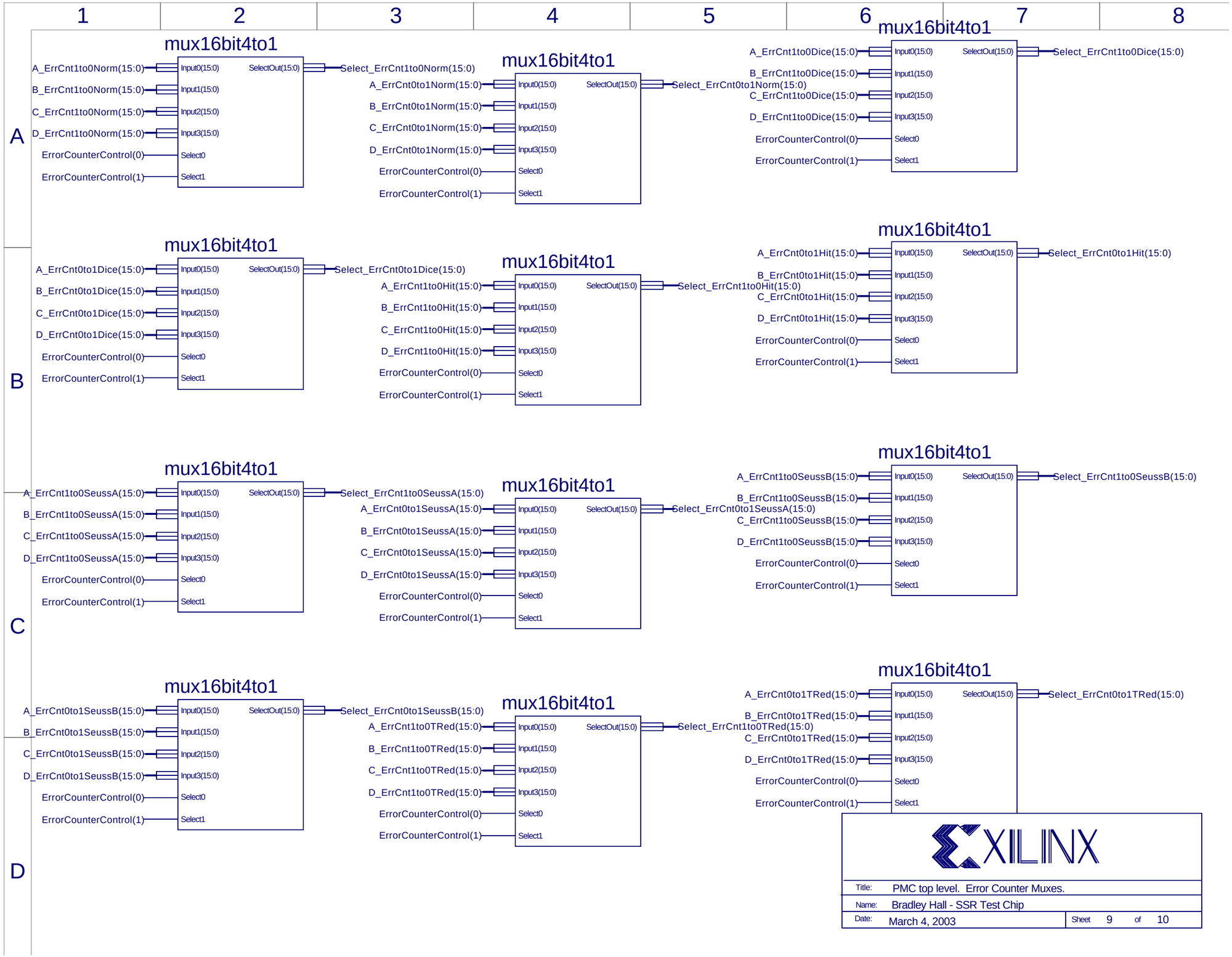
Title:	PMC top level. SSR B interface.
Name:	Bradley Hall - SSR Test Chip
Date:	March 4, 2003
Sheet	6 of 10

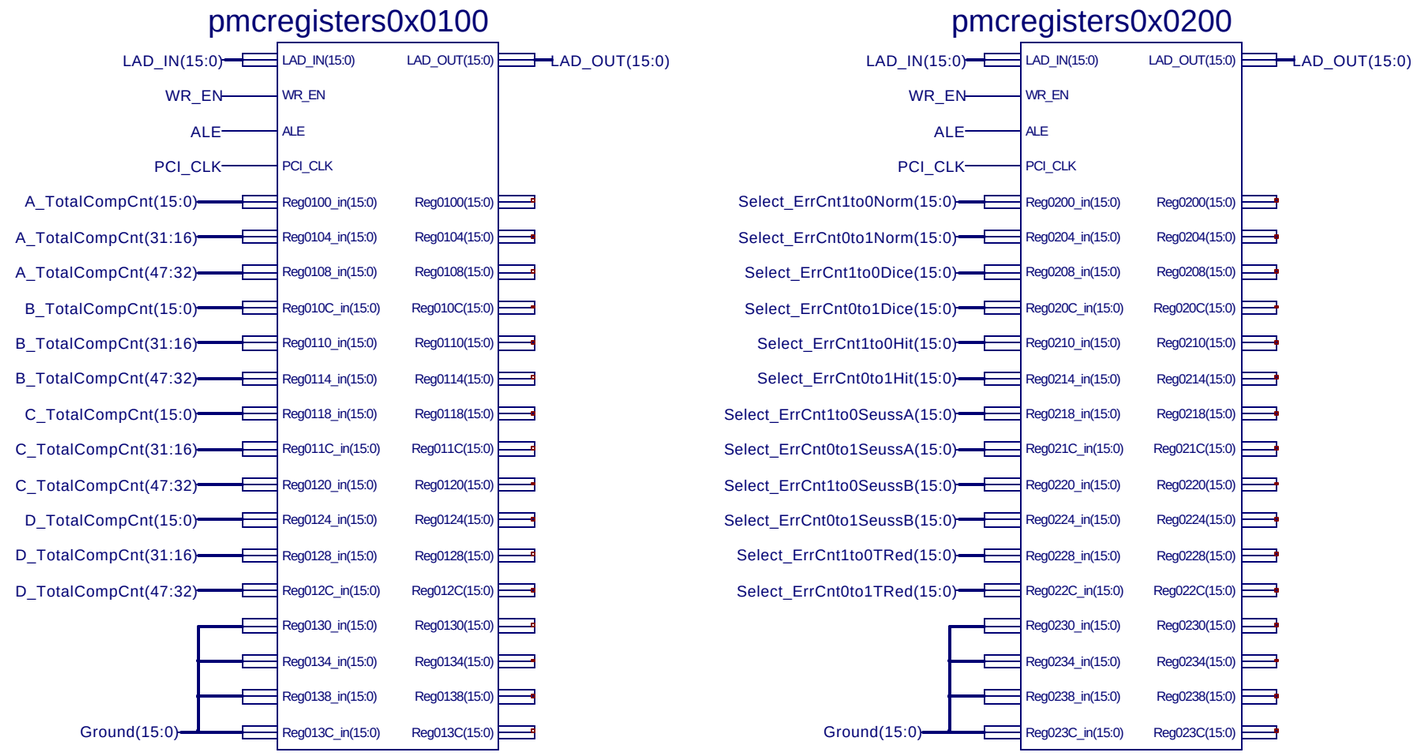
SAMTEC C



Title:	PMC top level. SSR C interface.
Name:	Bradley Hall - SSR Test Chip
Date:	March 4, 2003
Sheet	7 of 10


SAMTEC D
INV for board layout inversion
SSR_CLK
INV
OBUFDS
samtec_p_d10
samtec_n_d10
R42
INV for board layout inversion
FD_1
DataIN
D
Q
C
SSR_CLK
samtec_p_d11
samtec_n_d11
R35
bitcompareandcounts
D_OutClk
DlydEmulatedBitOut
D_OutNorm
D_OutDice
D_OutHit
D_OutSeussA
D_OutSeussB
D_OutTRed
ErrorCounterControl(7)
ControlRegA(11)
ControlRegA(15)
DataLatch
ExpectData
ActualDataNorm
ActualDataDice
ActualDataHit
ActualDataSeussA
ActualDataSeussB
ActualDataTRed
ClearErrorCounters
ClearTotalCompareCounter
EN_Compare
TotalCompareCount(47:0)
ErrCnt1to0Norm(15:0)
ErrCnt0to1Norm(15:0)
ErrCnt1to0Dice(15:0)
ErrCnt0to1Dice(15:0)
ErrCnt1to0Hit(15:0)
ErrCnt0to1Hit(15:0)
ErrCnt1to0SeussA(15:0)
ErrCnt0to1SeussA(15:0)
ErrCnt1to0SeussB(15:0)
ErrCnt0to1SeussB(15:0)
ErrCnt1to0TRed(15:0)
ErrCnt0to1TRed(15:0)
TestPt0to0
TestPt1to0
D_TotalCompCnt(47:0)
D_ErrCnt1to0Norm(15:0)
D_ErrCnt0to1Norm(15:0)
D_ErrCnt1to0Dice(15:0)
D_ErrCnt0to1Dice(15:0)
D_ErrCnt1to0Hit(15:0)
D_ErrCnt0to1Hit(15:0)
D_ErrCnt1to0SeussA(15:0)
D_ErrCnt0to1SeussA(15:0)
D_ErrCnt1to0SeussB(15:0)
D_ErrCnt0to1SeussB(15:0)
D_ErrCnt1to0TRed(15:0)
D_ErrCnt0to1TRed(15:0)
D_NormErr0to1
D_NormErr1to0
R52
samtec_p_d1
samtec_n_d1
IBUFDS
D_OutNorm
R50
samtec_p_d2
samtec_n_d2
D_OutDice
R46
samtec_p_d3
samtec_n_d3
D_OutHit
R45
samtec_p_d6
samtec_n_d6
R40
samtec_p_d7
samtec_n_d7
R49
samtec_p_d8
samtec_n_d8
R63
samtec_p_d0
samtec_n_d0
IBUFGDS
D_OutClk
Title: PMC top level. SSR D interface.
Name: Bradley Hall - SSR Test Chip
Date: March 4, 2003
Sheet 8 of 10


1
2
3
4
5
6
7
8
A
B
C
D
mux16bit4to1
A_ErrCnt1to0Norm(15:0)
B_ErrCnt1to0Norm(15:0)
C_ErrCnt1to0Norm(15:0)
D_ErrCnt1to0Norm(15:0)
ErrorCounterControl(0)
ErrorCounterControl(1)
Input0(15:0)
Input1(15:0)
Input2(15:0)
Input3(15:0)
Select0
Select1
SelectOut(15:0)
Select_ErrCnt1to0Norm(15:0)
A_ErrCnt0to1Norm(15:0)
B_ErrCnt0to1Norm(15:0)
C_ErrCnt0to1Norm(15:0)
D_ErrCnt0to1Norm(15:0)
Select_ErrCnt0to1Norm(15:0)
A_ErrCnt1to0Dice(15:0)
B_ErrCnt1to0Dice(15:0)
C_ErrCnt1to0Dice(15:0)
D_ErrCnt1to0Dice(15:0)
Select_ErrCnt1to0Dice(15:0)
A_ErrCnt0to1Dice(15:0)
B_ErrCnt0to1Dice(15:0)
C_ErrCnt0to1Dice(15:0)
D_ErrCnt0to1Dice(15:0)
Select_ErrCnt0to1Dice(15:0)
A_ErrCnt1to0Hit(15:0)
B_ErrCnt1to0Hit(15:0)
C_ErrCnt1to0Hit(15:0)
D_ErrCnt1to0Hit(15:0)
Select_ErrCnt1to0Hit(15:0)
A_ErrCnt0to1Hit(15:0)
B_ErrCnt0to1Hit(15:0)
C_ErrCnt0to1Hit(15:0)
D_ErrCnt0to1Hit(15:0)
Select_ErrCnt0to1Hit(15:0)
A_ErrCnt1to0SeussA(15:0)
B_ErrCnt1to0SeussA(15:0)
C_ErrCnt1to0SeussA(15:0)
D_ErrCnt1to0SeussA(15:0)
Select_ErrCnt1to0SeussA(15:0)
A_ErrCnt0to1SeussA(15:0)
B_ErrCnt0to1SeussA(15:0)
C_ErrCnt0to1SeussA(15:0)
D_ErrCnt0to1SeussA(15:0)
Select_ErrCnt0to1SeussA(15:0)
A_ErrCnt1to0SeussB(15:0)
B_ErrCnt1to0SeussB(15:0)
C_ErrCnt1to0SeussB(15:0)
D_ErrCnt1to0SeussB(15:0)
Select_ErrCnt1to0SeussB(15:0)
A_ErrCnt0to1SeussB(15:0)
B_ErrCnt0to1SeussB(15:0)
C_ErrCnt0to1SeussB(15:0)
D_ErrCnt0to1SeussB(15:0)
Select_ErrCnt0to1SeussB(15:0)
A_ErrCnt1to0TRed(15:0)
B_ErrCnt1to0TRed(15:0)
C_ErrCnt1to0TRed(15:0)
D_ErrCnt1to0TRed(15:0)
Select_ErrCnt1to0TRed(15:0)
A_ErrCnt0to1TRed(15:0)
B_ErrCnt0to1TRed(15:0)
C_ErrCnt0to1TRed(15:0)
D_ErrCnt0to1TRed(15:0)
Select_ErrCnt0to1TRed(15:0)
XILINX
Title: PMC top level. Error Counter Muxes.
Name: Bradley Hall - SSR Test Chip
Date: March 4, 2003
Sheet 9 of 10



XILINX

Title:	PMC top level. Read-Only Registers.
Name:	Bradley Hall - SSR Test Chip
Date:	March 4, 2003
Sheet	10 of 10