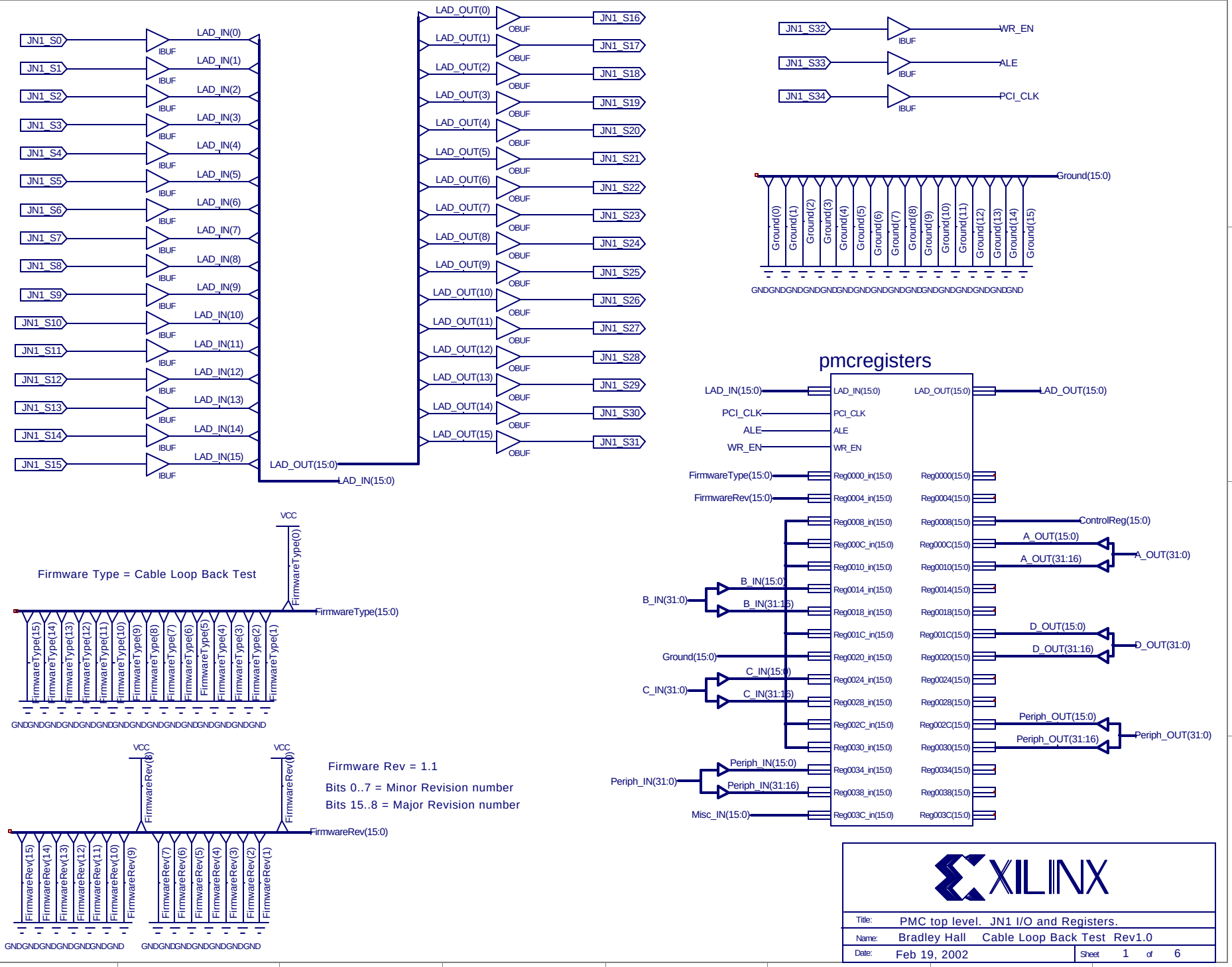
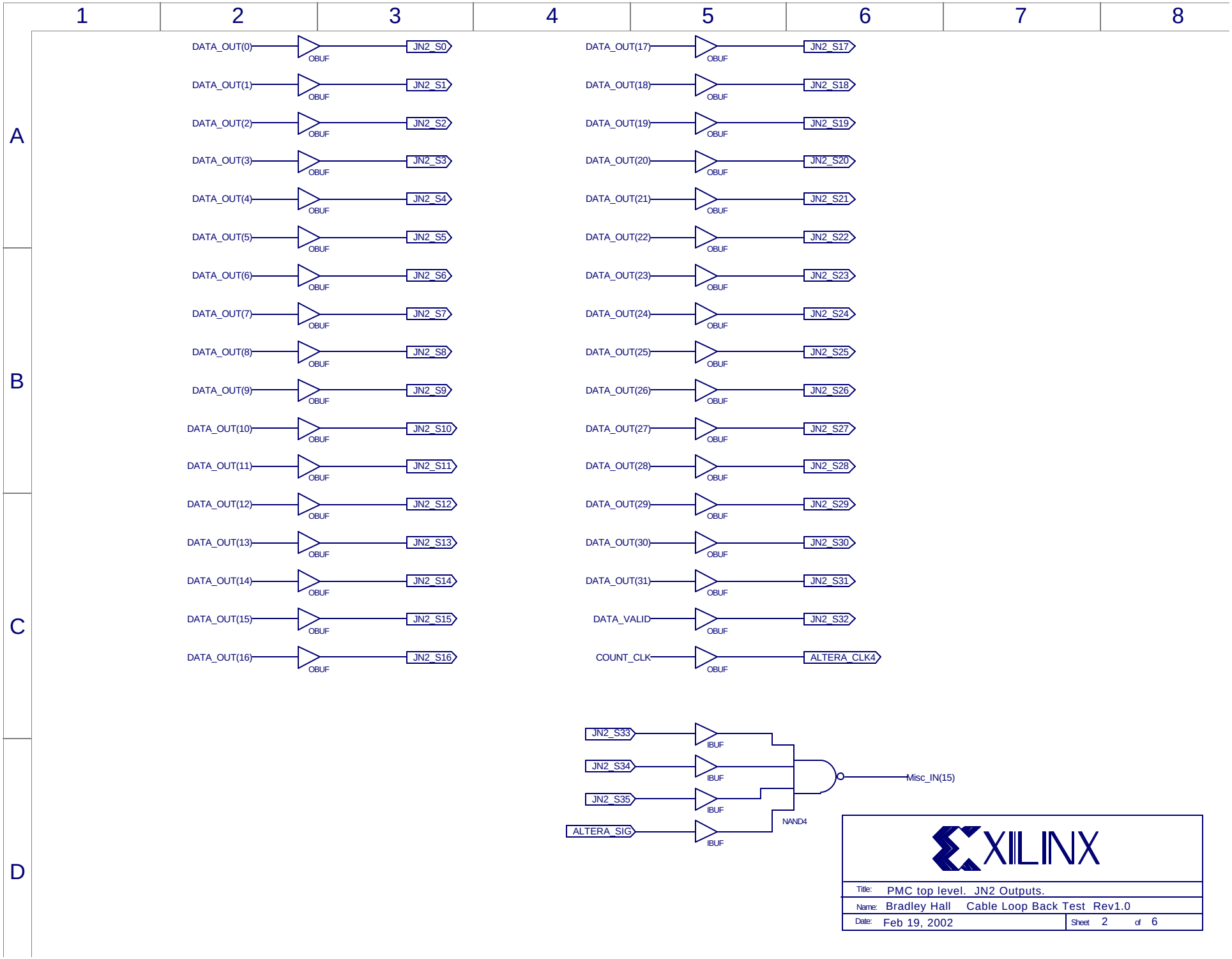
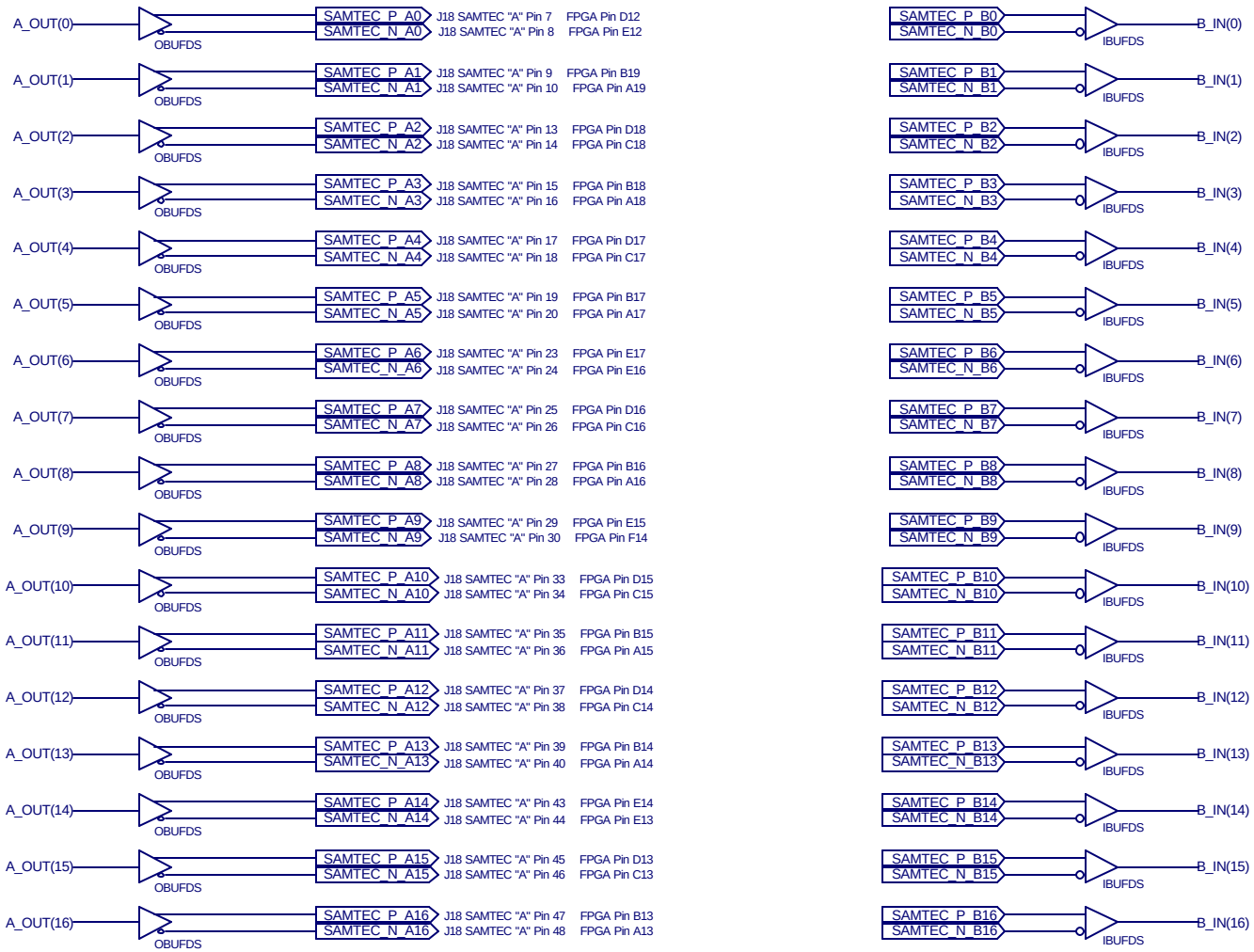
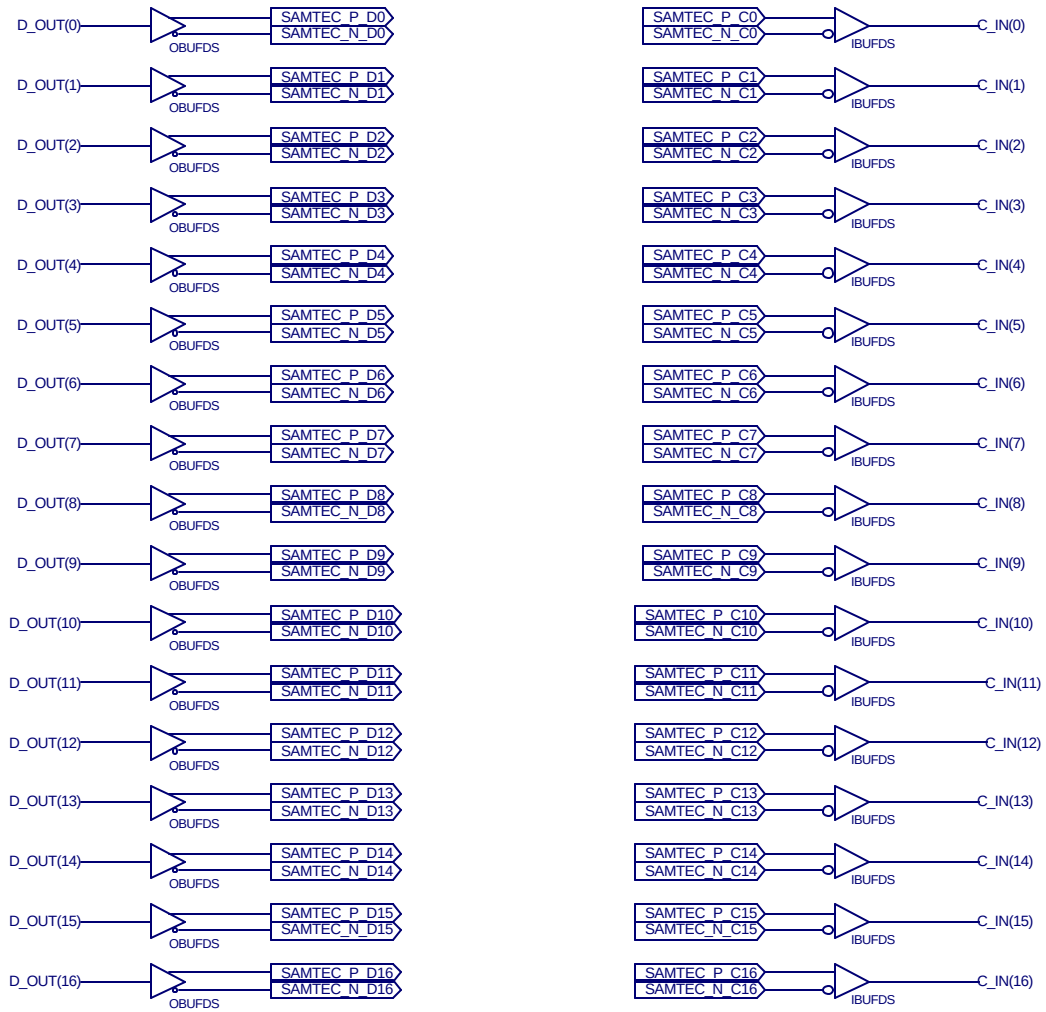

JN1_S0
JN1_S1
JN1_S2
JN1_S3
JN1_S4
JN1_S5
JN1_S6
JN1_S7
JN1_S8
JN1_S9
JN1_S10
JN1_S11
JN1_S12
JN1_S13
JN1_S14
JN1_S15
IBUF
LAD_IN(0)
LAD_IN(1)
LAD_IN(2)
LAD_IN(3)
LAD_IN(4)
LAD_IN(5)
LAD_IN(6)
LAD_IN(7)
LAD_IN(8)
LAD_IN(9)
LAD_IN(10)
LAD_IN(11)
LAD_IN(12)
LAD_IN(13)
LAD_IN(14)
LAD_IN(15)
LAD_OUT(15:0)
LAD_IN(15:0)
LAD_OUT(0)
LAD_OUT(1)
LAD_OUT(2)
LAD_OUT(3)
LAD_OUT(4)
LAD_OUT(5)
LAD_OUT(6)
LAD_OUT(7)
LAD_OUT(8)
LAD_OUT(9)
LAD_OUT(10)
LAD_OUT(11)
LAD_OUT(12)
LAD_OUT(13)
LAD_OUT(14)
LAD_OUT(15)
OBUF
JN1_S16
JN1_S17
JN1_S18
JN1_S19
JN1_S20
JN1_S21
JN1_S22
JN1_S23
JN1_S24
JN1_S25
JN1_S26
JN1_S27
JN1_S28
JN1_S29
JN1_S30
JN1_S31
JN1_S32
JN1_S33
JN1_S34
WR_EN
ALE
PCI_CLK
Ground(15:0)
Ground(0)
Ground(1)
Ground(2)
Ground(3)
Ground(4)
Ground(5)
Ground(6)
Ground(7)
Ground(8)
Ground(9)
Ground(10)
Ground(11)
Ground(12)
Ground(13)
Ground(14)
Ground(15)
GND
pmcregisters
LAD_IN(15:0)
PCI_CLK
ALE
WR_EN
FirmwareType(15:0)
FirmwareRev(15:0)
Reg0000_in(15:0)
Reg0004_in(15:0)
Reg0008_in(15:0)
Reg000C_in(15:0)
Reg0010_in(15:0)
Reg0014_in(15:0)
Reg0018_in(15:0)
Reg001C_in(15:0)
Reg0020_in(15:0)
Reg0024_in(15:0)
Reg0028_in(15:0)
Reg002C_in(15:0)
Reg0030_in(15:0)
Reg0034_in(15:0)
Reg0038_in(15:0)
Reg003C_in(15:0)
Reg0000(15:0)
Reg0004(15:0)
Reg0008(15:0)
Reg000C(15:0)
Reg0010(15:0)
Reg0014(15:0)
Reg0018(15:0)
Reg001C(15:0)
Reg0020(15:0)
Reg0024(15:0)
Reg0028(15:0)
Reg002C(15:0)
Reg0030(15:0)
Reg0034(15:0)
Reg0038(15:0)
Reg003C(15:0)
LAD_OUT(15:0)
ControlReg(15:0)
A_OUT(15:0)
A_OUT(31:16)
A_OUT(31:0)
B_IN(15:0)
B_IN(31:16)
B_IN(31:0)
D_OUT(15:0)
D_OUT(31:16)
D_OUT(31:0)
Ground(15:0)
C_IN(15:0)
C_IN(31:16)
C_IN(31:0)
Periph_OUT(15:0)
Periph_OUT(31:16)
Periph_OUT(31:0)
Periph_IN(15:0)
Periph_IN(31:16)
Periph_IN(31:0)
Misc_IN(15:0)
VCC
FirmwareType(0)
FirmwareType(15:0)
Firmware Type = Cable Loop Back Test
FirmwareRev(8)
FirmwareRev(0)
FirmwareRev(15:0)
Firmware Rev = 1.1
Bits 0..7 = Minor Revision number
Bits 15..8 = Major Revision number
XILINX
Title: PMC top level. JN1 I/O and Registers.
Name: Bradley Hall Cable Loop Back Test Rev1.0
Date: Feb 19, 2002
Sheet 1 of 6


DATA_OUT(0) OBUF JN2_S0
DATA_OUT(1) OBUF JN2_S1
DATA_OUT(2) OBUF JN2_S2
DATA_OUT(3) OBUF JN2_S3
DATA_OUT(4) OBUF JN2_S4
DATA_OUT(5) OBUF JN2_S5
DATA_OUT(6) OBUF JN2_S6
DATA_OUT(7) OBUF JN2_S7
DATA_OUT(8) OBUF JN2_S8
DATA_OUT(9) OBUF JN2_S9
DATA_OUT(10) OBUF JN2_S10
DATA_OUT(11) OBUF JN2_S11
DATA_OUT(12) OBUF JN2_S12
DATA_OUT(13) OBUF JN2_S13
DATA_OUT(14) OBUF JN2_S14
DATA_OUT(15) OBUF JN2_S15
DATA_OUT(16) OBUF JN2_S16
DATA_OUT(17) OBUF JN2_S17
DATA_OUT(18) OBUF JN2_S18
DATA_OUT(19) OBUF JN2_S19
DATA_OUT(20) OBUF JN2_S20
DATA_OUT(21) OBUF JN2_S21
DATA_OUT(22) OBUF JN2_S22
DATA_OUT(23) OBUF JN2_S23
DATA_OUT(24) OBUF JN2_S24
DATA_OUT(25) OBUF JN2_S25
DATA_OUT(26) OBUF JN2_S26
DATA_OUT(27) OBUF JN2_S27
DATA_OUT(28) OBUF JN2_S28
DATA_OUT(29) OBUF JN2_S29
DATA_OUT(30) OBUF JN2_S30
DATA_OUT(31) OBUF JN2_S31
DATA_VALID OBUF JN2_S32
COUNT_CLK OBUF ALTERA_CLK4
JN2_S33 IBUF
JN2_S34 IBUF
JN2_S35 IBUF
ALTERA_SIG IBUF
NAND4
Misc_IN(15)
XILINX
Title: PMC top level. JN2 Outputs.
Name: Bradley Hall Cable Loop Back Test Rev1.0
Date: Feb 19, 2002
Sheet 2 of 6



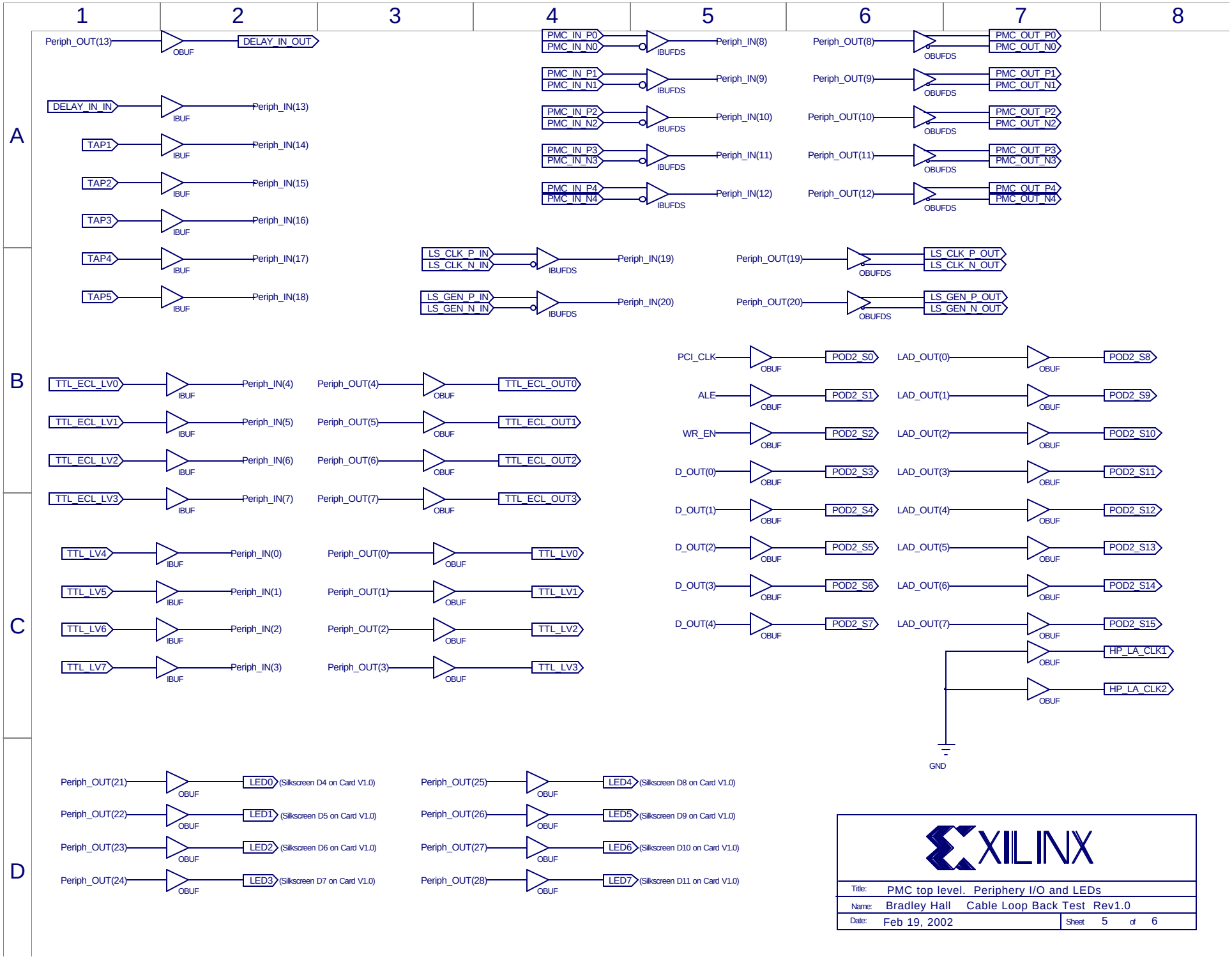
XILINX

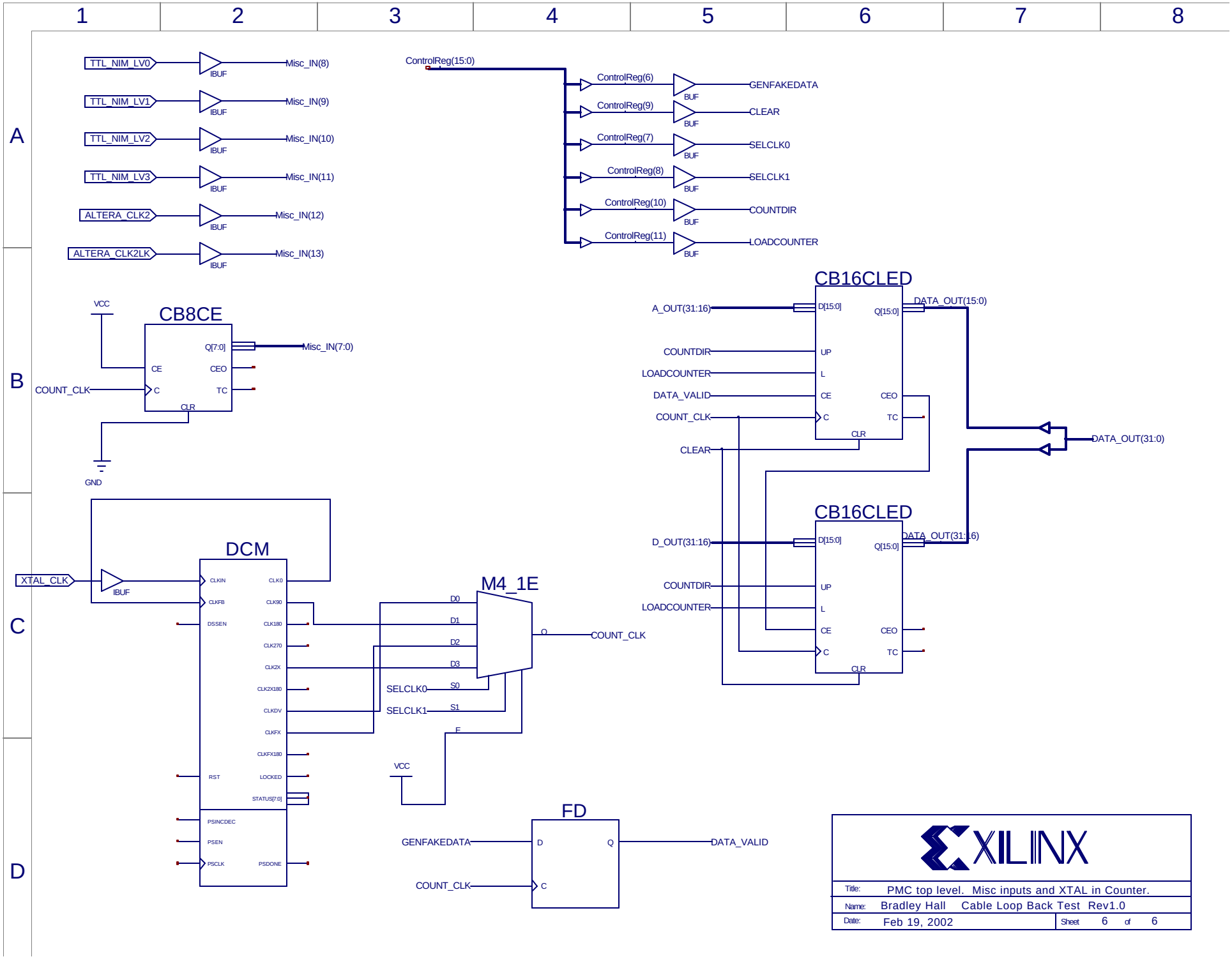
Title:	PMC top level. Samtec A and Samtec B I/O.
Name:	Bradley Hall Cable Loop Back Test Rev1.0
Date:	Feb 19, 2002
Sheet	3 of 6



XILINX

Title:	PMC top level. Samtec C and Samtec D I/O.
Name:	Bradley Hall Cable Loop Back Test Rev1.0
Date:	Feb 19, 2002
Sheet	4 of 6


1
2
3
4
5
6
7
8
A
B
C
D
Periph_OUT(13)
OBUF
DELAY_IN_OUT
DELAY_IN_IN
IBUF
Periph_IN(13)
TAP1
Periph_IN(14)
TAP2
Periph_IN(15)
TAP3
Periph_IN(16)
TAP4
Periph_IN(17)
TAP5
Periph_IN(18)
PMC_IN_P0
PMC_IN_N0
IBUFDS
Periph_IN(8)
PMC_IN_P1
PMC_IN_N1
Periph_IN(9)
PMC_IN_P2
PMC_IN_N2
Periph_IN(10)
PMC_IN_P3
PMC_IN_N3
Periph_IN(11)
PMC_IN_P4
PMC_IN_N4
Periph_IN(12)
Periph_OUT(8)
OBUFDS
PMC_OUT_P0
PMC_OUT_N0
Periph_OUT(9)
PMC_OUT_P1
PMC_OUT_N1
Periph_OUT(10)
PMC_OUT_P2
PMC_OUT_N2
Periph_OUT(11)
PMC_OUT_P3
PMC_OUT_N3
Periph_OUT(12)
PMC_OUT_P4
PMC_OUT_N4
LS_CLK_P_IN
LS_CLK_N_IN
Periph_IN(19)
LS_GEN_P_IN
LS_GEN_N_IN
Periph_IN(20)
Periph_OUT(19)
LS_CLK_P_OUT
LS_CLK_N_OUT
Periph_OUT(20)
LS_GEN_P_OUT
LS_GEN_N_OUT
TTL_ECL_LV0
Periph_IN(4)
TTL_ECL_LV1
Periph_IN(5)
TTL_ECL_LV2
Periph_IN(6)
TTL_ECL_LV3
Periph_IN(7)
Periph_OUT(4)
TTL_ECL_OUT0
Periph_OUT(5)
TTL_ECL_OUT1
Periph_OUT(6)
TTL_ECL_OUT2
Periph_OUT(7)
TTL_ECL_OUT3
TTL_LV4
Periph_IN(0)
TTL_LV5
Periph_IN(1)
TTL_LV6
Periph_IN(2)
TTL_LV7
Periph_IN(3)
Periph_OUT(0)
TTL_LV0
Periph_OUT(1)
TTL_LV1
Periph_OUT(2)
TTL_LV2
Periph_OUT(3)
TTL_LV3
PCI_CLK
POD2_S0
ALE
POD2_S1
WR_EN
POD2_S2
D_OUT(0)
POD2_S3
D_OUT(1)
POD2_S4
D_OUT(2)
POD2_S5
D_OUT(3)
POD2_S6
D_OUT(4)
POD2_S7
LAD_OUT(0)
POD2_S8
LAD_OUT(1)
POD2_S9
LAD_OUT(2)
POD2_S10
LAD_OUT(3)
POD2_S11
LAD_OUT(4)
POD2_S12
LAD_OUT(5)
POD2_S13
LAD_OUT(6)
POD2_S14
LAD_OUT(7)
POD2_S15
HP_LA_CLK1
HP_LA_CLK2
GND
Periph_OUT(21)
LED0
(Silkscreen D4 on Card V1.0)
Periph_OUT(22)
LED1
(Silkscreen D5 on Card V1.0)
Periph_OUT(23)
LED2
(Silkscreen D6 on Card V1.0)
Periph_OUT(24)
LED3
(Silkscreen D7 on Card V1.0)
Periph_OUT(25)
LED4
(Silkscreen D8 on Card V1.0)
Periph_OUT(26)
LED5
(Silkscreen D9 on Card V1.0)
Periph_OUT(27)
LED6
(Silkscreen D10 on Card V1.0)
Periph_OUT(28)
LED7
(Silkscreen D11 on Card V1.0)
XILINX
Title: PMC top level. Periphery I/O and LEDs
Name: Bradley Hall Cable Loop Back Test Rev1.0
Date: Feb 19, 2002
Sheet 5 of 6


TTL_NIM_LV0
IBUF
Misc_IN(8)
TTL_NIM_LV1
IBUF
Misc_IN(9)
TTL_NIM_LV2
IBUF
Misc_IN(10)
TTL_NIM_LV3
IBUF
Misc_IN(11)
ALTERA_CLK2
IBUF
Misc_IN(12)
ALTERA_CLK2LK
IBUF
Misc_IN(13)
ControlReg(15:0)
ControlReg(6)
BUF
GENFAKEDATA
ControlReg(9)
BUF
CLEAR
ControlReg(7)
BUF
SELCLK0
ControlReg(8)
BUF
SELCLK1
ControlReg(10)
BUF
COUNTDIR
ControlReg(11)
BUF
LOADCOUNTER
VCC
CB8CE
Q[7:0]
Misc_IN(7:0)
CE
CEO
COUNT_CLK
C
TC
CLR
GND
CB16CLED
A_OUT(31:16)
D[15:0]
Q[15:0]
DATA_OUT(15:0)
COUNTDIR
UP
LOADCOUNTER
L
DATA_VALID
CE
CEO
COUNT_CLK
C
TC
CLR
CLEAR
DATA_OUT(31:0)
CB16CLED
D_OUT(31:16)
D[15:0]
Q[15:0]
DATA_OUT(31:16)
COUNTDIR
UP
LOADCOUNTER
L
CE
CEO
C
TC
CLR
DCM
XTAL_CLK
IBUF
CLKIN
CLKFB
DSSEN
CLK0
CLK90
CLK180
CLK270
CLK2X
CLK2X180
CLKDV
CLKFX
CLKFX180
RST
LOCKED
STATUS[7:0]
PSINCDEC
PSEN
PSCLK
PSDONE
M4_1E
D0
D1
D2
D3
O
COUNT_CLK
SELCLK0
S0
SELCLK1
S1
E
VCC
FD
GENFAKEDATA
D
Q
DATA_VALID
COUNT_CLK
C
XILINX
Title: PMC top level. Misc inputs and XTAL in Counter.
Name: Bradley Hall Cable Loop Back Test Rev1.0
Date: Feb 19, 2002
Sheet 6 of 6