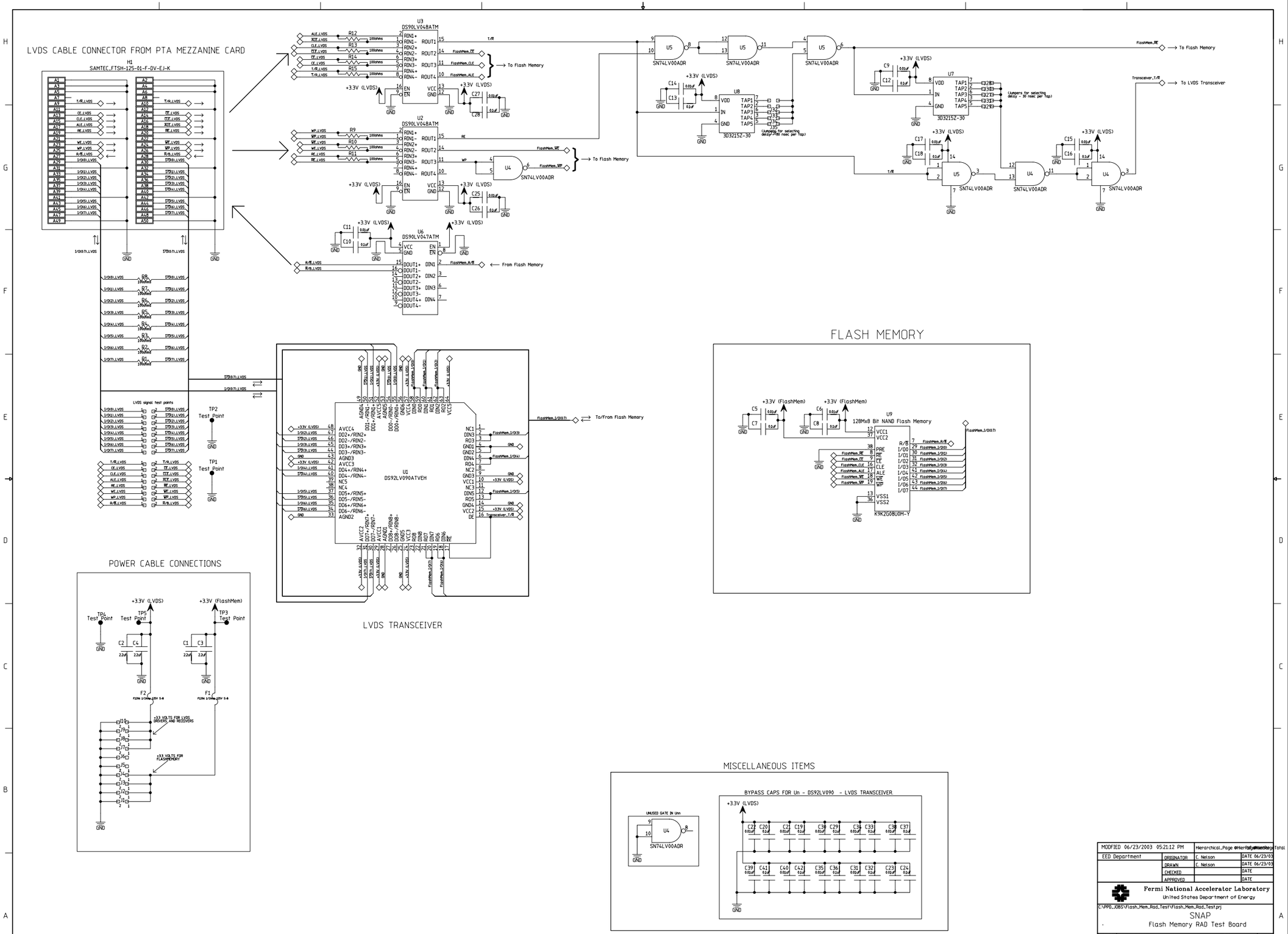
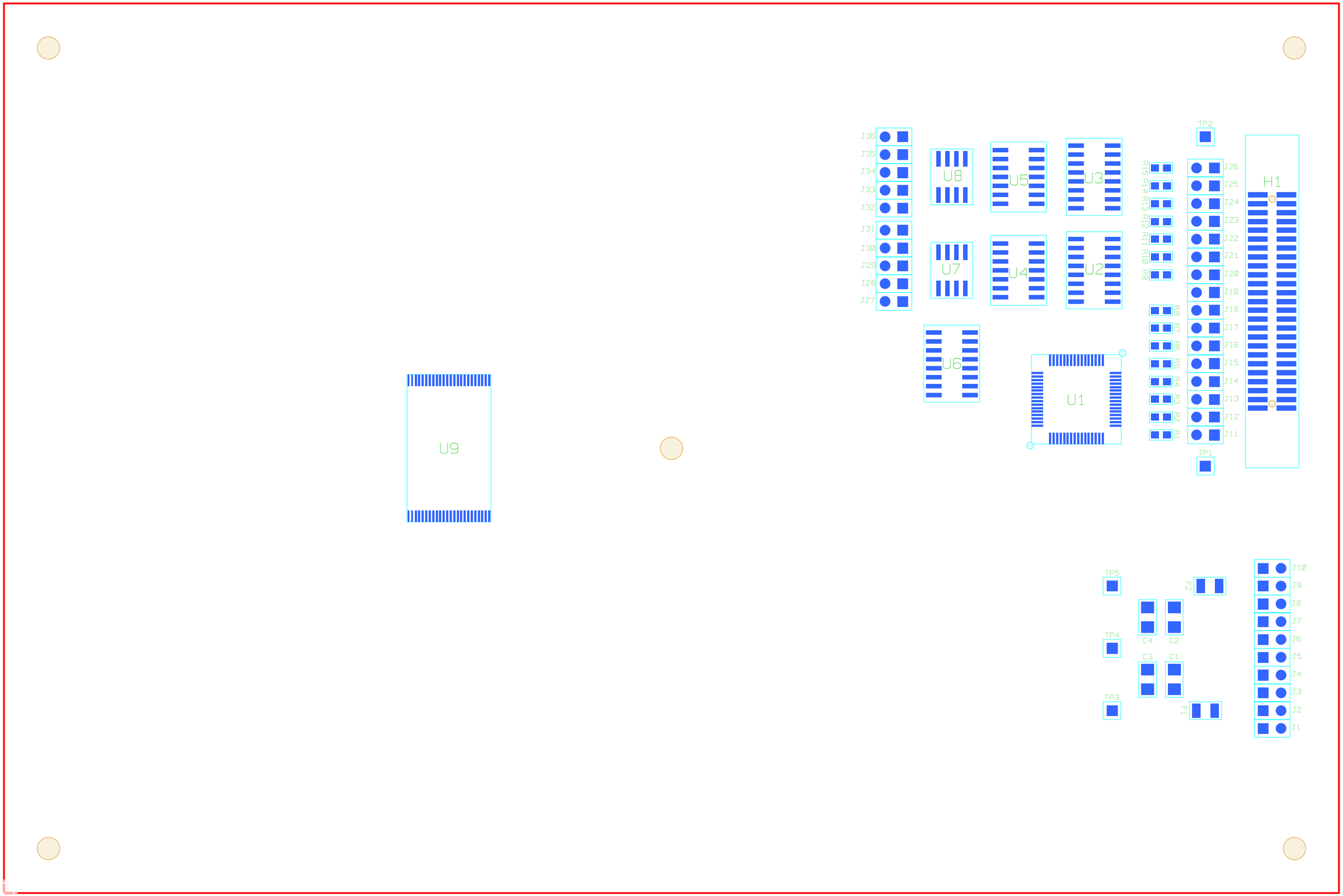
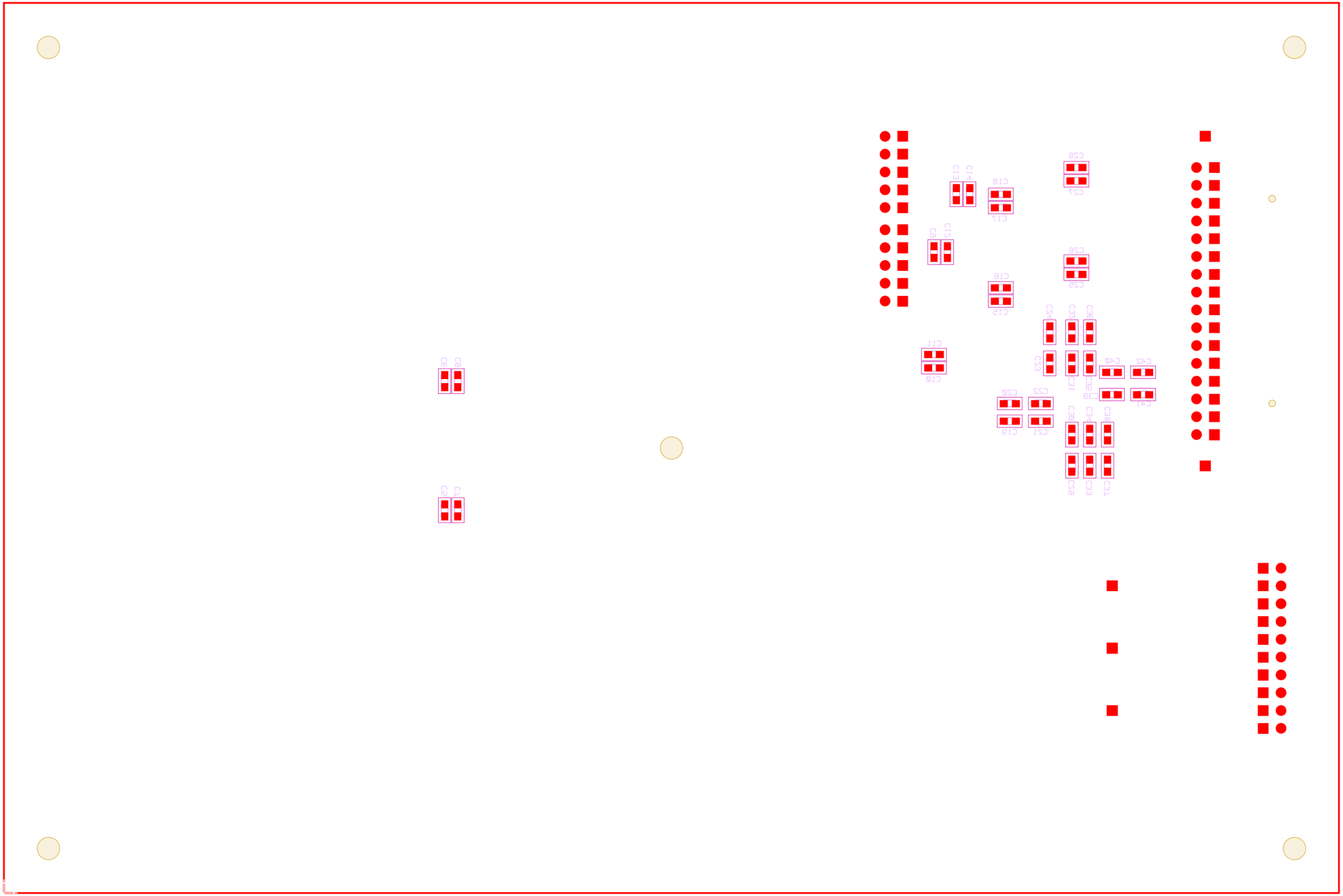

LVDS CABLE CONNECTOR FROM PTA MEZZANINE CARD
H1
SAMTEC_FTSH-125-01-F-DV-EJ-K
U3
DS90LV048ATM
U2
DS90LV048ATM
U6
DS90LV047ATM
U5
SN74LV00ADR
U4
SN74LV00ADR
U8
3D3215Z-30
U7
3D3215Z-30
(Jumpers for selecting delay - 30 nsec per tap)
To Flash Memory
From Flash Memory
To LVDS Transceiver
+3.3V (LVDS)
LVDS signal test points
TP2
Test Point
TP1
Test Point
U1
DS92LV090ATVEH
To/From Flash Memory
LVDS TRANSCEIVER
FLASH MEMORY
U9
128Mx8 Bit NAND Flash Memory
K9K2G08U0M-Y
+3.3V (FlashMem)
POWER CABLE CONNECTIONS
TP4
Test Point
TP5
Test Point
TP3
Test Point
F2
F1
+3.3 VOLTS FOR LVDS DRIVERS AND RECEIVERS
+3.3 VOLTS FOR FLASHMEMORY
MISCELLANEOUS ITEMS
UNUSED GATE IN Un
BYPASS CAPS FOR Un - DS92LV090 - LVDS TRANSCEIVER.
MODIFIED 06/23/2003 05:21:12 PM
EED Department
ORIGINATOR C. Nelson DATE 06/23/03
DRAWN C. Nelson DATE 06/23/03
CHECKED DATE
APPROVED DATE
Fermi National Accelerator Laboratory
United States Department of Energy
C:\PPD_JOBS\Flash_Mem_Rad_Test\Flash_Mem_Rad_Test.prj
SNAP
Flash Memory RAD Test Board
SIZE E
DRAWING NUMBER XXXXX
Schematic Page 01 of 01
REV A


J36
J35
J34
J33
J32
J31
J30
J29
J28
J27
U8
U5
U3
U7
U4
U2
U6
U1
U9
TP2
TP1
R15 R14 R13 R12 R11 R10 R9
R8 R7 R6 R5 R4 R3 R2 R1
J26
J25
J24
J23
J22
J21
J20
J19
J18
J17
J16
J15
J14
J13
J12
J11
H1
TP5
TP4
TP3
F2
F1
C4
C2
C3
C1
J10
J9
J8
J7
J6
J5
J4
J3
J2
J1


C1
C2
C3
C4
C5
C6
C7
C8
C9
C10
C11
C12
C13
C14
C15
C16
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C41
C42