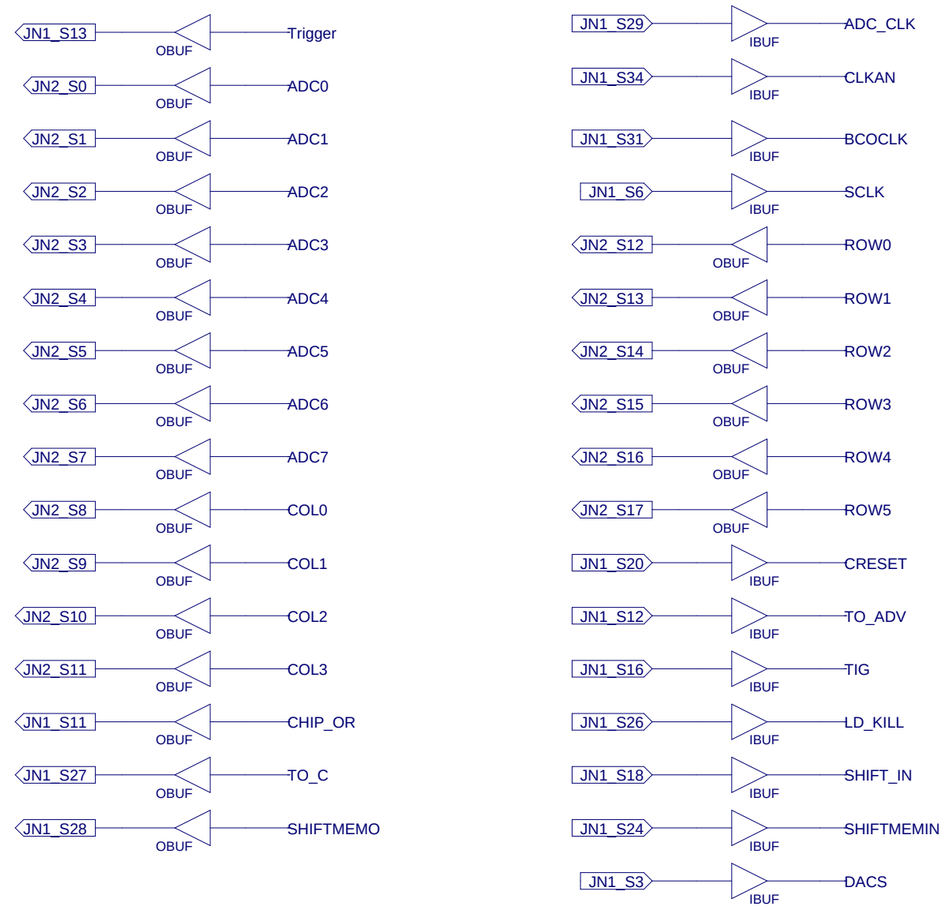
JN1/JN2 (PTA/PMC) Interface Inputs and Outputs



XILINX

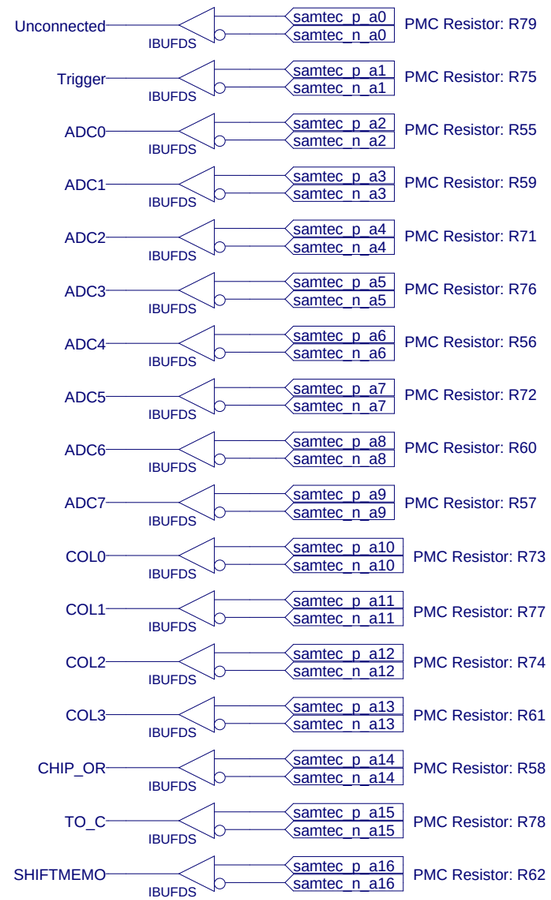
Title: SW Passthru to Test Beam '02 FPIX0 Inner Board. Rev 1.0

Name: Bradley Hall. JN1/JN2 signals.

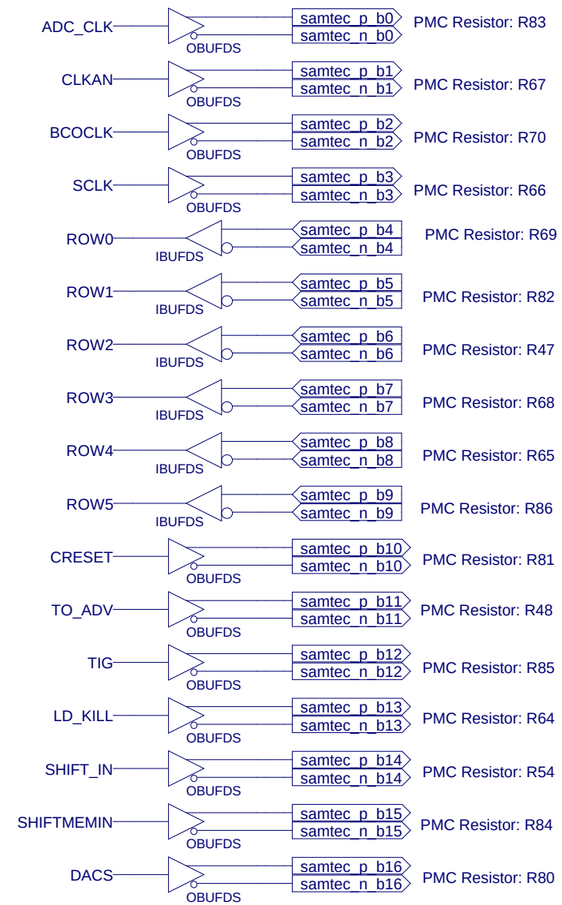
Date: August 15, 2002

Sheet 1 of 3

SAMTEC A LVDS Inputs



SAMTEC B LVDS Inputs and Outputs

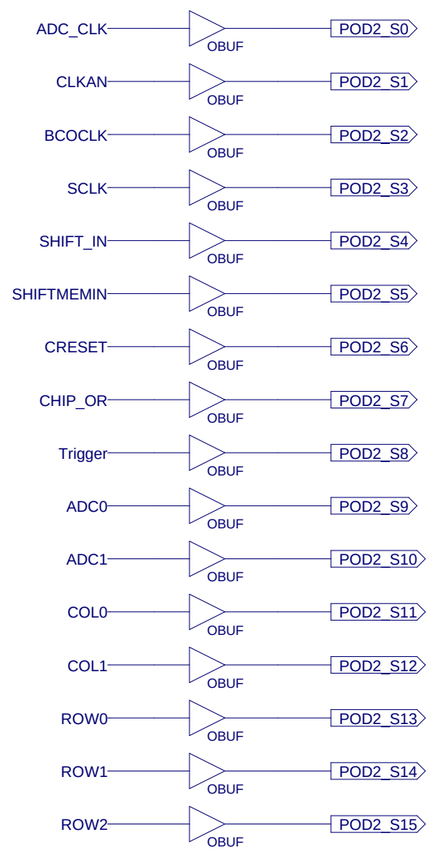


PMC Resistors are for LVDS termination. Only the LVDS Inputs should have their PMC resistor populated.

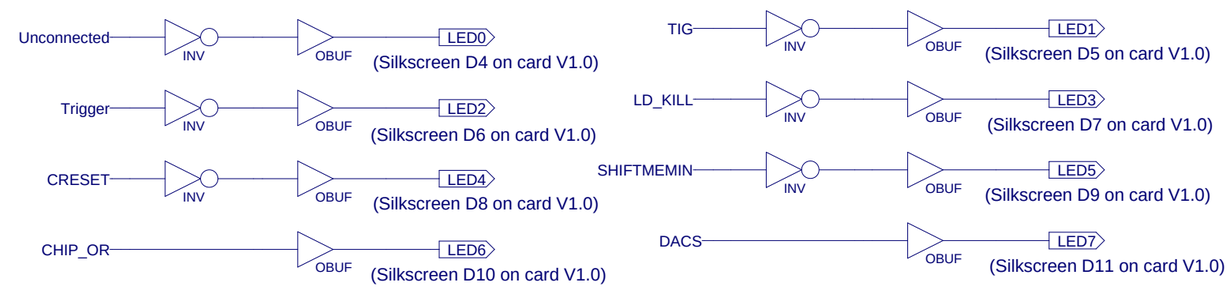
Note that PMC Document signal Name GPIO_A1_N_CLK is samtec_n_a0,
GPIO_A2_N is samtec_n_a1, and so on.

Title:	SW Passthru to Test Beam '02 FPIX0 Inner Board. Rev 1.0
Name:	Bradley Hall. LVDS I/O on SAMTEC A and B.
Date:	August 15, 2002 — Sheet 2 of 3

Logic Analyzer Header



LEDs



Signals 'CHIP_OR' and 'DACS' are active low.
LEDs will turn on when OBUF drive logic '0'.

Title:	SW Passthru to Test Beam '02 FPIX0 Inner Board. Rev 1.0
Name:	Bradley Hall. Debug Signals.
Date:	August 15, 2002
Sheet	3 of 3