

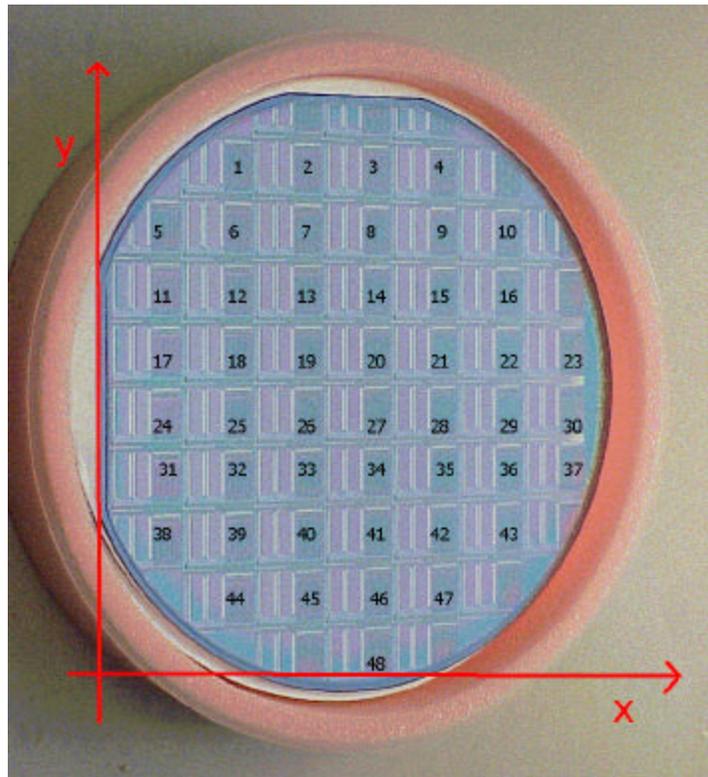
## FPIX1 Wafer Tests

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These notes briefly describe the tests done in three FPIX1 wafers with 48 chips each. This test was performed to identify good chips in the wafer. Once identified, the good chips can be diced and then bump bonded to sensors.

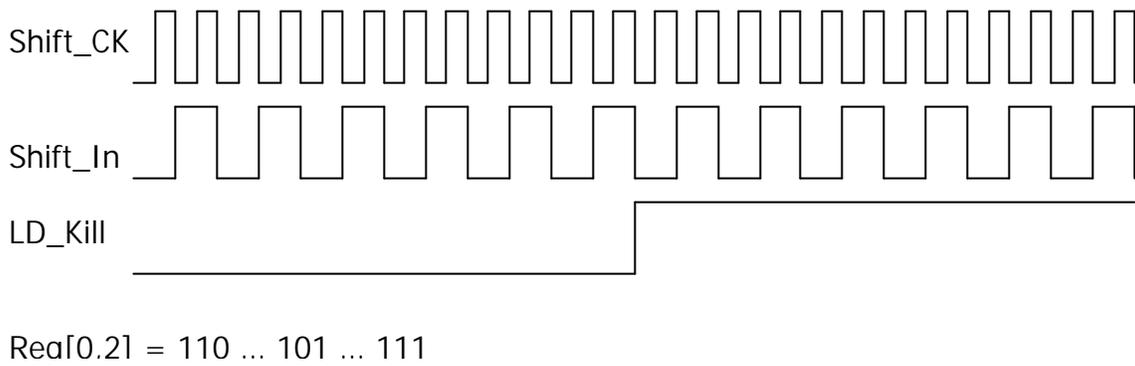
Figure 1 is a picture of the wafer tested. The numbers identify the chips under test.



**Figure 1**

The goal of this test is to determine if the digital block of the chips, basically composed of shift registers, is working. To do that we send initialization clocks to the chip (Shift\_Ck), while varying the shift path switching LD\_kill, Reg\_0, Reg\_1 and Reg\_2 signals.

Table 1, Table 2 and Table 3 show the values of Ivddd (the current in the digital voltage power supply) and Ivdda (the current in the analog power supply) for each one of the tested chips. Please refer to Figure 1 for a correlation between the current values and the geographic localization of the chip in the wafer.



**Figure 2**

<b>Ivddd[mA]</b>	61	23	18	35		
276	60	29	12	61	154	
18	17	15	10	10	12	
10	38	21	69	74	6	350
23	15	36	10	13	16	500
16	16	10	15	10	10	337
123	10	10	19	16	10	
	10	12	12	22		
			368			
<b>Ivdda[mA]</b>	1	1	4	1		
8	3	3	3	3	3	
2	3	3	4	3	1	
3	3	3	3	1	3	218
3	3	3	4	3	4	27
3	3	4	3	4	3	91
5	4	3	3	4	4	
	4	3	2	19		
			11			

**Table 1 – Wafer I currents**

<b>Ivddd[mA]</b>	30	50	37	29		
173	3	20	22	5	16	
31	17	16	20	25	130	
21	16	65	6	36	10	25
23	60	20	22	18	23	20
422	12	29	36	17	22	147
59	56	18	8	56	18	
	19	18	75	26		
			210			

<b>Ivdda[mA]</b>	2	4	3	4		
152	3	4	4	4	4	
4	3	3	3	3	191	
4	3	4	3	4	4	3
4	3	4	3	2	4	3
12	3	2	2	3	3	13
3	4	4	4	5	3	
	3	3	14	2		
			12			

**Table 2 – Wafer II currents**

<b>Ivddd[mA]</b>	108	79	18	18		
307	27	25	23	16	230	
18	10	18	18	29	20	
16	22	12	68	24	22	355
17	27	20	19	18	20	424
30	28	36	18	21	20	333
250	29	29	22	18	40	
	18	18	98	26		
			345			

<b>Ivdda[mA]</b>	1	3	3	4		
18	4	4	4	4	35	
3	3	4	4	5	4	
4	4	4	5	4	3	133
4	4	3	4	4	4	26
4	150	4	3	3	4	30
12	4	3	4	4	3	
	3	2	4	4		
			13			

**Table 3 – Wafer III currents**

A 3-D plot of the currents is shown in Figure 3. It can be verified that the non-working chips most of the time are localized in the periphery of the wafer, drawing a current that is much higher than the working ones. A color map identifying good and bad chips is also presented for completeness.

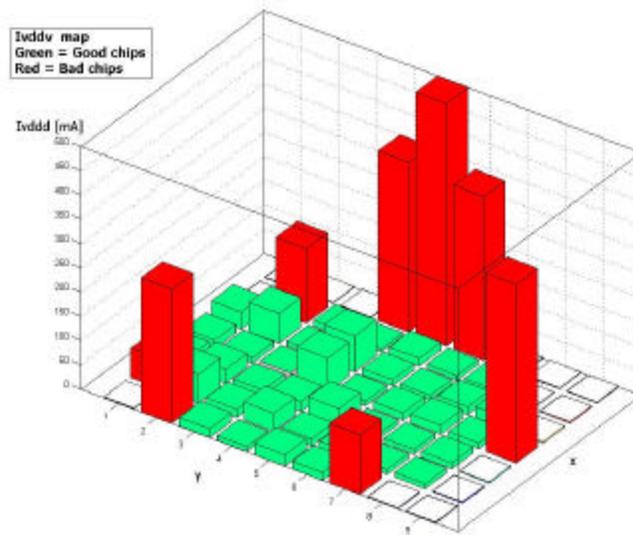


Figure 3

Ivdda map - Wafer 1  
 Green = Good chips  
 Red = Bad chips

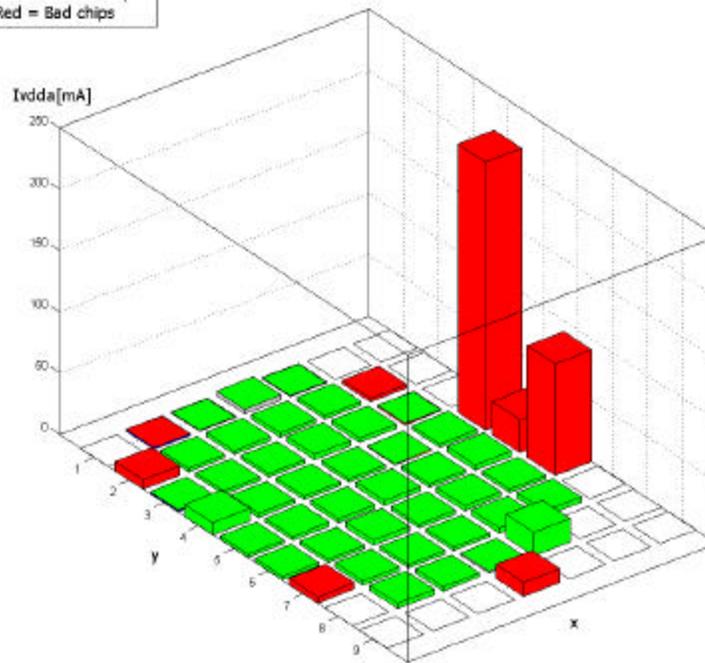


Figure 4

Wafer 1 - 48 FPX1 chips  
 Green = Good chips  
 Red = Bad chips  
 White = Dead area of the wafer

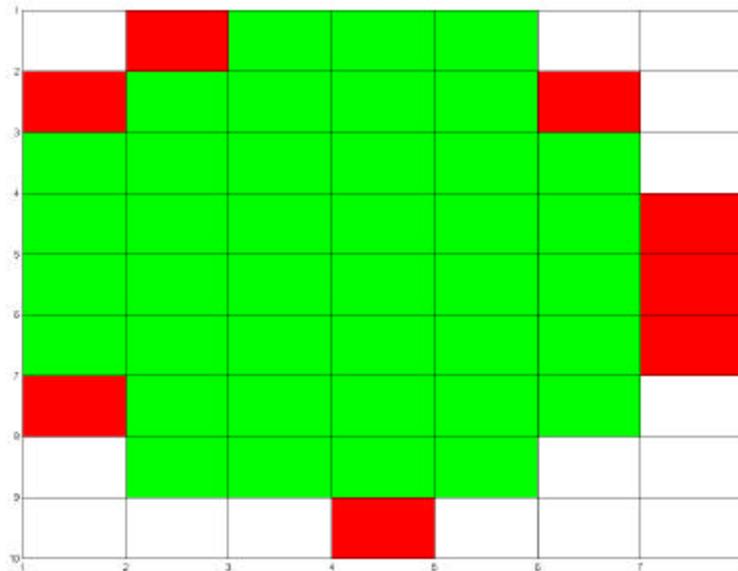


Figure 5

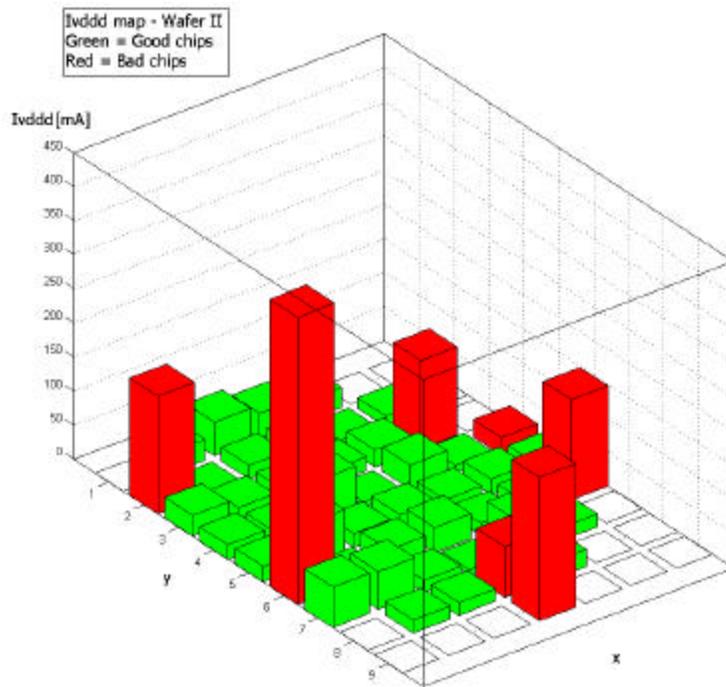


Figure 6

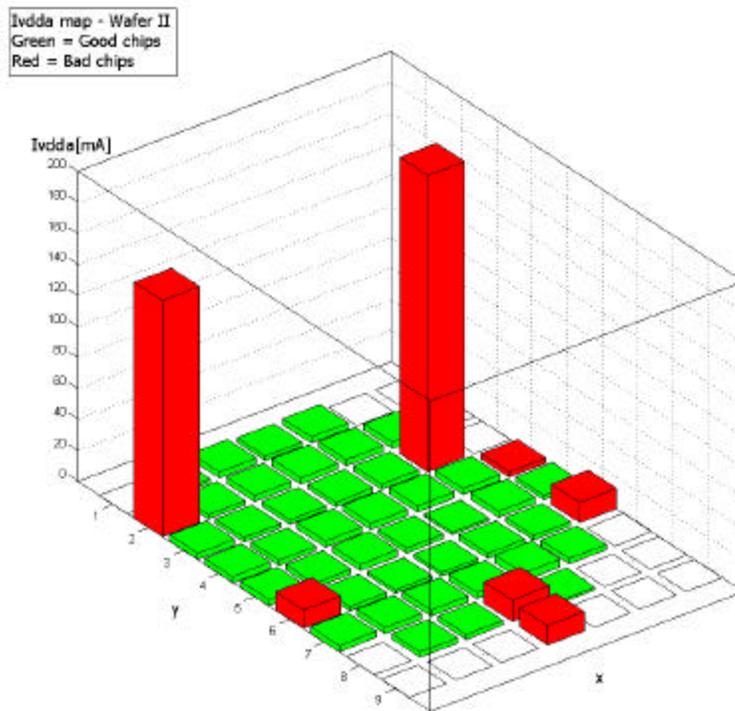


Figure 7

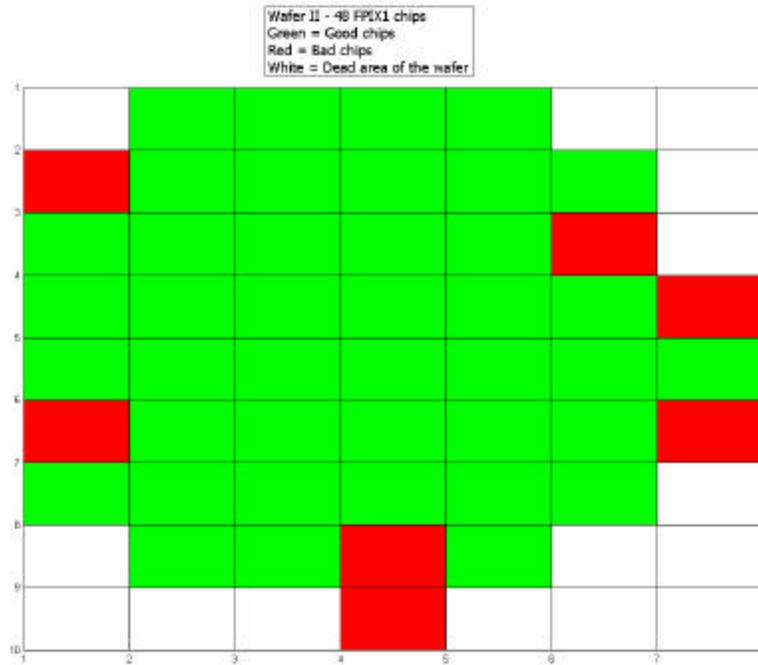


Figure 8

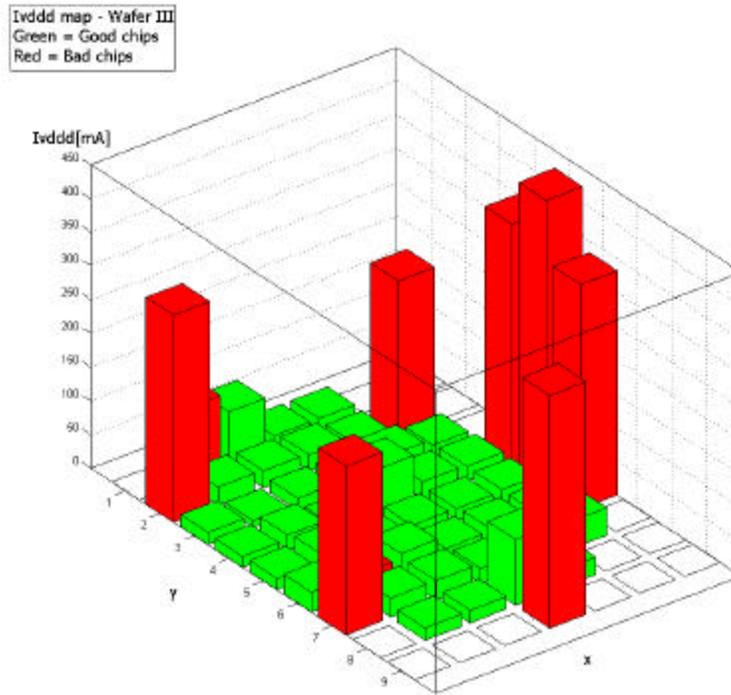


Figure 9

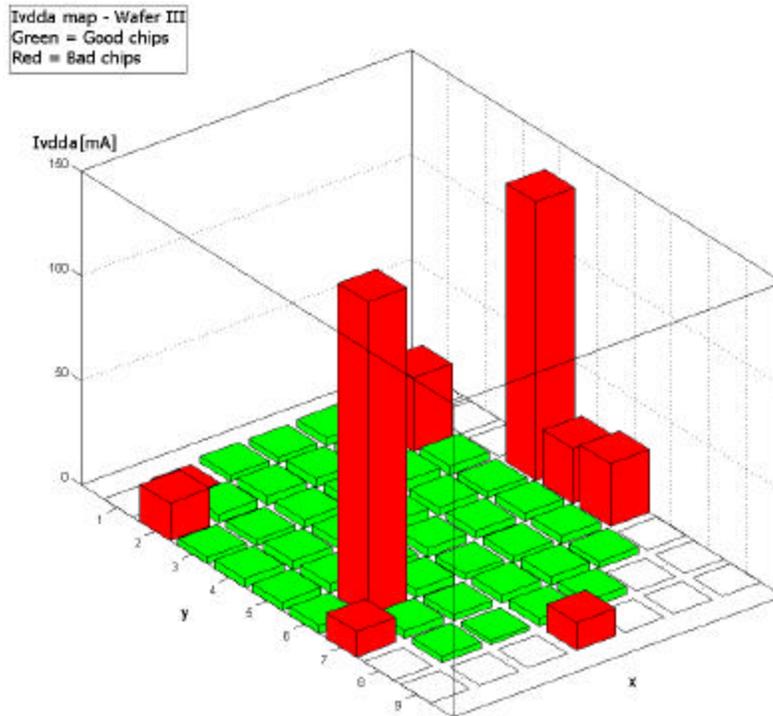


Figure 10

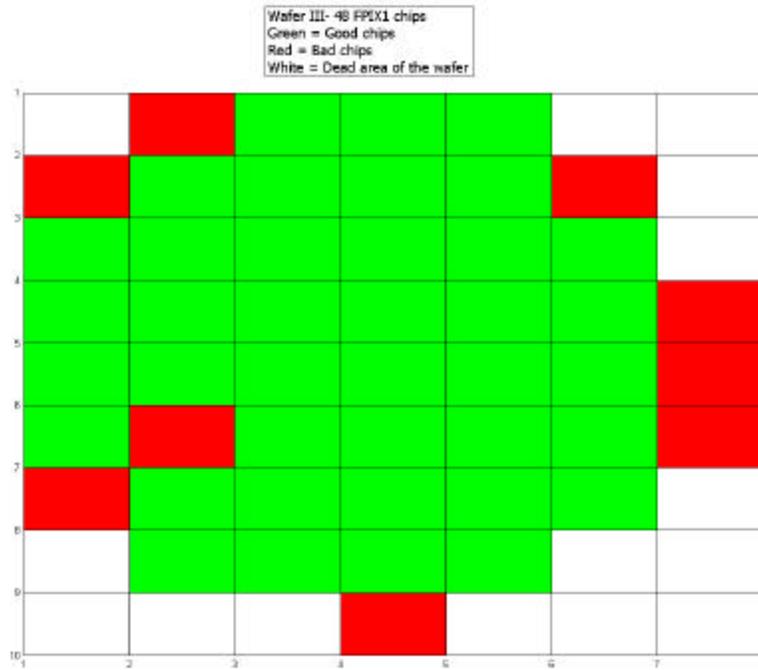
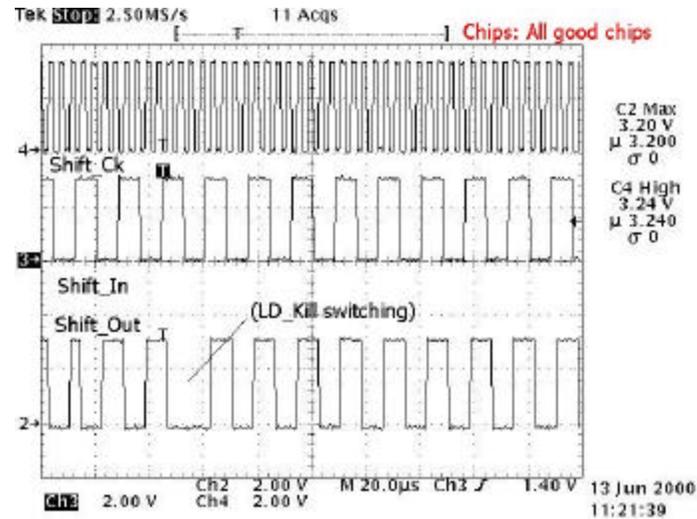


Figure 11

The following pictures show the oscilloscope screen with the outputs from each one of the chips. It demonstrates the reason why each one of them did or did not pass the test.



**Figure 12**

Figure 12 represents the expected output from this test. Given a pattern in the input of the shift registers (Shift\_In), the same pattern is seen in the output, considering some delay and an inversion. A chip that has this behavior is considered a good chip. On the other hand, Figure 13 shows the result from a chip where the shift registers are not working properly. In this case Shift\_Out will be present for some paths (combination of Reg\_0, Reg\_1, Reg\_2 and LD\_Kill) and not for others. In the top right corner are the identification numbers of such chips.

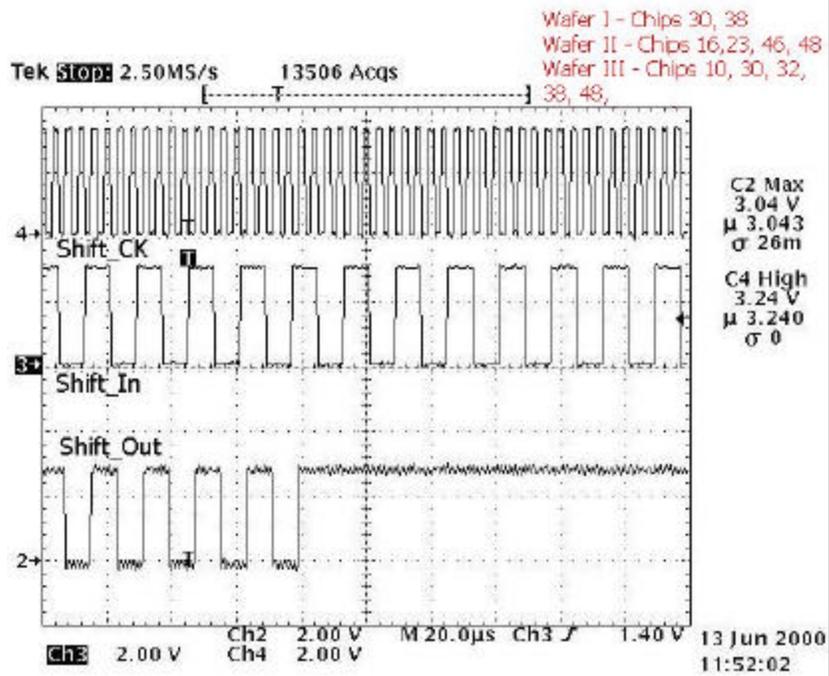


Figure 13

Figure 14 and Figure 15 show the case where the chip has its output Shift\_Out stuck respectively in GND and Vdd.

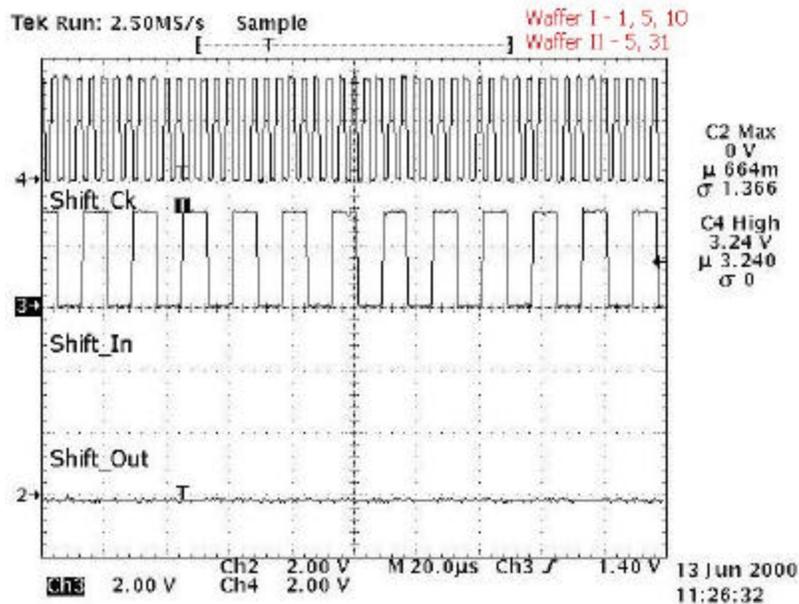


Figure 14

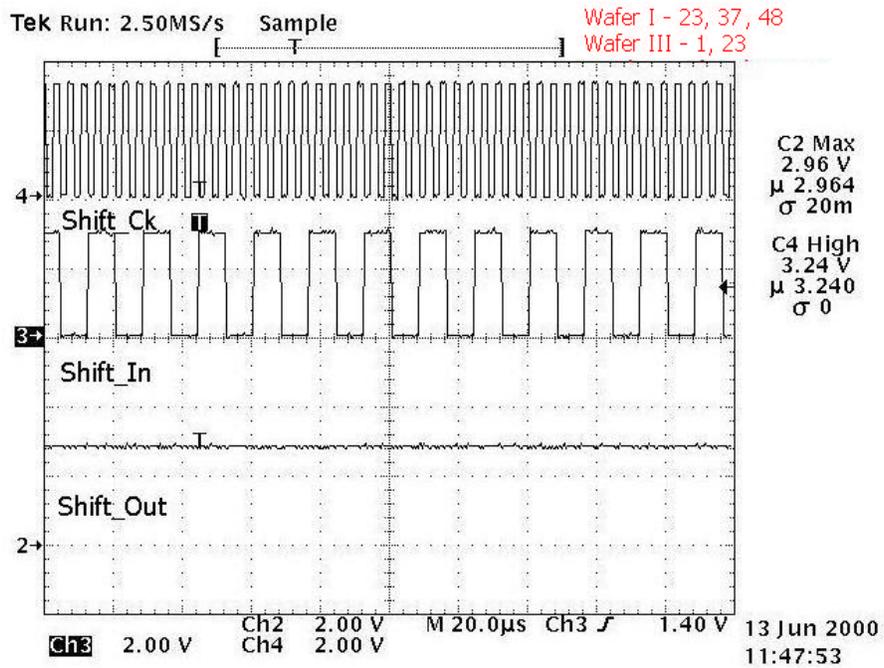


Figure 15

## Appendix – Test Stand Pictures



Figure 16 – Equipments used to perform wafer tests

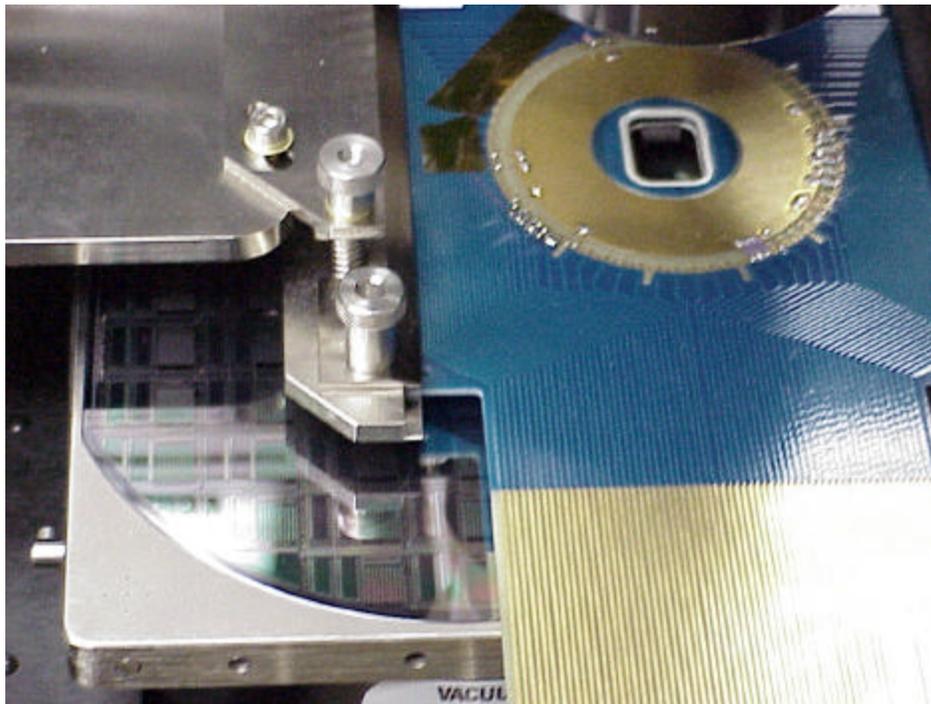
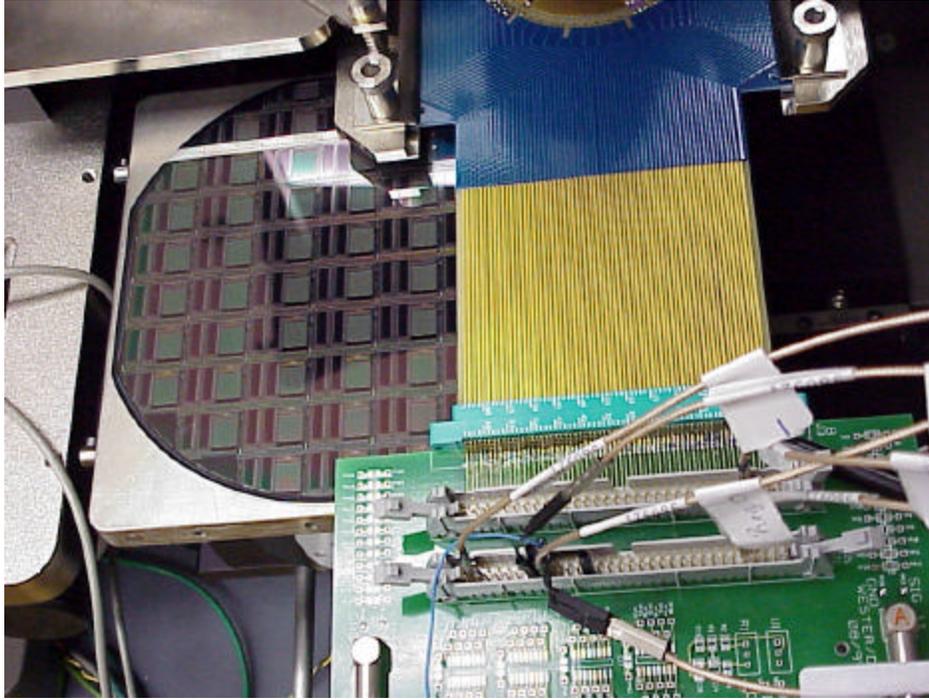


Figure 17 – FPIX1 chip being tested on a wafer



**Figure 18 – Detail showing wafer and connections in the probe card**