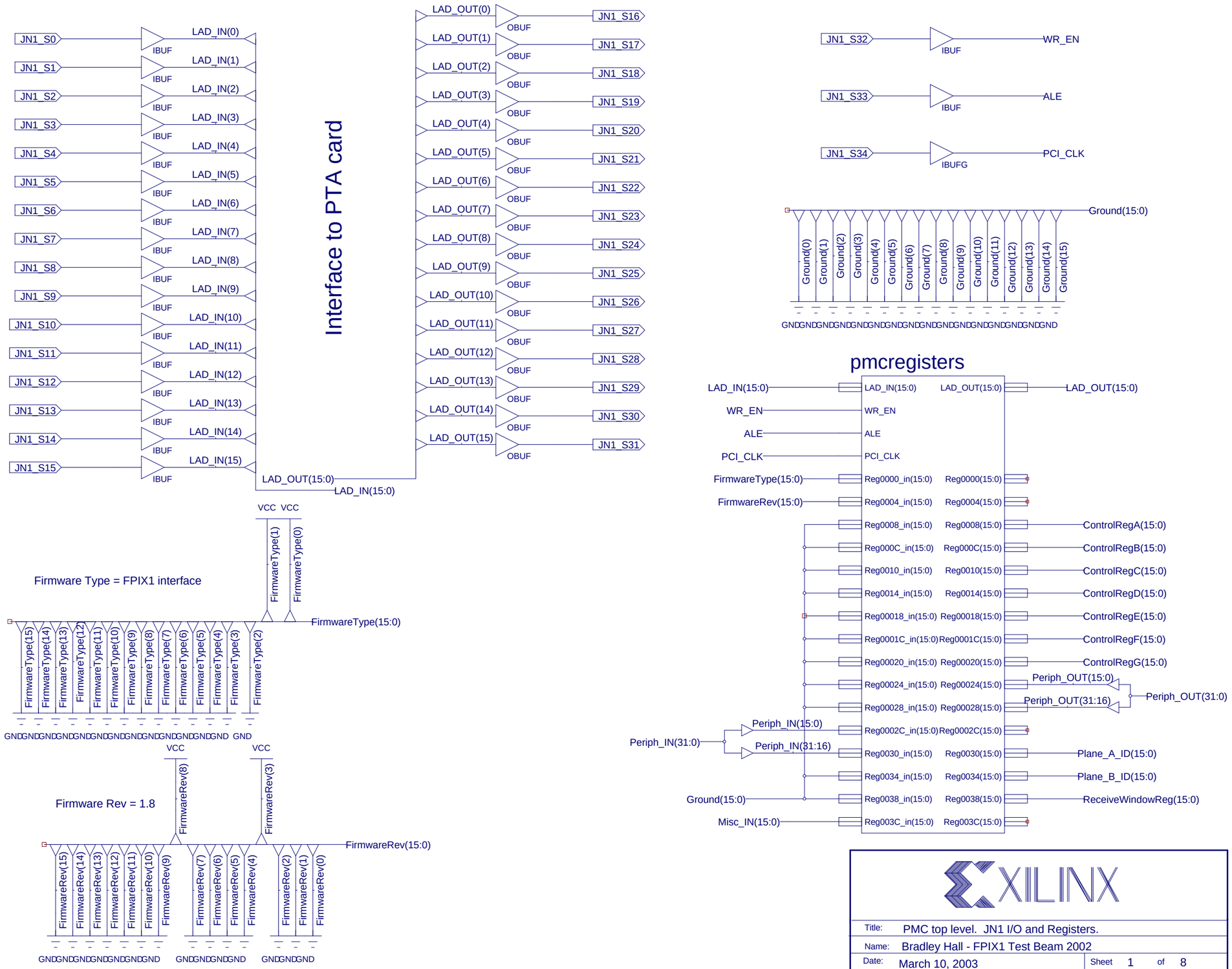
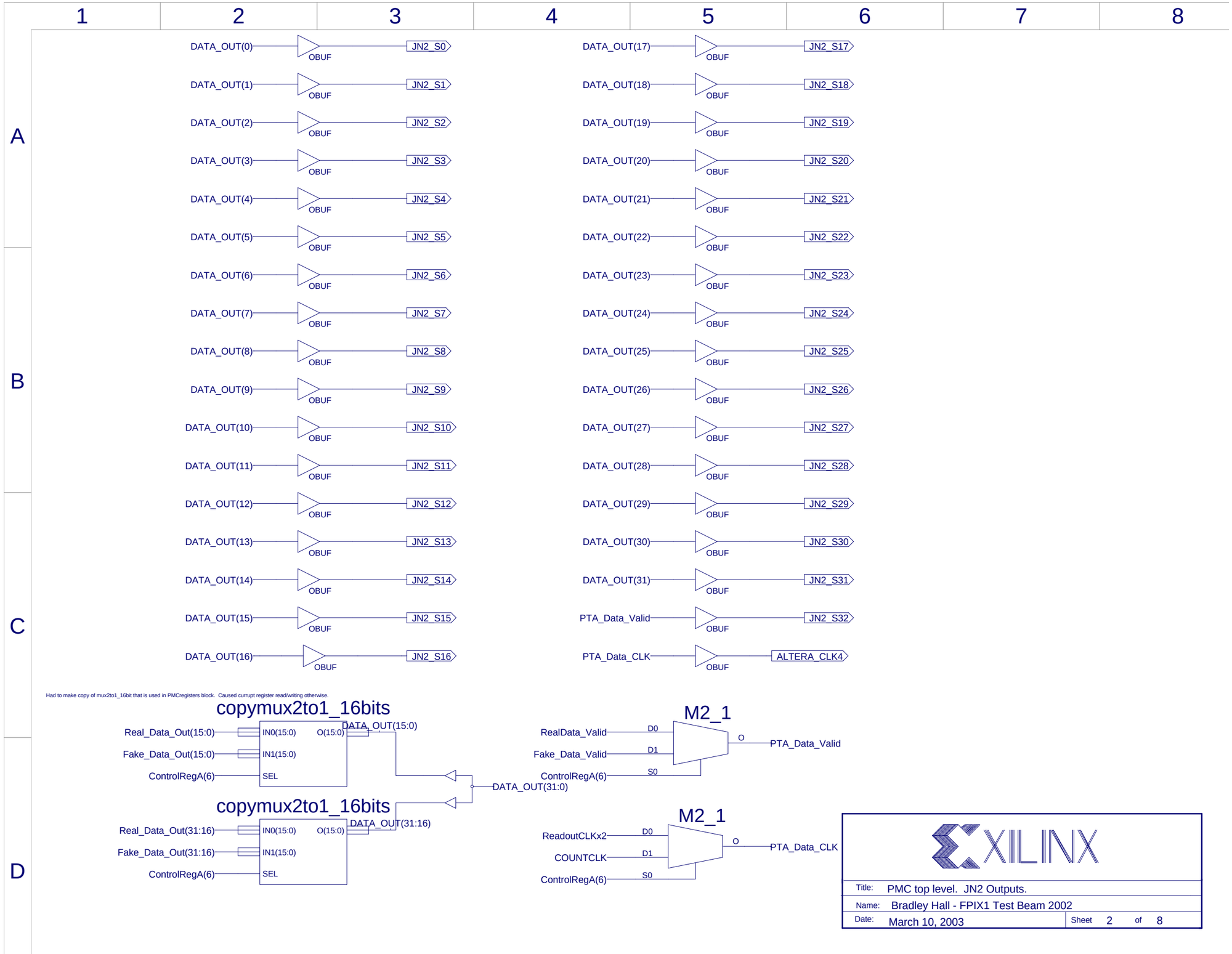
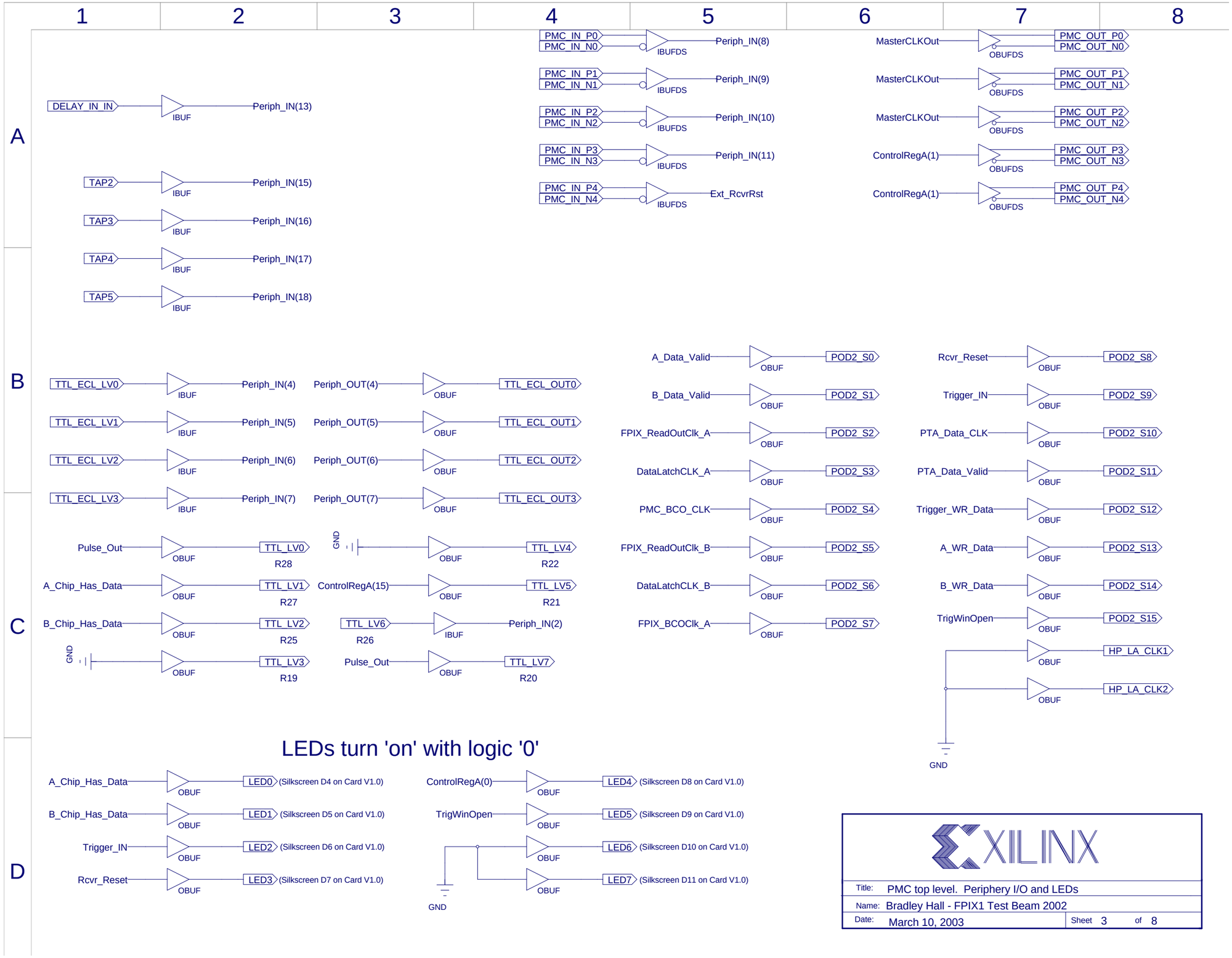
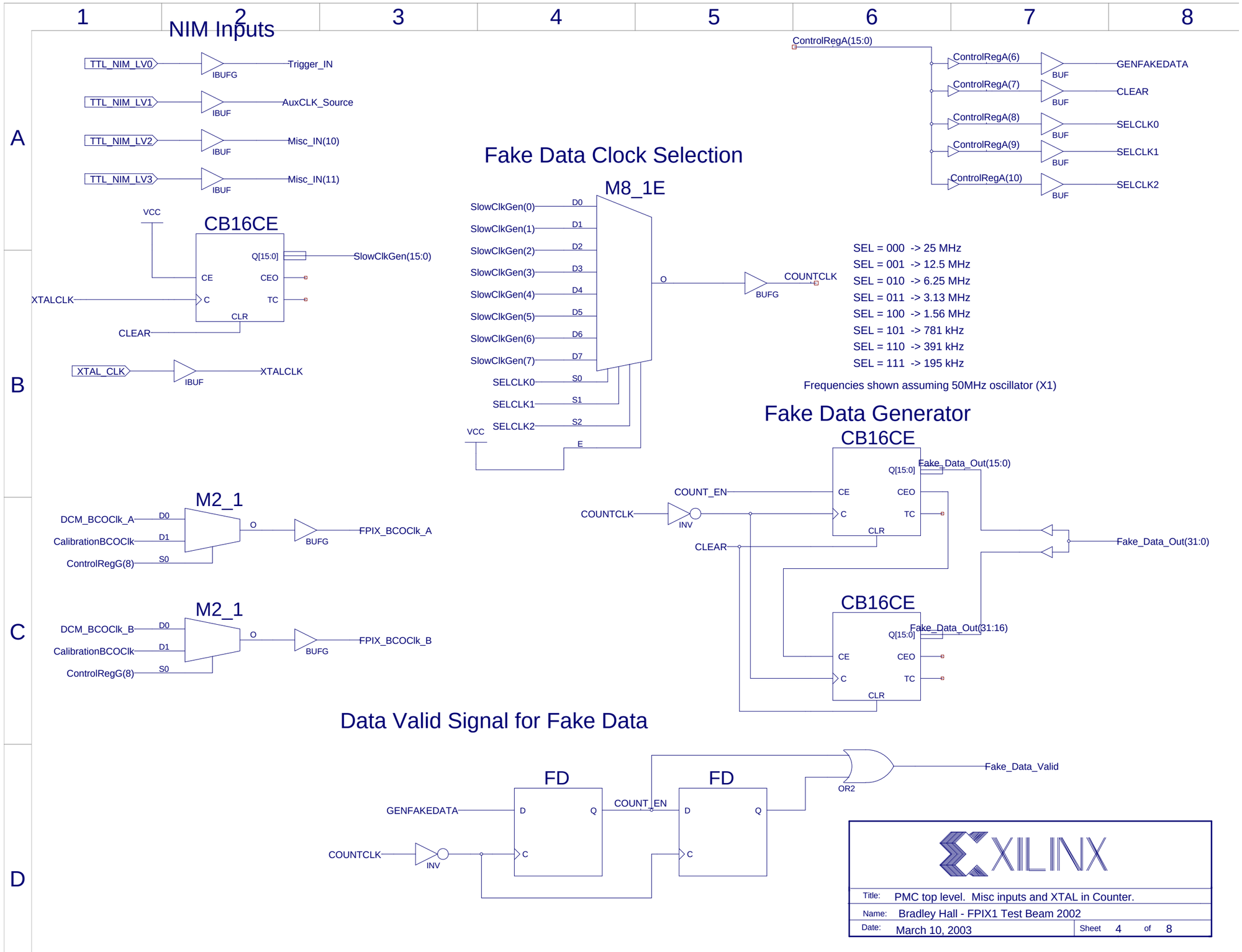
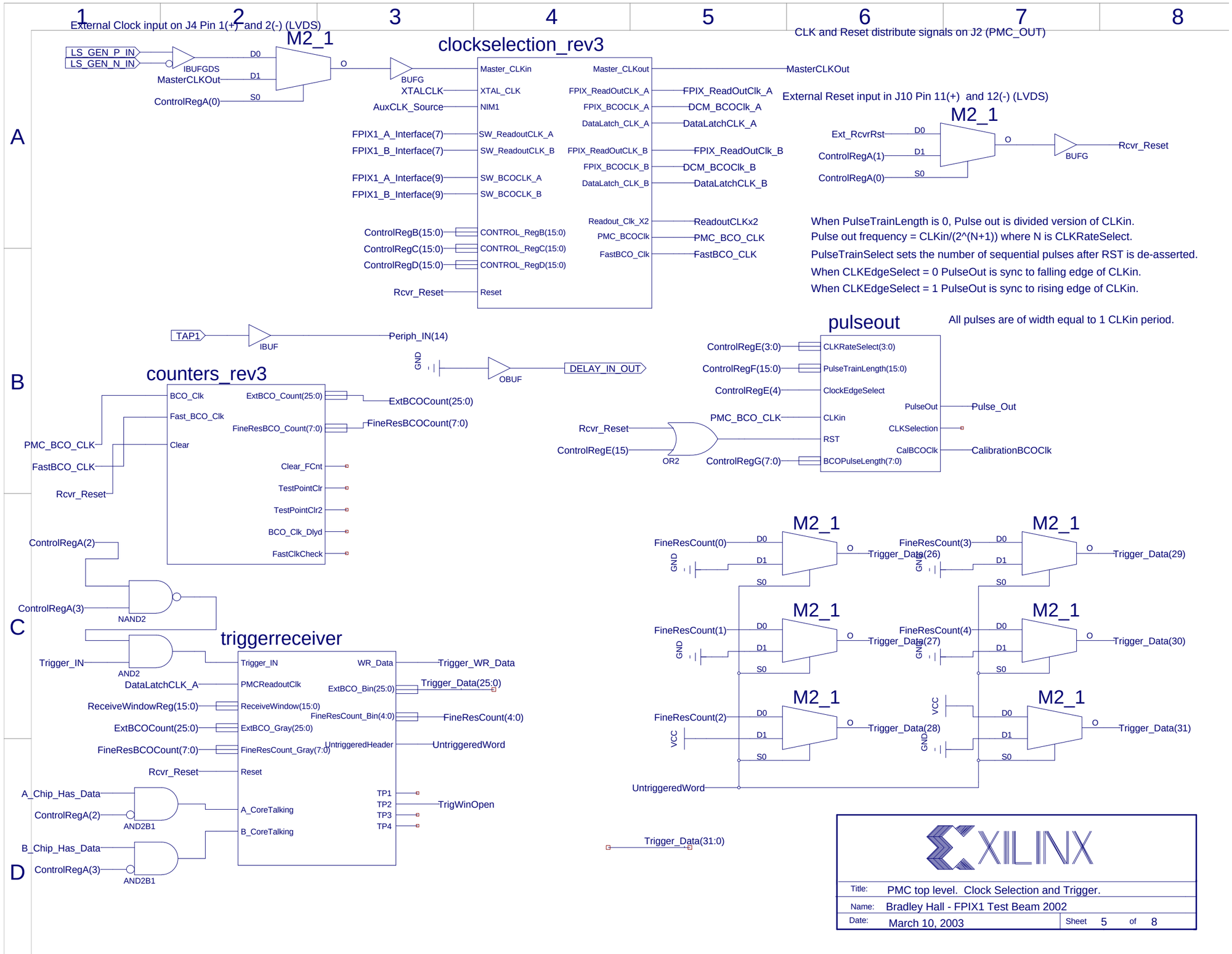

Interface to PTA card
JN1_S0 IBUF LAD_IN(0)
JN1_S1 IBUF LAD_IN(1)
JN1_S2 IBUF LAD_IN(2)
JN1_S3 IBUF LAD_IN(3)
JN1_S4 IBUF LAD_IN(4)
JN1_S5 IBUF LAD_IN(5)
JN1_S6 IBUF LAD_IN(6)
JN1_S7 IBUF LAD_IN(7)
JN1_S8 IBUF LAD_IN(8)
JN1_S9 IBUF LAD_IN(9)
JN1_S10 IBUF LAD_IN(10)
JN1_S11 IBUF LAD_IN(11)
JN1_S12 IBUF LAD_IN(12)
JN1_S13 IBUF LAD_IN(13)
JN1_S14 IBUF LAD_IN(14)
JN1_S15 IBUF LAD_IN(15)
LAD_OUT(15:0)
LAD_IN(15:0)
LAD_OUT(0) OBUF JN1_S16
LAD_OUT(1) OBUF JN1_S17
LAD_OUT(2) OBUF JN1_S18
LAD_OUT(3) OBUF JN1_S19
LAD_OUT(4) OBUF JN1_S20
LAD_OUT(5) OBUF JN1_S21
LAD_OUT(6) OBUF JN1_S22
LAD_OUT(7) OBUF JN1_S23
LAD_OUT(8) OBUF JN1_S24
LAD_OUT(9) OBUF JN1_S25
LAD_OUT(10) OBUF JN1_S26
LAD_OUT(11) OBUF JN1_S27
LAD_OUT(12) OBUF JN1_S28
LAD_OUT(13) OBUF JN1_S29
LAD_OUT(14) OBUF JN1_S30
LAD_OUT(15) OBUF JN1_S31
JN1_S32 IBUF WR_EN
JN1_S33 IBUF ALE
JN1_S34 IBUFG PCI_CLK
Ground(15:0)
Ground(0) Ground(1) Ground(2) Ground(3) Ground(4) Ground(5) Ground(6) Ground(7) Ground(8) Ground(9) Ground(10) Ground(11) Ground(12) Ground(13) Ground(14) Ground(15)
GND GND GND GND GND GND GND GND GND GND GND GND GND GND GND GND
pmcregisters
LAD_IN(15:0) LAD_IN(15:0) LAD_OUT(15:0) LAD_OUT(15:0)
WR_EN WR_EN
ALE ALE
PCI_CLK PCI_CLK
FirmwareType(15:0) Reg0000_in(15:0) Reg0000(15:0)
FirmwareRev(15:0) Reg0004_in(15:0) Reg0004(15:0)
Reg0008_in(15:0) Reg0008(15:0) ControlRegA(15:0)
Reg000C_in(15:0) Reg000C(15:0) ControlRegB(15:0)
Reg0010_in(15:0) Reg0010(15:0) ControlRegC(15:0)
Reg0014_in(15:0) Reg0014(15:0) ControlRegD(15:0)
Reg00018_in(15:0) Reg00018(15:0) ControlRegE(15:0)
Reg0001C_in(15:0) Reg0001C(15:0) ControlRegF(15:0)
Reg00020_in(15:0) Reg00020(15:0) ControlRegG(15:0)
Reg00024_in(15:0) Reg00024(15:0) Periph_OUT(15:0)
Reg00028_in(15:0) Reg00028(15:0) Periph_OUT(31:16) Periph_OUT(31:0)
Periph_IN(15:0) Periph_IN(31:0) Periph_IN(31:16)
Reg0002C_in(15:0) Reg0002C(15:0)
Reg0030_in(15:0) Reg0030(15:0) Plane_A_ID(15:0)
Reg0034_in(15:0) Reg0034(15:0) Plane_B_ID(15:0)
Ground(15:0) Reg0038_in(15:0) Reg0038(15:0) ReceiveWindowReg(15:0)
Misc_IN(15:0) Reg003C_in(15:0) Reg003C(15:0)
VCC VCC
FirmwareType(1) FirmwareType(0)
Firmware Type = FPIX1 interface
FirmwareType(15:0)
FirmwareType(15) FirmwareType(14) FirmwareType(13) FirmwareType(12) FirmwareType(11) FirmwareType(10) FirmwareType(9) FirmwareType(8) FirmwareType(7) FirmwareType(6) FirmwareType(5) FirmwareType(4) FirmwareType(3) FirmwareType(2)
GND GND GND GND GND GND GND GND GND GND GND GND GND GND GND GND GND
VCC VCC
FirmwareRev(8) FirmwareRev(3)
Firmware Rev = 1.8
FirmwareRev(15:0)
FirmwareRev(15) FirmwareRev(14) FirmwareRev(13) FirmwareRev(12) FirmwareRev(11) FirmwareRev(10) FirmwareRev(9) FirmwareRev(7) FirmwareRev(6) FirmwareRev(5) FirmwareRev(4) FirmwareRev(2) FirmwareRev(1) FirmwareRev(0)
GND GND GND GND GND GND GND GND GND GND GND GND GND GND GND GND
XILINX
Title: PMC top level. JN1 I/O and Registers.
Name: Bradley Hall - FPIX1 Test Beam 2002
Date: March 10, 2003
Sheet 1 of 8


DATA_OUT(0) OBUF JN2_S0
DATA_OUT(1) OBUF JN2_S1
DATA_OUT(2) OBUF JN2_S2
DATA_OUT(3) OBUF JN2_S3
DATA_OUT(4) OBUF JN2_S4
DATA_OUT(5) OBUF JN2_S5
DATA_OUT(6) OBUF JN2_S6
DATA_OUT(7) OBUF JN2_S7
DATA_OUT(8) OBUF JN2_S8
DATA_OUT(9) OBUF JN2_S9
DATA_OUT(10) OBUF JN2_S10
DATA_OUT(11) OBUF JN2_S11
DATA_OUT(12) OBUF JN2_S12
DATA_OUT(13) OBUF JN2_S13
DATA_OUT(14) OBUF JN2_S14
DATA_OUT(15) OBUF JN2_S15
DATA_OUT(16) OBUF JN2_S16
DATA_OUT(17) OBUF JN2_S17
DATA_OUT(18) OBUF JN2_S18
DATA_OUT(19) OBUF JN2_S19
DATA_OUT(20) OBUF JN2_S20
DATA_OUT(21) OBUF JN2_S21
DATA_OUT(22) OBUF JN2_S22
DATA_OUT(23) OBUF JN2_S23
DATA_OUT(24) OBUF JN2_S24
DATA_OUT(25) OBUF JN2_S25
DATA_OUT(26) OBUF JN2_S26
DATA_OUT(27) OBUF JN2_S27
DATA_OUT(28) OBUF JN2_S28
DATA_OUT(29) OBUF JN2_S29
DATA_OUT(30) OBUF JN2_S30
DATA_OUT(31) OBUF JN2_S31
PTA_Data_Valid OBUF JN2_S32
PTA_Data_CLK OBUF ALTERA_CLK4
Had to make copy of mux2to1_16bit that is used in PMCregisters block. Caused currupt register read/writing otherwise.
copymux2to1_16bits
Real_Data_Out(15:0) IN0(15:0) O(15:0) DATA_OUT(15:0)
Fake_Data_Out(15:0) IN1(15:0)
ControlRegA(6) SEL
copymux2to1_16bits
Real_Data_Out(31:16) IN0(15:0) O(15:0) DATA_OUT(31:16)
Fake_Data_Out(31:16) IN1(15:0)
ControlRegA(6) SEL
DATA_OUT(31:0)
M2_1
RealData_Valid D0
Fake_Data_Valid D1
ControlRegA(6) S0
O PTA_Data_Valid
M2_1
ReadoutCLKx2 D0
COUNTCLK D1
ControlRegA(6) S0
O PTA_Data_CLK
XILINX
Title: PMC top level. JN2 Outputs.
Name: Bradley Hall - FPIX1 Test Beam 2002
Date: March 10, 2003
Sheet 2 of 8

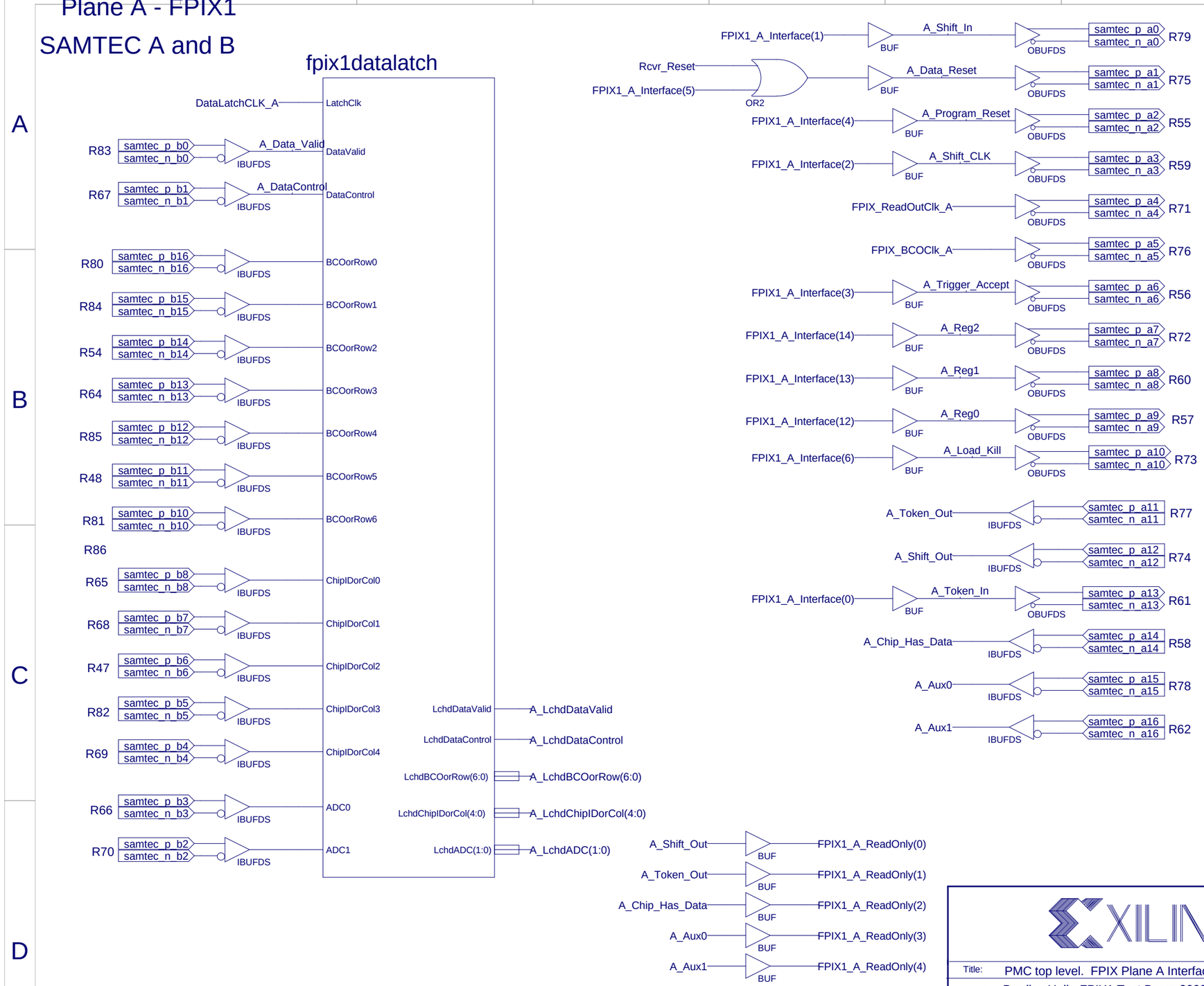

1 2 3 4 5 6 7 8
A
B
C
D
DELAY_IN_IN
IBUF
Periph_IN(13)
TAP2
Periph_IN(15)
TAP3
Periph_IN(16)
TAP4
Periph_IN(17)
TAP5
Periph_IN(18)
PMC_IN_P0
PMC_IN_N0
IBUFDS
Periph_IN(8)
PMC_IN_P1
PMC_IN_N1
Periph_IN(9)
PMC_IN_P2
PMC_IN_N2
Periph_IN(10)
PMC_IN_P3
PMC_IN_N3
Periph_IN(11)
PMC_IN_P4
PMC_IN_N4
Ext_RcvrRst
MasterCLKOut
OBUFDS
PMC_OUT_P0
PMC_OUT_N0
PMC_OUT_P1
PMC_OUT_N1
PMC_OUT_P2
PMC_OUT_N2
ControlRegA(1)
PMC_OUT_P3
PMC_OUT_N3
PMC_OUT_P4
PMC_OUT_N4
TTL_ECL_LV0
Periph_IN(4)
Periph_OUT(4)
TTL_ECL_OUT0
TTL_ECL_LV1
Periph_IN(5)
Periph_OUT(5)
TTL_ECL_OUT1
TTL_ECL_LV2
Periph_IN(6)
Periph_OUT(6)
TTL_ECL_OUT2
TTL_ECL_LV3
Periph_IN(7)
Periph_OUT(7)
TTL_ECL_OUT3
Pulse_Out
TTL_LV0
R28
GND
TTL_LV4
R22
A_Chip_Has_Data
TTL_LV1
R27
ControlRegA(15)
TTL_LV5
R21
B_Chip_Has_Data
TTL_LV2
R25
TTL_LV6
R26
Periph_IN(2)
TTL_LV3
R19
TTL_LV7
R20
A_Data_Valid
POD2_S0
B_Data_Valid
POD2_S1
FPIX_ReadOutClk_A
POD2_S2
DataLatchCLK_A
POD2_S3
PMC_BCO_CLK
POD2_S4
FPIX_ReadOutClk_B
POD2_S5
DataLatchCLK_B
POD2_S6
FPIX_BCOClk_A
POD2_S7
Rcvr_Reset
POD2_S8
Trigger_IN
POD2_S9
PTA_Data_CLK
POD2_S10
PTA_Data_Valid
POD2_S11
Trigger_WR_Data
POD2_S12
A_WR_Data
POD2_S13
B_WR_Data
POD2_S14
TrigWinOpen
POD2_S15
HP_LA_CLK1
HP_LA_CLK2
LEDs turn 'on' with logic '0'
A_Chip_Has_Data
LED0 (Silkscreen D4 on Card V1.0)
B_Chip_Has_Data
LED1 (Silkscreen D5 on Card V1.0)
Trigger_IN
LED2 (Silkscreen D6 on Card V1.0)
Rcvr_Reset
LED3 (Silkscreen D7 on Card V1.0)
ControlRegA(0)
LED4 (Silkscreen D8 on Card V1.0)
TrigWinOpen
LED5 (Silkscreen D9 on Card V1.0)
LED6 (Silkscreen D10 on Card V1.0)
LED7 (Silkscreen D11 on Card V1.0)
OBUF
XILINX
Title: PMC top level. Periphery I/O and LEDs
Name: Bradley Hall - FPIX1 Test Beam 2002
Date: March 10, 2003
Sheet 3 of 8


NIM Inputs
TTL_NIM_LV0
IBUFG
Trigger_IN
TTL_NIM_LV1
IBUF
AuxCLK_Source
TTL_NIM_LV2
IBUF
Misc_IN(10)
TTL_NIM_LV3
IBUF
Misc_IN(11)
VCC
CB16CE
Q[15:0]
SlowClkGen(15:0)
CE
CEO
XTALCLK
C
TC
CLR
CLEAR
XTAL_CLK
IBUF
XTALCLK
ControlRegA(15:0)
ControlRegA(6)
BUF
GENFAKEDATA
ControlRegA(7)
BUF
CLEAR
ControlRegA(8)
BUF
SELCLK0
ControlRegA(9)
BUF
SELCLK1
ControlRegA(10)
BUF
SELCLK2
Fake Data Clock Selection
M8_1E
SlowClkGen(0)
D0
SlowClkGen(1)
D1
SlowClkGen(2)
D2
SlowClkGen(3)
D3
SlowClkGen(4)
D4
SlowClkGen(5)
D5
SlowClkGen(6)
D6
SlowClkGen(7)
D7
SELCLK0
S0
SELCLK1
S1
SELCLK2
S2
VCC
E
O
BUFG
COUNTCLK
SEL = 000 -> 25 MHz
SEL = 001 -> 12.5 MHz
SEL = 010 -> 6.25 MHz
SEL = 011 -> 3.13 MHz
SEL = 100 -> 1.56 MHz
SEL = 101 -> 781 kHz
SEL = 110 -> 391 kHz
SEL = 111 -> 195 kHz
Frequencies shown assuming 50MHz oscillator (X1)
Fake Data Generator
CB16CE
Q[15:0]
Fake_Data_Out(15:0)
COUNT_EN
CE
CEO
COUNTCLK
C
TC
INV
CLR
CLEAR
Fake_Data_Out(31:0)
CB16CE
Q[15:0]
Fake_Data_Out(31:16)
CE
CEO
C
TC
CLR
M2_1
DCM_BCOClk_A
D0
CalibrationBCOClk
D1
ControlRegG(8)
S0
O
BUFG
FPIX_BCOClk_A
M2_1
DCM_BCOClk_B
D0
CalibrationBCOClk
D1
ControlRegG(8)
S0
O
BUFG
FPIX_BCOClk_B
Data Valid Signal for Fake Data
FD
GENFAKEDATA
D
Q
COUNTCLK
INV
C
COUNT_EN
FD
D
Q
C
OR2
Fake_Data_Valid
XILINX
Title: PMC top level. Misc inputs and XTAL in Counter.
Name: Bradley Hall - FPIX1 Test Beam 2002
Date: March 10, 2003
Sheet 4 of 8


1
2
3
4
5
6
7
8
A
B
C
D
External Clock input on J4 Pin 1(+) and 2(-) (LVDS)
LS_GEN_P_IN
LS_GEN_N_IN
IBUFGDS
MasterCLKOut
ControlRegA(0)
M2_1
D0
D1
S0
O
BUFG
clockselection_rev3
Master_CLKin
XTALCLK
XTAL_CLK
AuxCLK_Source
NIM1
FPIX1_A_Interface(7)
SW_ReadoutCLK_A
FPIX1_B_Interface(7)
SW_ReadoutCLK_B
FPIX1_A_Interface(9)
SW_BCOCLK_A
FPIX1_B_Interface(9)
SW_BCOCLK_B
ControlRegB(15:0)
CONTROL_RegB(15:0)
ControlRegC(15:0)
CONTROL_RegC(15:0)
ControlRegD(15:0)
CONTROL_RegD(15:0)
Rcvr_Reset
Reset
Master_CLKout
MasterCLKOut
FPIX_ReadOutCLK_A
FPIX_ReadOutCLK_A
FPIX_BCOCLK_A
DCM_BCOClk_A
DataLatch_CLK_A
DataLatchCLK_A
FPIX_ReadOutCLK_B
FPIX_ReadOutClk_B
FPIX_BCOCLK_B
DCM_BCOClk_B
DataLatch_CLK_B
DataLatchCLK_B
Readout_Clk_X2
ReadoutCLKx2
PMC_BCOClk
PMC_BCO_CLK
FastBCO_Clk
FastBCO_CLK
CLK and Reset distribute signals on J2 (PMC_OUT)
External Reset input in J10 Pin 11(+) and 12(-) (LVDS)
M2_1
Ext_RcvrRst
ControlRegA(1)
ControlRegA(0)
D0
D1
S0
O
BUFG
Rcvr_Reset
When PulseTrainLength is 0, Pulse out is divided version of CLKin.
Pulse out frequency = CLKin/(2^(N+1)) where N is CLKRateSelect.
PulseTrainSelect sets the number of sequential pulses after RST is de-asserted.
When CLKEdgeSelect = 0 PulseOut is sync to falling edge of CLKin.
When CLKEdgeSelect = 1 PulseOut is sync to rising edge of CLKin.
TAP1
IBUF
Periph_IN(14)
GND
OBUF
DELAY_IN_OUT
pulseout
All pulses are of width equal to 1 CLKin period.
ControlRegE(3:0)
CLKRateSelect(3:0)
ControlRegF(15:0)
PulseTrainLength(15:0)
ControlRegE(4)
ClockEdgeSelect
PMC_BCO_CLK
CLKin
Rcvr_Reset
RST
ControlRegE(15)
OR2
ControlRegG(7:0)
BCOPulseLength(7:0)
PulseOut
Pulse_Out
CLKSelection
CalBCOClk
CalibrationBCOClk
counters_rev3
BCO_Clk
Fast_BCO_Clk
Clear
PMC_BCO_CLK
FastBCO_CLK
Rcvr_Reset
ExtBCO_Count(25:0)
ExtBCOCount(25:0)
FineResBCO_Count(7:0)
FineResBCOCount(7:0)
Clear_FCnt
TestPointClr
TestPointClr2
BCO_Clk_Dlyd
FastClkCheck
ControlRegA(2)
ControlRegA(3)
NAND2
Trigger_IN
AND2
triggerreceiver
Trigger_IN
DataLatchCLK_A
PMCReadoutClk
ReceiveWindowReg(15:0)
ReceiveWindow(15:0)
ExtBCOCount(25:0)
ExtBCO_Gray(25:0)
FineResBCOCount(7:0)
FineResCount_Gray(7:0)
Rcvr_Reset
Reset
A_Chip_Has_Data
ControlRegA(2)
AND2B1
A_CoreTalking
B_Chip_Has_Data
ControlRegA(3)
AND2B1
B_CoreTalking
WR_Data
Trigger_WR_Data
ExtBCO_Bin(25:0)
Trigger_Data(25:0)
FineResCount_Bin(4:0)
FineResCount(4:0)
UntriggeredHeader
UntriggeredWord
TP1
TP2
TP3
TP4
TrigWinOpen
M2_1
FineResCount(0)
GND
Trigger_Data(26)
FineResCount(3)
Trigger_Data(29)
FineResCount(1)
Trigger_Data(27)
FineResCount(4)
Trigger_Data(30)
FineResCount(2)
VCC
Trigger_Data(28)
Trigger_Data(31)
UntriggeredWord
Trigger_Data(31:0)
XILINX
Title: PMC top level. Clock Selection and Trigger.
Name: Bradley Hall - FPIX1 Test Beam 2002
Date: March 10, 2003
Sheet 5 of 8

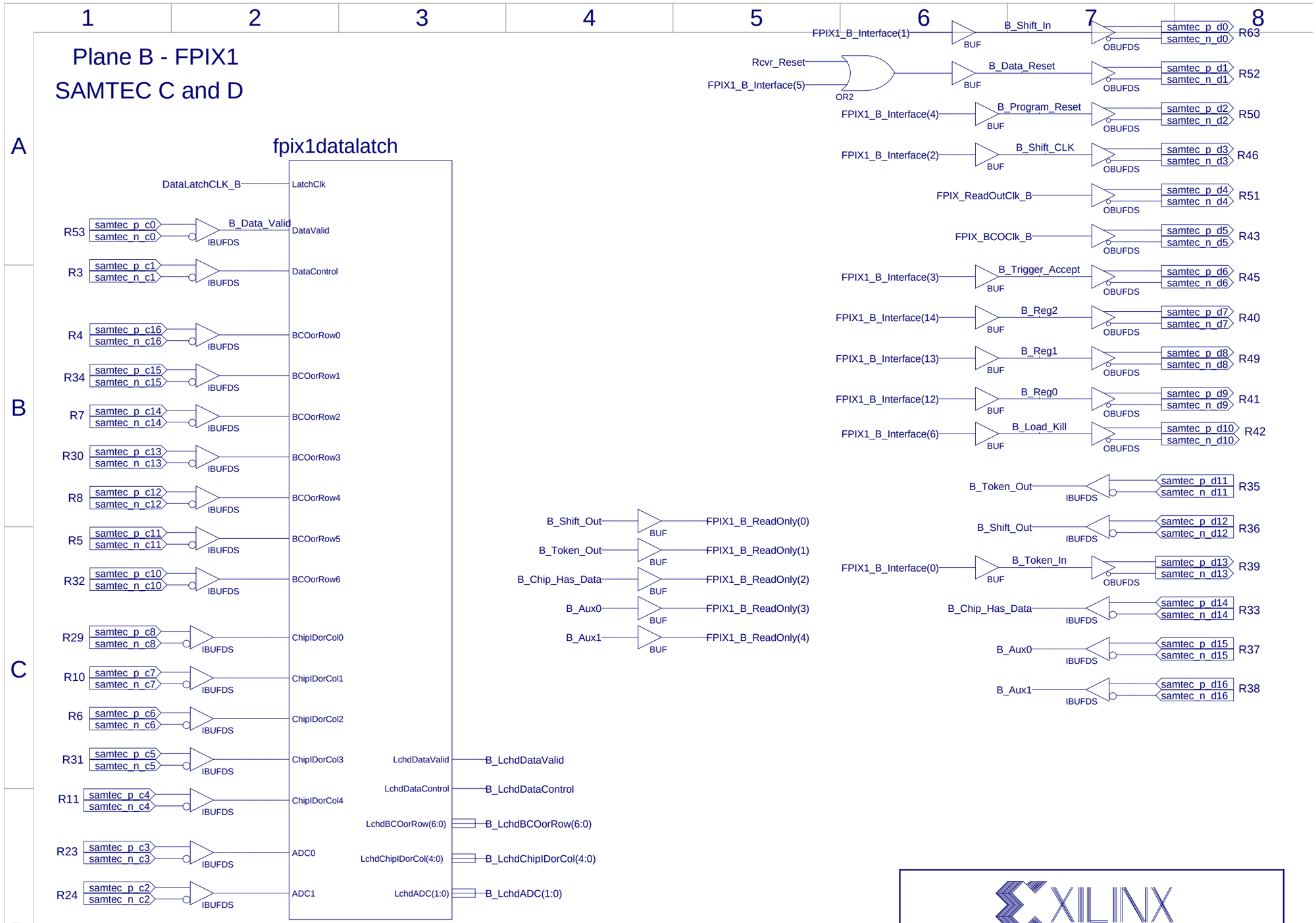
Plane A - FPIX1

SAMTEC A and B

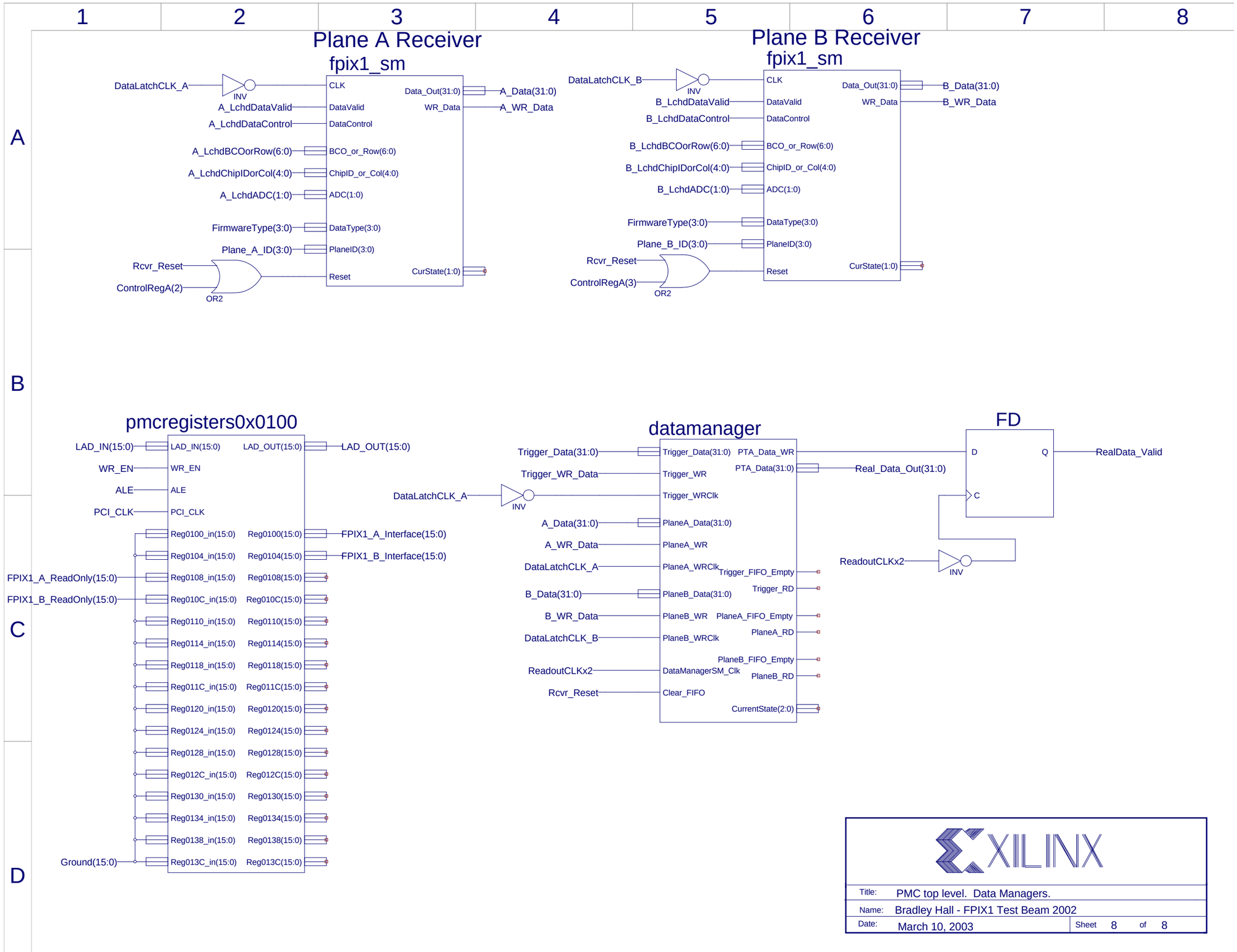


Title:	PMC top level. FPIX Plane A Interface.
Name:	Bradley Hall - FPIX1 Test Beam 2002
Date:	March 10, 2003
Sheet	6 of 8

Plane B - FPIX1
SAMTEC C and D



Title:	PMC top level. FPIX Plane B Interface.
Name:	Bradley Hall - FPIX1 Test Beam 2002
Date:	March 10, 2003
Sheet	7 of 8


Plane A Receiver
fpix1_sm
DataLatchCLK_A
INV
A_LchdDataValid
A_LchdDataControl
A_LchdBCOorRow(6:0)
A_LchdChipIDorCol(4:0)
A_LchdADC(1:0)
FirmwareType(3:0)
Plane_A_ID(3:0)
Rcvr_Reset
ControlRegA(2)
OR2
CLK
DataValid
DataControl
BCO_or_Row(6:0)
ChipID_or_Col(4:0)
ADC(1:0)
DataType(3:0)
PlaneID(3:0)
Reset
Data_Out(31:0)
WR_Data
CurState(1:0)
A_Data(31:0)
A_WR_Data
Plane B Receiver
fpix1_sm
DataLatchCLK_B
INV
B_LchdDataValid
B_LchdDataControl
B_LchdBCOorRow(6:0)
B_LchdChipIDorCol(4:0)
B_LchdADC(1:0)
FirmwareType(3:0)
Plane_B_ID(3:0)
Rcvr_Reset
ControlRegA(3)
OR2
CLK
DataValid
DataControl
BCO_or_Row(6:0)
ChipID_or_Col(4:0)
ADC(1:0)
DataType(3:0)
PlaneID(3:0)
Reset
Data_Out(31:0)
WR_Data
CurState(1:0)
B_Data(31:0)
B_WR_Data
pmcregisters0x0100
LAD_IN(15:0)
WR_EN
ALE
PCI_CLK
FPIX1_A_ReadOnly(15:0)
FPIX1_B_ReadOnly(15:0)
Ground(15:0)
LAD_IN(15:0)
WR_EN
ALE
PCI_CLK
Reg0100_in(15:0)
Reg0104_in(15:0)
Reg0108_in(15:0)
Reg010C_in(15:0)
Reg0110_in(15:0)
Reg0114_in(15:0)
Reg0118_in(15:0)
Reg011C_in(15:0)
Reg0120_in(15:0)
Reg0124_in(15:0)
Reg0128_in(15:0)
Reg012C_in(15:0)
Reg0130_in(15:0)
Reg0134_in(15:0)
Reg0138_in(15:0)
Reg013C_in(15:0)
LAD_OUT(15:0)
Reg0100(15:0)
Reg0104(15:0)
Reg0108(15:0)
Reg010C(15:0)
Reg0110(15:0)
Reg0114(15:0)
Reg0118(15:0)
Reg011C(15:0)
Reg0120(15:0)
Reg0124(15:0)
Reg0128(15:0)
Reg012C(15:0)
Reg0130(15:0)
Reg0134(15:0)
Reg0138(15:0)
Reg013C(15:0)
LAD_OUT(15:0)
FPIX1_A_Interface(15:0)
FPIX1_B_Interface(15:0)
datamanager
Trigger_Data(31:0)
Trigger_WR_Data
DataLatchCLK_A
INV
A_Data(31:0)
A_WR_Data
DataLatchCLK_A
B_Data(31:0)
B_WR_Data
DataLatchCLK_B
ReadoutCLKx2
Rcvr_Reset
Trigger_Data(31:0)
Trigger_WR
Trigger_WRClk
PlaneA_Data(31:0)
PlaneA_WR
PlaneA_WRClk
PlaneB_Data(31:0)
PlaneB_WR
PlaneB_WRClk
DataManagerSM_Clk
Clear_FIFO
PTA_Data_WR
PTA_Data(31:0)
Trigger_FIFO_Empty
Trigger_RD
PlaneA_FIFO_Empty
PlaneA_RD
PlaneB_FIFO_Empty
PlaneB_RD
CurrentState(2:0)
Real_Data_Out(31:0)
FD
D
Q
C
RealData_Valid
ReadoutCLKx2
INV
XILINX
Title: PMC top level. Data Managers.
Name: Bradley Hall - FPIX1 Test Beam 2002
Date: March 10, 2003
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