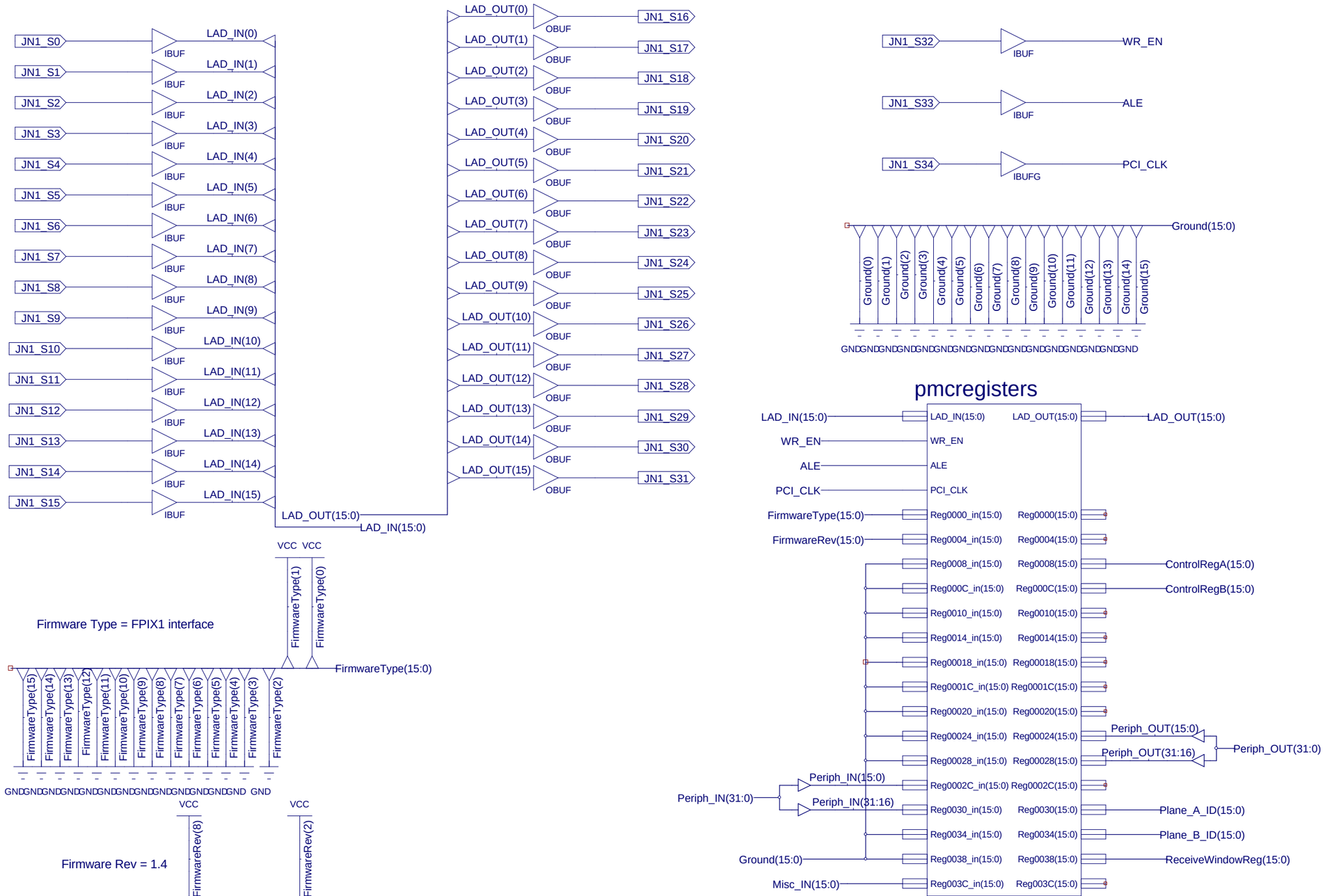
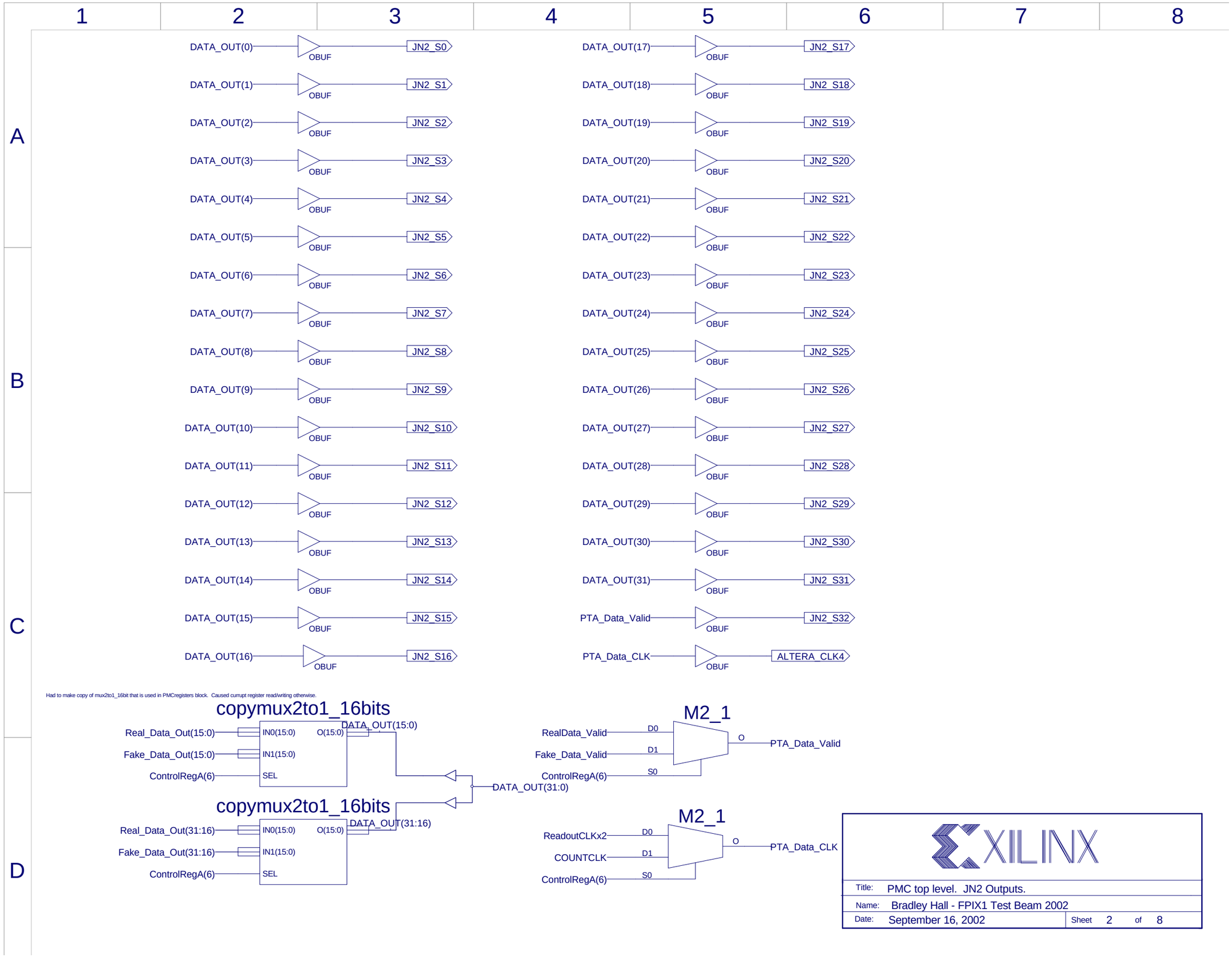
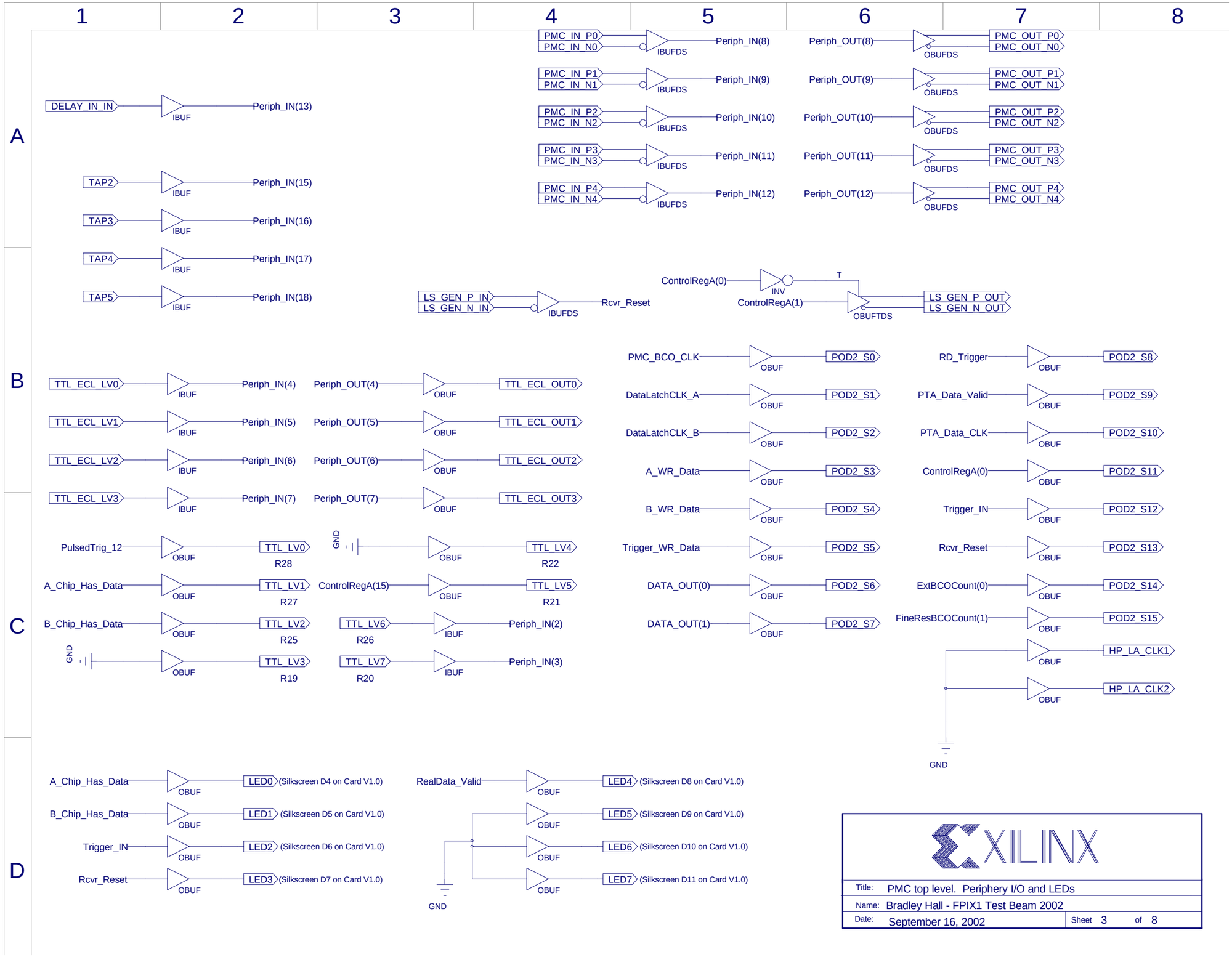
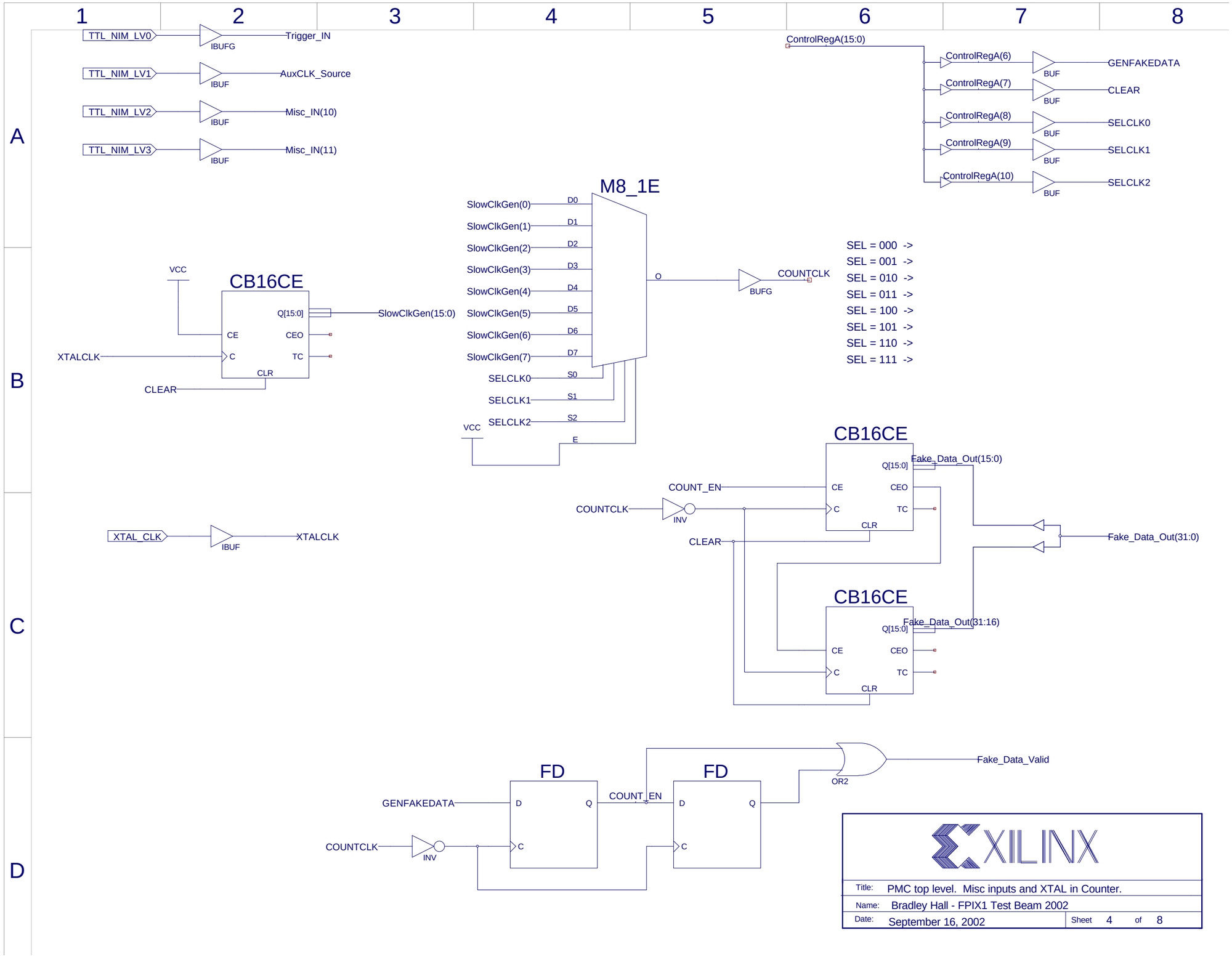
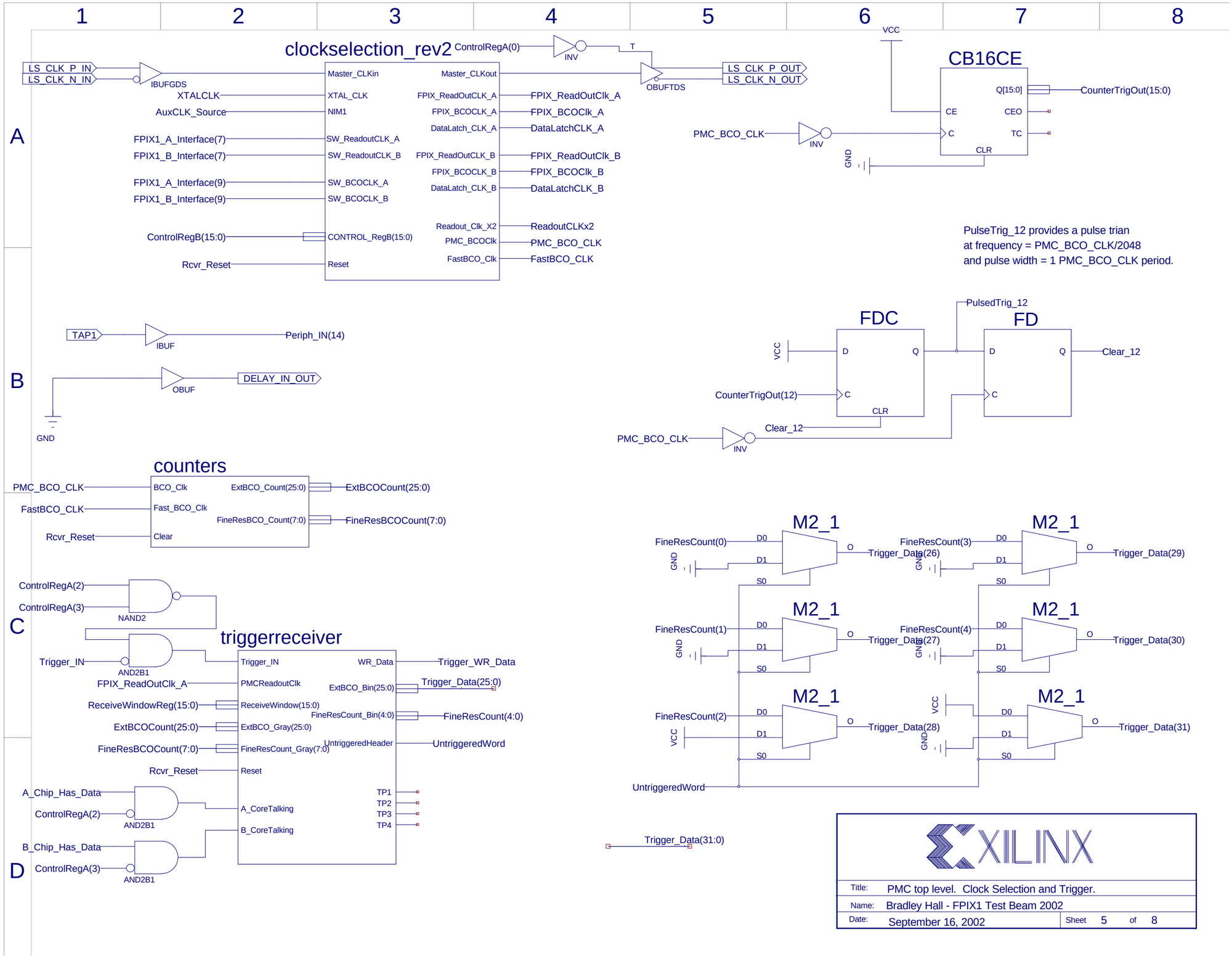
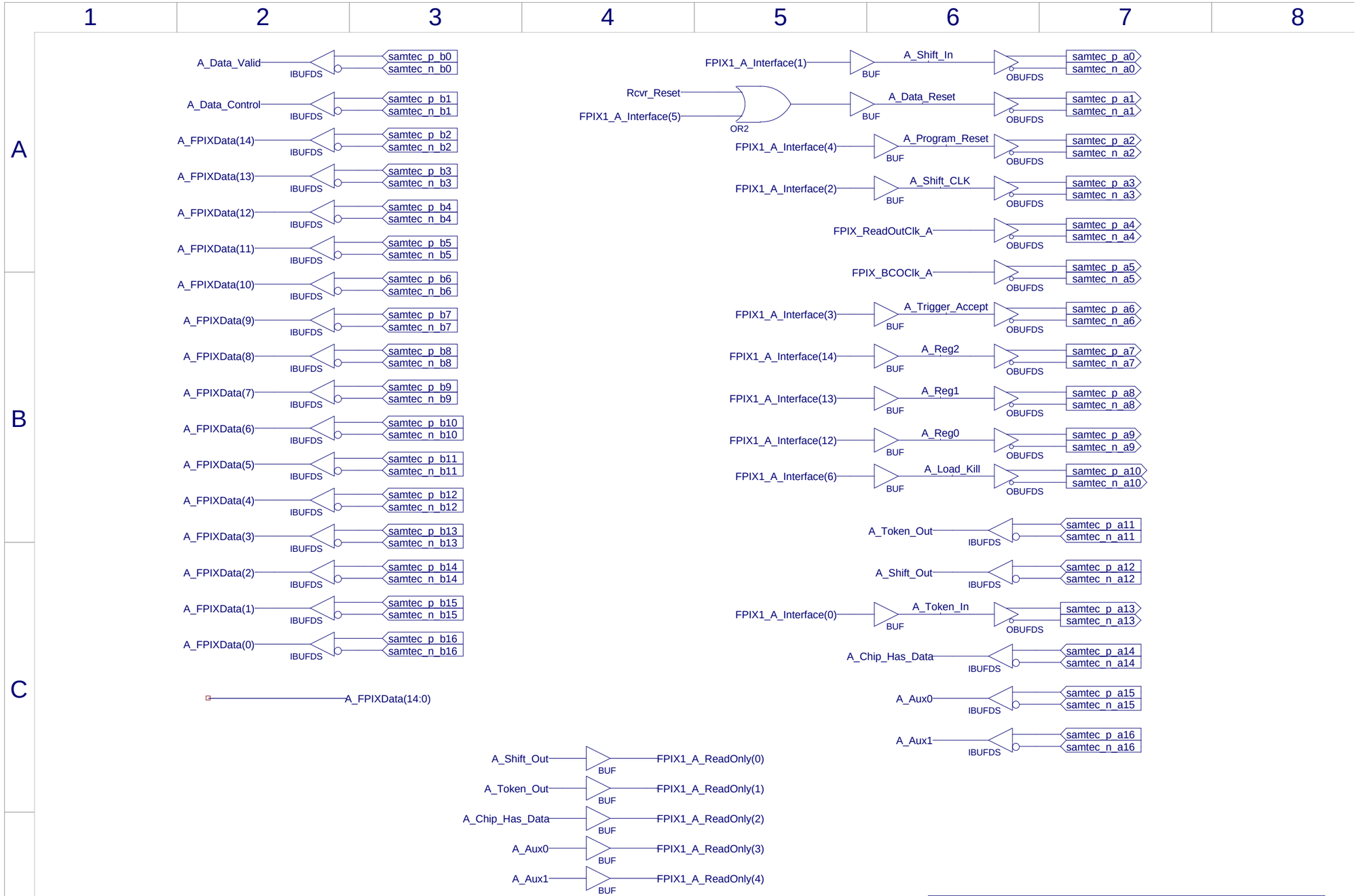

JN1_S0
JN1_S1
JN1_S2
JN1_S3
JN1_S4
JN1_S5
JN1_S6
JN1_S7
JN1_S8
JN1_S9
JN1_S10
JN1_S11
JN1_S12
JN1_S13
JN1_S14
JN1_S15
IBUF
LAD_IN(0)
LAD_IN(1)
LAD_IN(2)
LAD_IN(3)
LAD_IN(4)
LAD_IN(5)
LAD_IN(6)
LAD_IN(7)
LAD_IN(8)
LAD_IN(9)
LAD_IN(10)
LAD_IN(11)
LAD_IN(12)
LAD_IN(13)
LAD_IN(14)
LAD_IN(15)
LAD_OUT(15:0)
LAD_IN(15:0)
OBUF
LAD_OUT(0)
LAD_OUT(1)
LAD_OUT(2)
LAD_OUT(3)
LAD_OUT(4)
LAD_OUT(5)
LAD_OUT(6)
LAD_OUT(7)
LAD_OUT(8)
LAD_OUT(9)
LAD_OUT(10)
LAD_OUT(11)
LAD_OUT(12)
LAD_OUT(13)
LAD_OUT(14)
LAD_OUT(15)
JN1_S16
JN1_S17
JN1_S18
JN1_S19
JN1_S20
JN1_S21
JN1_S22
JN1_S23
JN1_S24
JN1_S25
JN1_S26
JN1_S27
JN1_S28
JN1_S29
JN1_S30
JN1_S31
JN1_S32
JN1_S33
JN1_S34
IBUFG
WR_EN
ALE
PCI_CLK
Ground(15:0)
Ground(0)
Ground(1)
Ground(2)
Ground(3)
Ground(4)
Ground(5)
Ground(6)
Ground(7)
Ground(8)
Ground(9)
Ground(10)
Ground(11)
Ground(12)
Ground(13)
Ground(14)
Ground(15)
GND
pmcregisters
LAD_IN(15:0)
WR_EN
ALE
PCI_CLK
FirmwareType(15:0)
FirmwareRev(15:0)
Misc_IN(15:0)
Ground(15:0)
Periph_IN(31:0)
Periph_IN(15:0)
Periph_IN(31:16)
LAD_OUT(15:0)
Reg0000_in(15:0)
Reg0000(15:0)
Reg0004_in(15:0)
Reg0004(15:0)
Reg0008_in(15:0)
Reg0008(15:0)
Reg000C_in(15:0)
Reg000C(15:0)
Reg0010_in(15:0)
Reg0010(15:0)
Reg0014_in(15:0)
Reg0014(15:0)
Reg00018_in(15:0)
Reg00018(15:0)
Reg0001C_in(15:0)
Reg0001C(15:0)
Reg00020_in(15:0)
Reg00020(15:0)
Reg00024_in(15:0)
Reg00024(15:0)
Reg00028_in(15:0)
Reg00028(15:0)
Reg0002C_in(15:0)
Reg0002C(15:0)
Reg0030_in(15:0)
Reg0030(15:0)
Reg0034_in(15:0)
Reg0034(15:0)
Reg0038_in(15:0)
Reg0038(15:0)
Reg003C_in(15:0)
Reg003C(15:0)
LAD_OUT(15:0)
ControlRegA(15:0)
ControlRegB(15:0)
Periph_OUT(15:0)
Periph_OUT(31:16)
Periph_OUT(31:0)
Plane_A_ID(15:0)
Plane_B_ID(15:0)
ReceiveWindowReg(15:0)
VCC
Firmware Type = FPIX1 interface
FirmwareType(1)
FirmwareType(0)
FirmwareType(15:0)
FirmwareType(15)
FirmwareType(14)
FirmwareType(13)
FirmwareType(12)
FirmwareType(11)
FirmwareType(10)
FirmwareType(9)
FirmwareType(8)
FirmwareType(7)
FirmwareType(6)
FirmwareType(5)
FirmwareType(4)
FirmwareType(3)
FirmwareType(2)
Firmware Rev = 1.4
FirmwareRev(8)
FirmwareRev(2)
FirmwareRev(15:0)
FirmwareRev(15)
FirmwareRev(14)
FirmwareRev(13)
FirmwareRev(12)
FirmwareRev(11)
FirmwareRev(10)
FirmwareRev(9)
FirmwareRev(7)
FirmwareRev(6)
FirmwareRev(5)
FirmwareRev(4)
FirmwareRev(3)
FirmwareRev(1)
FirmwareRev(0)
XILINX
Title: PMC top level. JN1 I/O and Registers.
Name: Bradley Hall - FPIX1 Test Beam 2002
Date: September 16, 2002
Sheet 1 of 8


DATA_OUT(0) OBUF JN2_S0
DATA_OUT(1) OBUF JN2_S1
DATA_OUT(2) OBUF JN2_S2
DATA_OUT(3) OBUF JN2_S3
DATA_OUT(4) OBUF JN2_S4
DATA_OUT(5) OBUF JN2_S5
DATA_OUT(6) OBUF JN2_S6
DATA_OUT(7) OBUF JN2_S7
DATA_OUT(8) OBUF JN2_S8
DATA_OUT(9) OBUF JN2_S9
DATA_OUT(10) OBUF JN2_S10
DATA_OUT(11) OBUF JN2_S11
DATA_OUT(12) OBUF JN2_S12
DATA_OUT(13) OBUF JN2_S13
DATA_OUT(14) OBUF JN2_S14
DATA_OUT(15) OBUF JN2_S15
DATA_OUT(16) OBUF JN2_S16
DATA_OUT(17) OBUF JN2_S17
DATA_OUT(18) OBUF JN2_S18
DATA_OUT(19) OBUF JN2_S19
DATA_OUT(20) OBUF JN2_S20
DATA_OUT(21) OBUF JN2_S21
DATA_OUT(22) OBUF JN2_S22
DATA_OUT(23) OBUF JN2_S23
DATA_OUT(24) OBUF JN2_S24
DATA_OUT(25) OBUF JN2_S25
DATA_OUT(26) OBUF JN2_S26
DATA_OUT(27) OBUF JN2_S27
DATA_OUT(28) OBUF JN2_S28
DATA_OUT(29) OBUF JN2_S29
DATA_OUT(30) OBUF JN2_S30
DATA_OUT(31) OBUF JN2_S31
PTA_Data_Valid OBUF JN2_S32
PTA_Data_CLK OBUF ALTERA_CLK4
Had to make copy of mux2to1_16bit that is used in PMCregisters block. Caused currupt register read/writing otherwise.
copymux2to1_16bits
Real_Data_Out(15:0)
Fake_Data_Out(15:0)
ControlRegA(6)
IN0(15:0)
IN1(15:0)
SEL
O(15:0)
DATA_OUT(15:0)
copymux2to1_16bits
Real_Data_Out(31:16)
Fake_Data_Out(31:16)
ControlRegA(6)
IN0(15:0)
IN1(15:0)
SEL
O(15:0)
DATA_OUT(31:16)
DATA_OUT(31:0)
M2_1
RealData_Valid D0
Fake_Data_Valid D1
ControlRegA(6) S0
O
PTA_Data_Valid
M2_1
ReadoutCLKx2 D0
COUNTCLK D1
ControlRegA(6) S0
O
PTA_Data_CLK
XILINX
Title: PMC top level. JN2 Outputs.
Name: Bradley Hall - FPIX1 Test Beam 2002
Date: September 16, 2002
Sheet 2 of 8


1
2
3
4
5
6
7
8
A
B
C
D
PMC_IN_P0
PMC_IN_N0
IBUFDS
Periph_IN(8)
Periph_OUT(8)
OBUFDS
PMC_OUT_P0
PMC_OUT_N0
PMC_IN_P1
PMC_IN_N1
Periph_IN(9)
Periph_OUT(9)
PMC_OUT_P1
PMC_OUT_N1
DELAY_IN_IN
IBUF
Periph_IN(13)
PMC_IN_P2
PMC_IN_N2
Periph_IN(10)
Periph_OUT(10)
PMC_OUT_P2
PMC_OUT_N2
PMC_IN_P3
PMC_IN_N3
Periph_IN(11)
Periph_OUT(11)
PMC_OUT_P3
PMC_OUT_N3
TAP2
Periph_IN(15)
PMC_IN_P4
PMC_IN_N4
Periph_IN(12)
Periph_OUT(12)
PMC_OUT_P4
PMC_OUT_N4
TAP3
Periph_IN(16)
TAP4
Periph_IN(17)
TAP5
Periph_IN(18)
ControlRegA(0)
INV
T
LS_GEN_P_IN
LS_GEN_N_IN
Rcvr_Reset
ControlRegA(1)
OBUFTDS
LS_GEN_P_OUT
LS_GEN_N_OUT
PMC_BCO_CLK
POD2_S0
RD_Trigger
POD2_S8
TTL_ECL_LV0
Periph_IN(4)
Periph_OUT(4)
TTL_ECL_OUT0
DataLatchCLK_A
POD2_S1
PTA_Data_Valid
POD2_S9
TTL_ECL_LV1
Periph_IN(5)
Periph_OUT(5)
TTL_ECL_OUT1
DataLatchCLK_B
POD2_S2
PTA_Data_CLK
POD2_S10
TTL_ECL_LV2
Periph_IN(6)
Periph_OUT(6)
TTL_ECL_OUT2
A_WR_Data
POD2_S3
ControlRegA(0)
POD2_S11
TTL_ECL_LV3
Periph_IN(7)
Periph_OUT(7)
TTL_ECL_OUT3
B_WR_Data
POD2_S4
Trigger_IN
POD2_S12
PulsedTrig_12
TTL_LV0
R28
GND
TTL_LV4
R22
Trigger_WR_Data
POD2_S5
Rcvr_Reset
POD2_S13
A_Chip_Has_Data
TTL_LV1
R27
ControlRegA(15)
TTL_LV5
R21
DATA_OUT(0)
POD2_S6
ExtBCOCount(0)
POD2_S14
B_Chip_Has_Data
TTL_LV2
R25
TTL_LV6
R26
Periph_IN(2)
DATA_OUT(1)
POD2_S7
FineResBCOCount(1)
POD2_S15
GND
TTL_LV3
R19
TTL_LV7
R20
Periph_IN(3)
HP_LA_CLK1
HP_LA_CLK2
GND
A_Chip_Has_Data
LED0
(Silkscreen D4 on Card V1.0)
RealData_Valid
LED4
(Silkscreen D8 on Card V1.0)
B_Chip_Has_Data
LED1
(Silkscreen D5 on Card V1.0)
LED5
(Silkscreen D9 on Card V1.0)
Trigger_IN
LED2
(Silkscreen D6 on Card V1.0)
LED6
(Silkscreen D10 on Card V1.0)
Rcvr_Reset
LED3
(Silkscreen D7 on Card V1.0)
LED7
(Silkscreen D11 on Card V1.0)
GND
XILINX
Title: PMC top level. Periphery I/O and LEDs
Name: Bradley Hall - FPIX1 Test Beam 2002
Date: September 16, 2002
Sheet 3 of 8

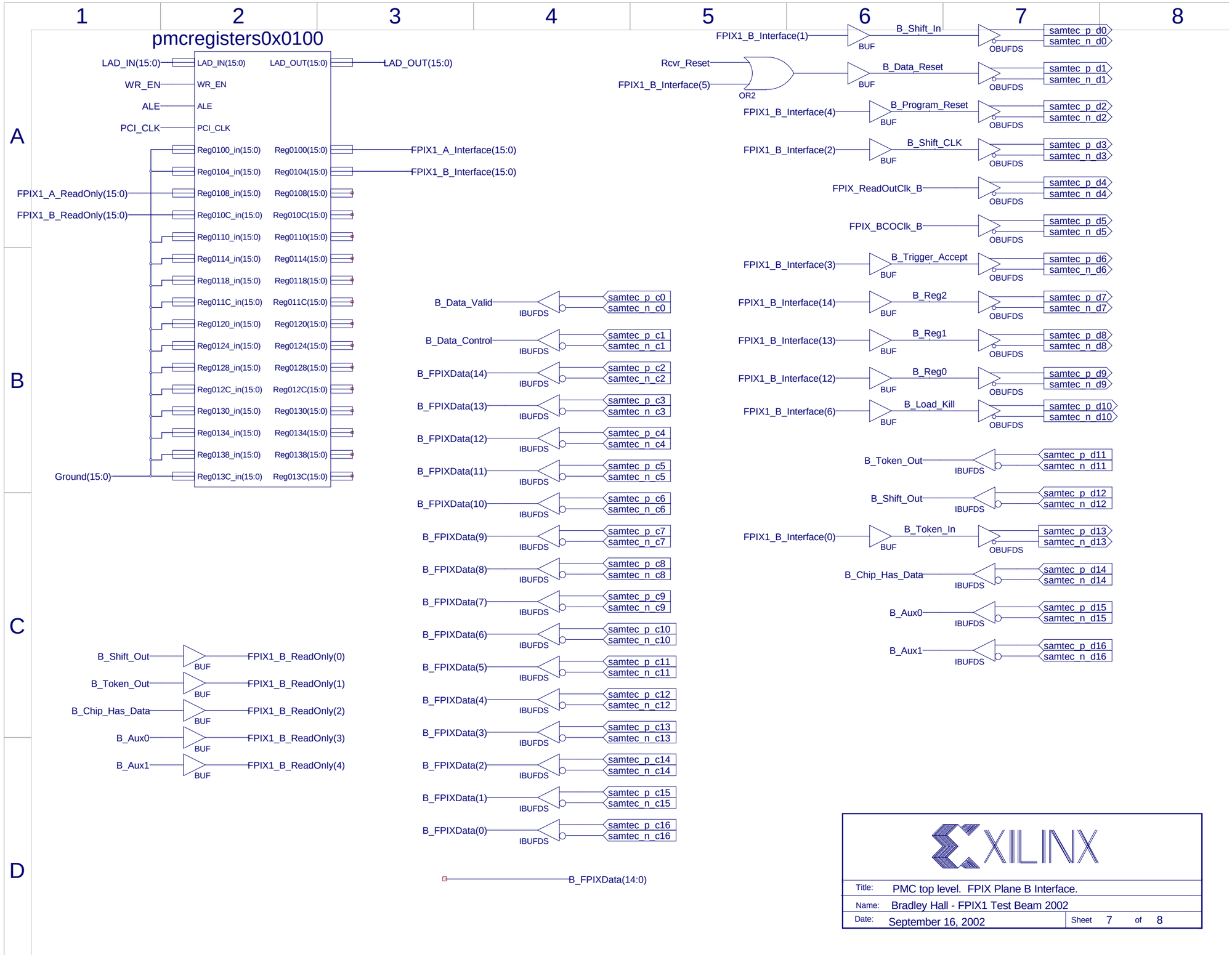

1
2
3
4
5
6
7
8
A
B
C
D
TTL_NIM_LV0
IBUFG
Trigger_IN
TTL_NIM_LV1
IBUF
AuxCLK_Source
TTL_NIM_LV2
IBUF
Misc_IN(10)
TTL_NIM_LV3
IBUF
Misc_IN(11)
ControlRegA(15:0)
ControlRegA(6)
BUF
GENFAKEDATA
ControlRegA(7)
BUF
CLEAR
ControlRegA(8)
BUF
SELCLK0
ControlRegA(9)
BUF
SELCLK1
ControlRegA(10)
BUF
SELCLK2
M8_1E
SlowClkGen(0)
D0
SlowClkGen(1)
D1
SlowClkGen(2)
D2
SlowClkGen(3)
D3
SlowClkGen(4)
D4
SlowClkGen(5)
D5
SlowClkGen(6)
D6
SlowClkGen(7)
D7
SELCLK0
S0
SELCLK1
S1
SELCLK2
S2
VCC
E
O
BUFG
COUNTCLK
SEL = 000 ->
SEL = 001 ->
SEL = 010 ->
SEL = 011 ->
SEL = 100 ->
SEL = 101 ->
SEL = 110 ->
SEL = 111 ->
VCC
CB16CE
Q[15:0]
SlowClkGen(15:0)
CE
CEO
XTALCLK
C
TC
CLR
CLEAR
CB16CE
Fake_Data_Out(15:0)
Q[15:0]
COUNT_EN
CE
CEO
COUNTCLK
INV
C
TC
CLR
CLEAR
Fake_Data_Out(31:0)
XTAL_CLK
IBUF
XTALCLK
CB16CE
Fake_Data_Out(31:16)
Q[15:0]
CE
CEO
C
TC
CLR
FD
FD
GENFAKEDATA
D
Q
COUNT_EN
D
Q
COUNTCLK
INV
C
C
OR2
Fake_Data_Valid
XILINX
Title: PMC top level. Misc inputs and XTAL in Counter.
Name: Bradley Hall - FPIX1 Test Beam 2002
Date: September 16, 2002
Sheet 4 of 8


1
2
3
4
5
6
7
8
A
B
C
D
clockselection_rev2
LS_CLK_P_IN
LS_CLK_N_IN
IBUFGDS
XTALCLK
AuxCLK_Source
FPIX1_A_Interface(7)
FPIX1_B_Interface(7)
FPIX1_A_Interface(9)
FPIX1_B_Interface(9)
ControlRegB(15:0)
Rcvr_Reset
Master_CLKin
XTAL_CLK
NIM1
SW_ReadoutCLK_A
SW_ReadoutCLK_B
SW_BCOCLK_A
SW_BCOCLK_B
CONTROL_RegB(15:0)
Reset
Master_CLKout
FPIX_ReadOutCLK_A
FPIX_BCOCLK_A
DataLatch_CLK_A
FPIX_ReadOutCLK_B
FPIX_BCOCLK_B
DataLatch_CLK_B
Readout_Clk_X2
PMC_BCOClk
FastBCO_Clk
ControlRegA(0)
INV
T
OBUFTDS
LS_CLK_P_OUT
LS_CLK_N_OUT
FPIX_ReadOutClk_A
FPIX_BCOClk_A
DataLatchCLK_A
FPIX_ReadOutClk_B
FPIX_BCOClk_B
DataLatchCLK_B
ReadoutCLKx2
PMC_BCO_CLK
FastBCO_CLK
VCC
CB16CE
Q[15:0]
CE
CEO
C
TC
CLR
CounterTrigOut(15:0)
PMC_BCO_CLK
INV
GND
PulseTrig_12 provides a pulse trian
at frequency = PMC_BCO_CLK/2048
and pulse width = 1 PMC_BCO_CLK period.
TAP1
IBUF
Periph_IN(14)
OBUF
DELAY_IN_OUT
GND
FDC
FD
PulsedTrig_12
VCC
D
Q
C
CLR
CounterTrigOut(12)
Clear_12
PMC_BCO_CLK
INV
counters
PMC_BCO_CLK
FastBCO_CLK
Rcvr_Reset
BCO_Clk
Fast_BCO_Clk
Clear
ExtBCO_Count(25:0)
FineResBCO_Count(7:0)
ExtBCOCount(25:0)
FineResBCOCount(7:0)
ControlRegA(2)
ControlRegA(3)
NAND2
Trigger_IN
AND2B1
triggerreceiver
FPIX_ReadOutClk_A
ReceiveWindowReg(15:0)
ExtBCOCount(25:0)
FineResBCOCount(7:0)
Rcvr_Reset
PMCReadoutClk
ReceiveWindow(15:0)
ExtBCO_Gray(25:0)
FineResCount_Gray(7:0)
Reset
WR_Data
ExtBCO_Bin(25:0)
FineResCount_Bin(4:0)
UntriggeredHeader
A_CoreTalking
B_CoreTalking
TP1
TP2
TP3
TP4
Trigger_WR_Data
Trigger_Data(25:0)
FineResCount(4:0)
UntriggeredWord
A_Chip_Has_Data
ControlRegA(2)
B_Chip_Has_Data
ControlRegA(3)
M2_1
FineResCount(0)
FineResCount(1)
FineResCount(2)
FineResCount(3)
FineResCount(4)
D0
D1
S0
O
Trigger_Data(26)
Trigger_Data(27)
Trigger_Data(28)
Trigger_Data(29)
Trigger_Data(30)
Trigger_Data(31)
UntriggeredWord
Trigger_Data(31:0)
XILINX
Title: PMC top level. Clock Selection and Trigger.
Name: Bradley Hall - FPIX1 Test Beam 2002
Date: September 16, 2002
Sheet 5 of 8



XILINX

Title:	PMC top level. FPIX Plane A Interface.
Name:	Bradley Hall - FPIX1 Test Beam 2002
Date:	September 16, 2002
Sheet	6 of 8


1
2
3
4
5
6
7
8
A
B
C
D
pmcregisters0x0100
LAD_IN(15:0)
WR_EN
ALE
PCI_CLK
FPIX1_A_ReadOnly(15:0)
FPIX1_B_ReadOnly(15:0)
Ground(15:0)
LAD_OUT(15:0)
FPIX1_A_Interface(15:0)
FPIX1_B_Interface(15:0)
Reg0100_in(15:0)
Reg0104_in(15:0)
Reg0108_in(15:0)
Reg010C_in(15:0)
Reg0110_in(15:0)
Reg0114_in(15:0)
Reg0118_in(15:0)
Reg011C_in(15:0)
Reg0120_in(15:0)
Reg0124_in(15:0)
Reg0128_in(15:0)
Reg012C_in(15:0)
Reg0130_in(15:0)
Reg0134_in(15:0)
Reg0138_in(15:0)
Reg013C_in(15:0)
Reg0100(15:0)
Reg0104(15:0)
Reg0108(15:0)
Reg010C(15:0)
Reg0110(15:0)
Reg0114(15:0)
Reg0118(15:0)
Reg011C(15:0)
Reg0120(15:0)
Reg0124(15:0)
Reg0128(15:0)
Reg012C(15:0)
Reg0130(15:0)
Reg0134(15:0)
Reg0138(15:0)
Reg013C(15:0)
B_Shift_Out
B_Token_Out
B_Chip_Has_Data
B_Aux0
B_Aux1
BUF
FPIX1_B_ReadOnly(0)
FPIX1_B_ReadOnly(1)
FPIX1_B_ReadOnly(2)
FPIX1_B_ReadOnly(3)
FPIX1_B_ReadOnly(4)
B_Data_Valid
B_Data_Control
B_FPIXData(14)
B_FPIXData(13)
B_FPIXData(12)
B_FPIXData(11)
B_FPIXData(10)
B_FPIXData(9)
B_FPIXData(8)
B_FPIXData(7)
B_FPIXData(6)
B_FPIXData(5)
B_FPIXData(4)
B_FPIXData(3)
B_FPIXData(2)
B_FPIXData(1)
B_FPIXData(0)
IBUFDS
samtec_p_c0
samtec_n_c0
samtec_p_c1
samtec_n_c1
samtec_p_c2
samtec_n_c2
samtec_p_c3
samtec_n_c3
samtec_p_c4
samtec_n_c4
samtec_p_c5
samtec_n_c5
samtec_p_c6
samtec_n_c6
samtec_p_c7
samtec_n_c7
samtec_p_c8
samtec_n_c8
samtec_p_c9
samtec_n_c9
samtec_p_c10
samtec_n_c10
samtec_p_c11
samtec_n_c11
samtec_p_c12
samtec_n_c12
samtec_p_c13
samtec_n_c13
samtec_p_c14
samtec_n_c14
samtec_p_c15
samtec_n_c15
samtec_p_c16
samtec_n_c16
B_FPIXData(14:0)
FPIX1_B_Interface(1)
Rcvr_Reset
FPIX1_B_Interface(5)
OR2
FPIX1_B_Interface(4)
FPIX1_B_Interface(2)
FPIX_ReadOutClk_B
FPIX_BCOClk_B
FPIX1_B_Interface(3)
FPIX1_B_Interface(14)
FPIX1_B_Interface(13)
FPIX1_B_Interface(12)
FPIX1_B_Interface(6)
B_Shift_In
B_Data_Reset
B_Program_Reset
B_Shift_CLK
B_Trigger_Accept
B_Reg2
B_Reg1
B_Reg0
B_Load_Kill
OBUFDS
samtec_p_d0
samtec_n_d0
samtec_p_d1
samtec_n_d1
samtec_p_d2
samtec_n_d2
samtec_p_d3
samtec_n_d3
samtec_p_d4
samtec_n_d4
samtec_p_d5
samtec_n_d5
samtec_p_d6
samtec_n_d6
samtec_p_d7
samtec_n_d7
samtec_p_d8
samtec_n_d8
samtec_p_d9
samtec_n_d9
samtec_p_d10
samtec_n_d10
B_Token_Out
B_Shift_Out
FPIX1_B_Interface(0)
B_Token_In
B_Chip_Has_Data
B_Aux0
B_Aux1
samtec_p_d11
samtec_n_d11
samtec_p_d12
samtec_n_d12
samtec_p_d13
samtec_n_d13
samtec_p_d14
samtec_n_d14
samtec_p_d15
samtec_n_d15
samtec_p_d16
samtec_n_d16
XILINX
Title: PMC top level. FPIX Plane B Interface.
Name: Bradley Hall - FPIX1 Test Beam 2002
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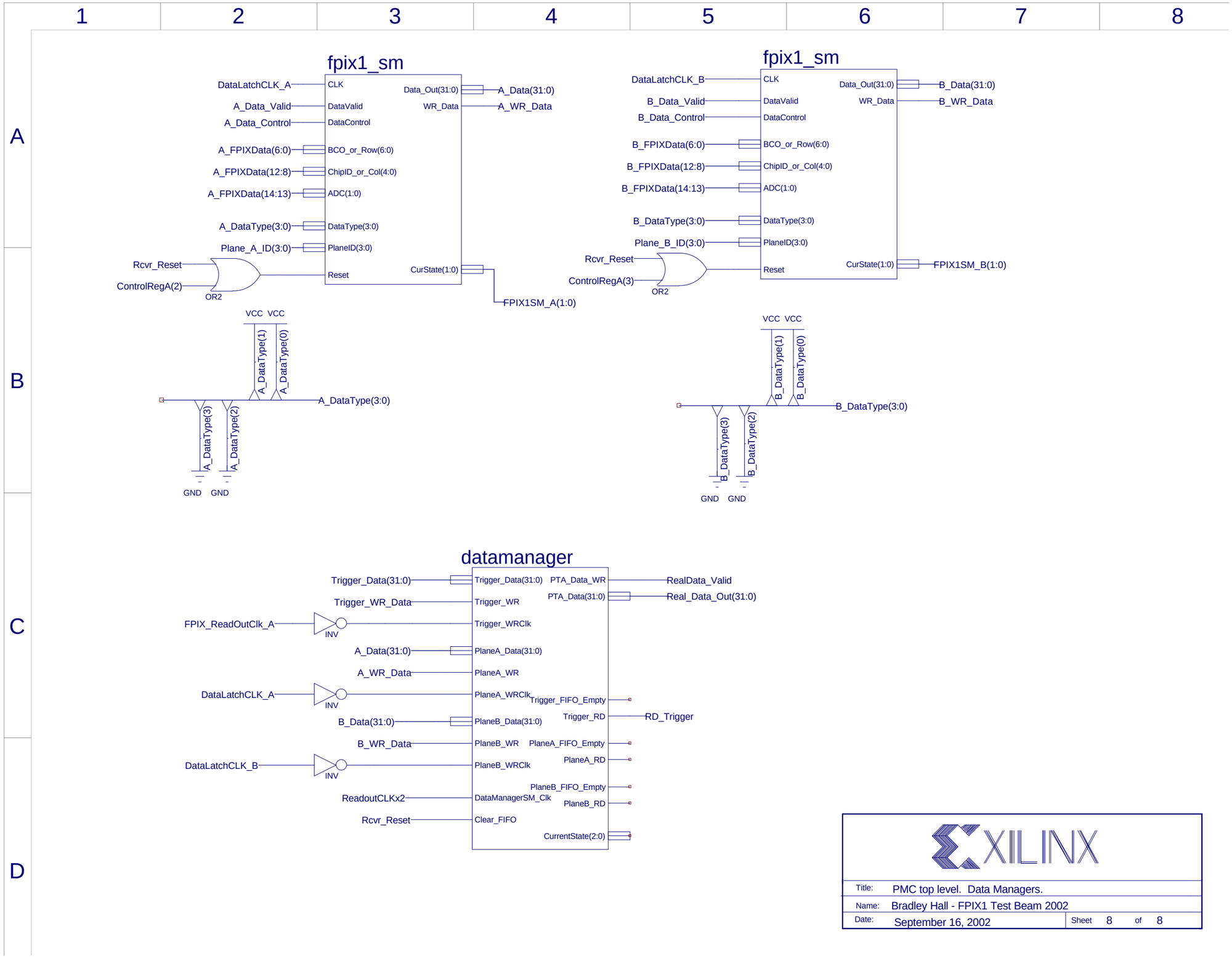
fpix1_sm
DataLatchCLK_A
A_Data_Valid
A_Data_Control
A_FPIXData(6:0)
A_FPIXData(12:8)
A_FPIXData(14:13)
A_DataType(3:0)
Plane_A_ID(3:0)
Rcvr_Reset
ControlRegA(2)
OR2
CLK
DataValid
DataControl
BCO_or_Row(6:0)
ChipID_or_Col(4:0)
ADC(1:0)
DataType(3:0)
PlaneID(3:0)
Reset
Data_Out(31:0)
WR_Data
CurState(1:0)
A_Data(31:0)
A_WR_Data
FPIX1SM_A(1:0)
fpix1_sm
DataLatchCLK_B
B_Data_Valid
B_Data_Control
B_FPIXData(6:0)
B_FPIXData(12:8)
B_FPIXData(14:13)
B_DataType(3:0)
Plane_B_ID(3:0)
Rcvr_Reset
ControlRegA(3)
OR2
CLK
DataValid
DataControl
BCO_or_Row(6:0)
ChipID_or_Col(4:0)
ADC(1:0)
DataType(3:0)
PlaneID(3:0)
Reset
Data_Out(31:0)
WR_Data
CurState(1:0)
B_Data(31:0)
B_WR_Data
FPIX1SM_B(1:0)
VCC VCC
A_DataType(1)
A_DataType(0)
A_DataType(3:0)
A_DataType(3)
A_DataType(2)
GND GND
VCC VCC
B_DataType(1)
B_DataType(0)
B_DataType(3:0)
B_DataType(3)
B_DataType(2)
GND GND
datamanager
Trigger_Data(31:0)
Trigger_WR_Data
FPIX_ReadOutClk_A
INV
A_Data(31:0)
A_WR_Data
DataLatchCLK_A
INV
B_Data(31:0)
B_WR_Data
DataLatchCLK_B
INV
ReadoutCLKx2
Rcvr_Reset
Trigger_Data(31:0)
Trigger_WR
Trigger_WRClk
PlaneA_Data(31:0)
PlaneA_WR
PlaneA_WRClk
PlaneB_Data(31:0)
PlaneB_WR
PlaneB_WRClk
DataManagerSM_Clk
Clear_FIFO
PTA_Data_WR
PTA_Data(31:0)
Trigger_FIFO_Empty
Trigger_RD
PlaneA_FIFO_Empty
PlaneA_RD
PlaneB_FIFO_Empty
PlaneB_RD
CurrentState(2:0)
RealData_Valid
Real_Data_Out(31:0)
RD_Trigger
XILINX
Title: PMC top level. Data Managers.
Name: Bradley Hall - FPIX1 Test Beam 2002
Date: September 16, 2002
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