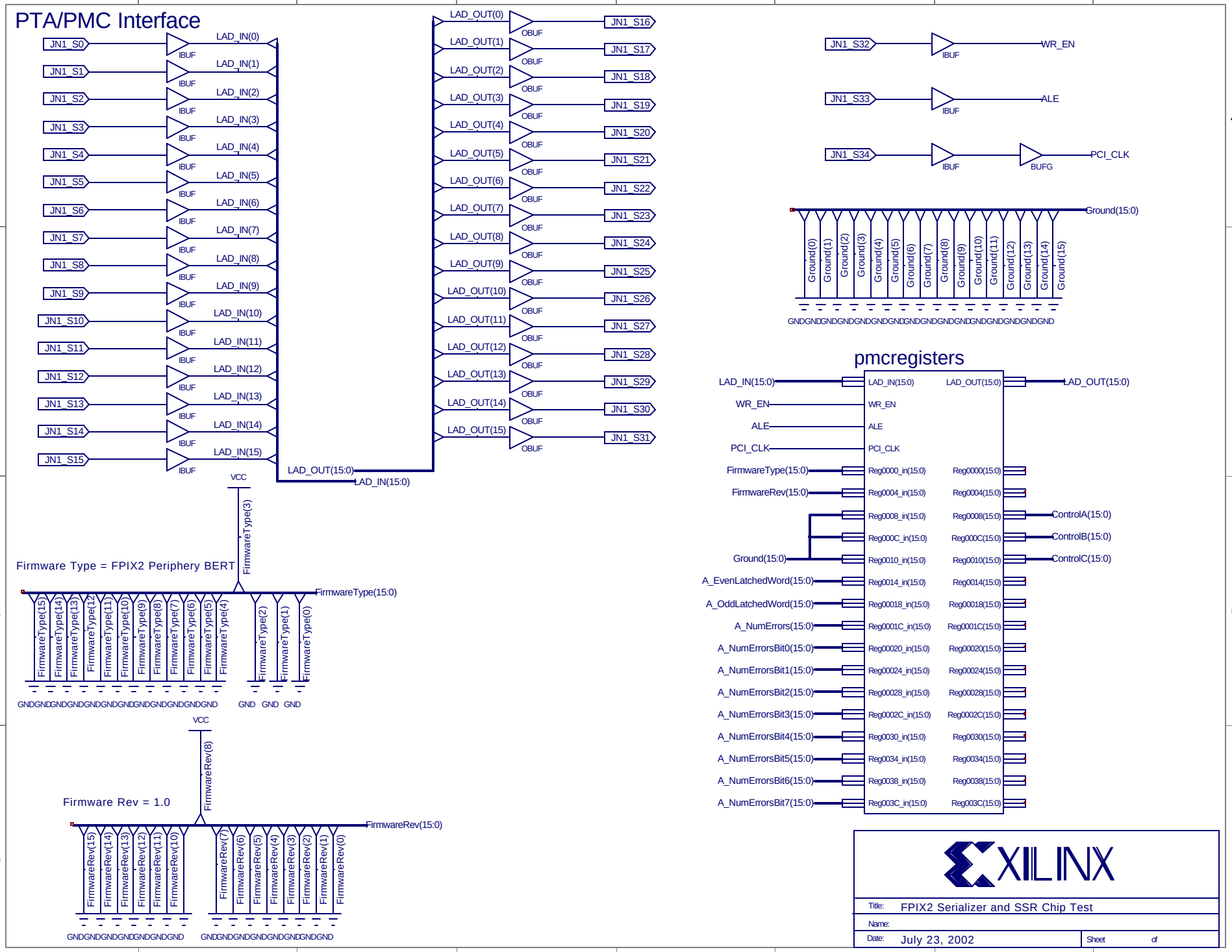
PTA/PMC Interface
JN1_S0
JN1_S1
JN1_S2
JN1_S3
JN1_S4
JN1_S5
JN1_S6
JN1_S7
JN1_S8
JN1_S9
JN1_S10
JN1_S11
JN1_S12
JN1_S13
JN1_S14
JN1_S15
IBUF
LAD_IN(0)
LAD_IN(1)
LAD_IN(2)
LAD_IN(3)
LAD_IN(4)
LAD_IN(5)
LAD_IN(6)
LAD_IN(7)
LAD_IN(8)
LAD_IN(9)
LAD_IN(10)
LAD_IN(11)
LAD_IN(12)
LAD_IN(13)
LAD_IN(14)
LAD_IN(15)
LAD_OUT(15:0)
LAD_IN(15:0)
LAD_OUT(0)
LAD_OUT(1)
LAD_OUT(2)
LAD_OUT(3)
LAD_OUT(4)
LAD_OUT(5)
LAD_OUT(6)
LAD_OUT(7)
LAD_OUT(8)
LAD_OUT(9)
LAD_OUT(10)
LAD_OUT(11)
LAD_OUT(12)
LAD_OUT(13)
LAD_OUT(14)
LAD_OUT(15)
OBUF
JN1_S16
JN1_S17
JN1_S18
JN1_S19
JN1_S20
JN1_S21
JN1_S22
JN1_S23
JN1_S24
JN1_S25
JN1_S26
JN1_S27
JN1_S28
JN1_S29
JN1_S30
JN1_S31
JN1_S32
JN1_S33
JN1_S34
WR_EN
ALE
PCI_CLK
BUFG
Ground(15:0)
Ground(0)
Ground(1)
Ground(2)
Ground(3)
Ground(4)
Ground(5)
Ground(6)
Ground(7)
Ground(8)
Ground(9)
Ground(10)
Ground(11)
Ground(12)
Ground(13)
Ground(14)
Ground(15)
GND
VCC
FirmwareType(3)
Firmware Type = FPIX2 Periphery BERT
FirmwareType(15:0)
FirmwareType(15)
FirmwareType(14)
FirmwareType(13)
FirmwareType(12)
FirmwareType(11)
FirmwareType(10)
FirmwareType(9)
FirmwareType(8)
FirmwareType(7)
FirmwareType(6)
FirmwareType(5)
FirmwareType(4)
FirmwareType(2)
FirmwareType(1)
FirmwareType(0)
FirmwareRev(8)
Firmware Rev = 1.0
FirmwareRev(15:0)
FirmwareRev(15)
FirmwareRev(14)
FirmwareRev(13)
FirmwareRev(12)
FirmwareRev(11)
FirmwareRev(10)
FirmwareRev(7)
FirmwareRev(6)
FirmwareRev(5)
FirmwareRev(4)
FirmwareRev(3)
FirmwareRev(2)
FirmwareRev(1)
FirmwareRev(0)
pmcregisters
LAD_IN(15:0)
WR_EN
ALE
PCI_CLK
FirmwareType(15:0)
FirmwareRev(15:0)
Ground(15:0)
A_EvenLatchedWord(15:0)
A_OddLatchedWord(15:0)
A_NumErrors(15:0)
A_NumErrorsBit0(15:0)
A_NumErrorsBit1(15:0)
A_NumErrorsBit2(15:0)
A_NumErrorsBit3(15:0)
A_NumErrorsBit4(15:0)
A_NumErrorsBit5(15:0)
A_NumErrorsBit6(15:0)
A_NumErrorsBit7(15:0)
Reg0000_in(15:0)
Reg0004_in(15:0)
Reg0008_in(15:0)
Reg000C_in(15:0)
Reg0010_in(15:0)
Reg0014_in(15:0)
Reg00018_in(15:0)
Reg0001C_in(15:0)
Reg00020_in(15:0)
Reg00024_in(15:0)
Reg00028_in(15:0)
Reg0002C_in(15:0)
Reg0030_in(15:0)
Reg0034_in(15:0)
Reg0038_in(15:0)
Reg003C_in(15:0)
Reg0000(15:0)
Reg0004(15:0)
Reg0008(15:0)
Reg000C(15:0)
Reg0010(15:0)
Reg0014(15:0)
Reg00018(15:0)
Reg0001C(15:0)
Reg00020(15:0)
Reg00024(15:0)
Reg00028(15:0)
Reg0002C(15:0)
Reg0030(15:0)
Reg0034(15:0)
Reg0038(15:0)
Reg003C(15:0)
ControlA(15:0)
ControlB(15:0)
ControlC(15:0)
XILINX
Title: FPIX2 Serializer and SSR Chip Test
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Date: July 23, 2002
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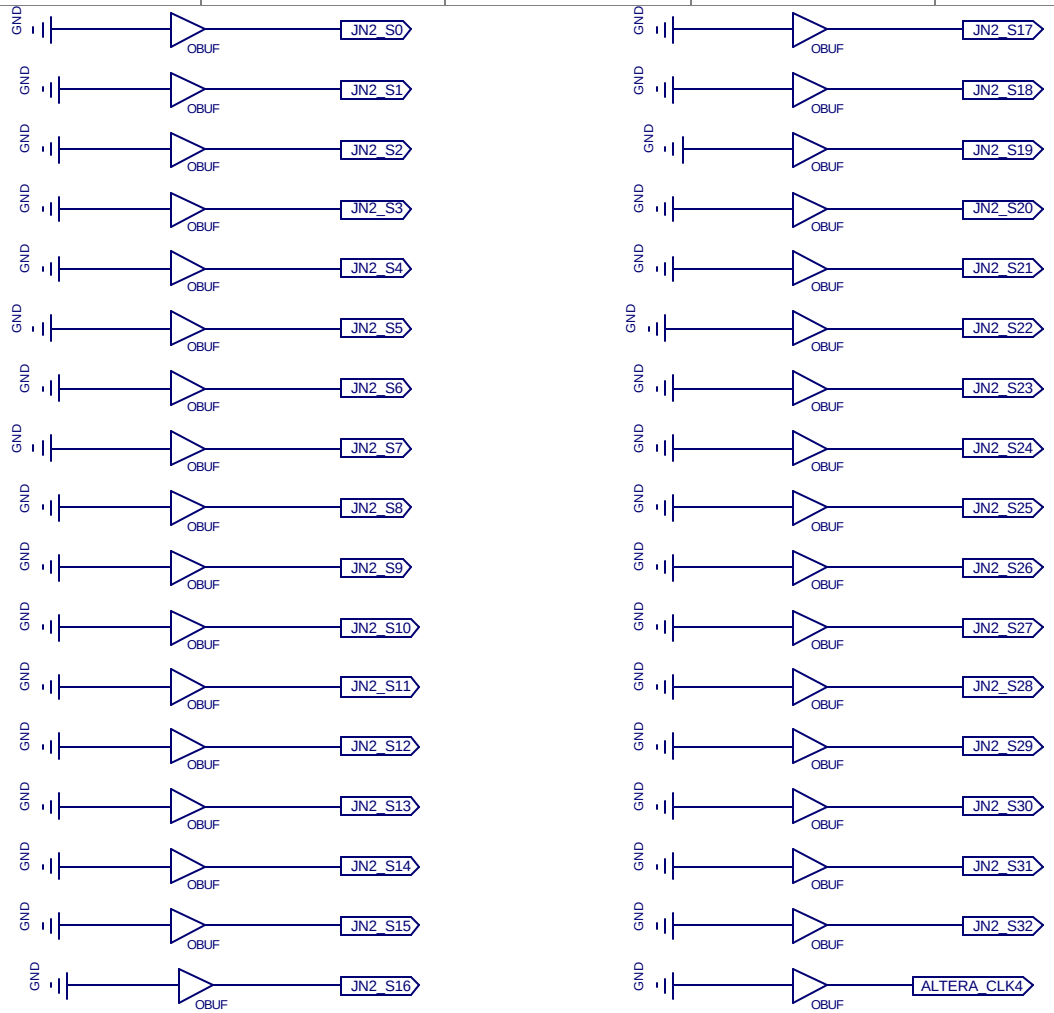
PTA/PMC Interface



XILINX

Title:	FPIX2 Serializer and SSR Chip Test
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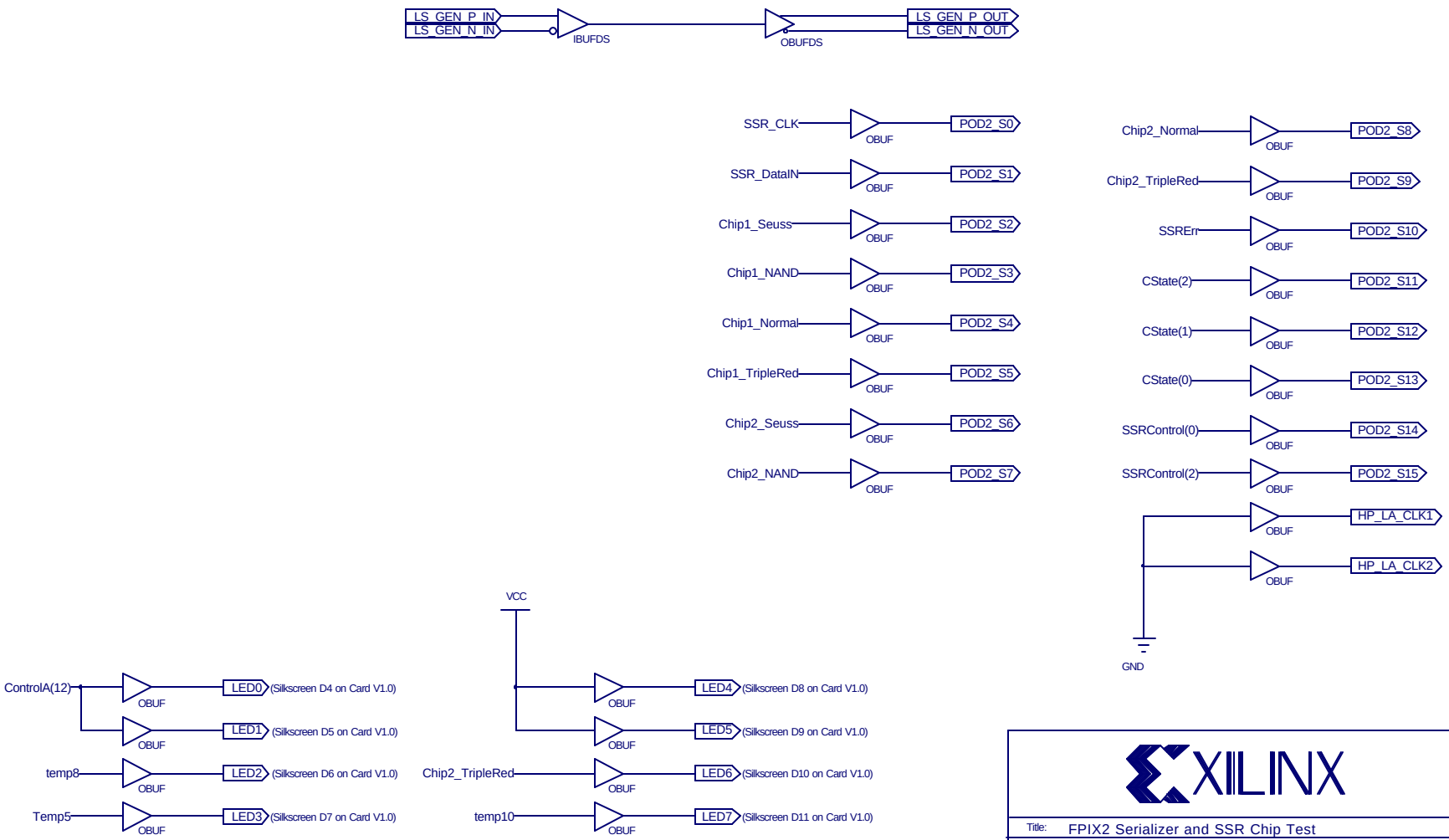
Logic Analyzer and LEDs



XILINX

Title:	FPIX2 Serializer and SSR Chip Test
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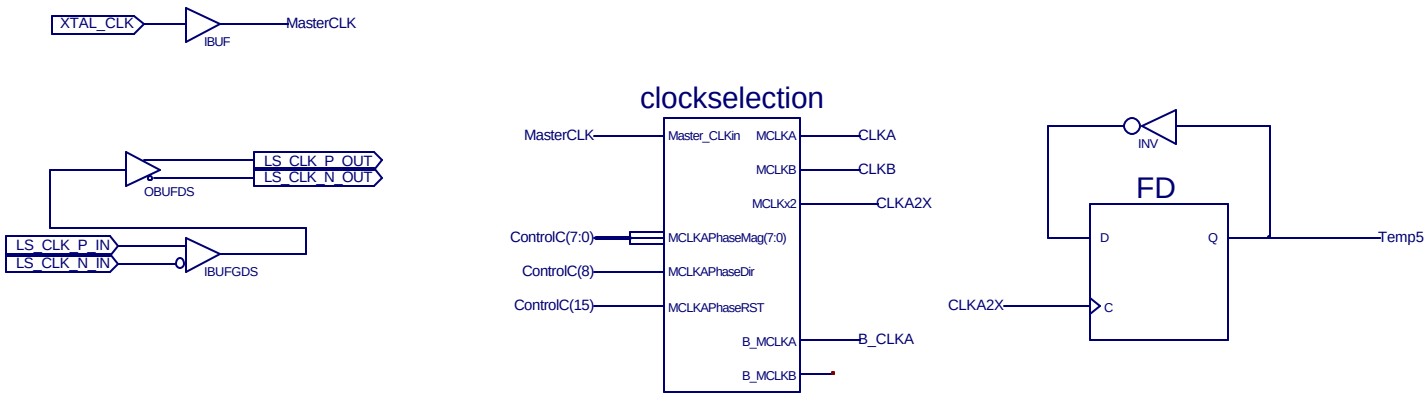
Clocks



XILINX

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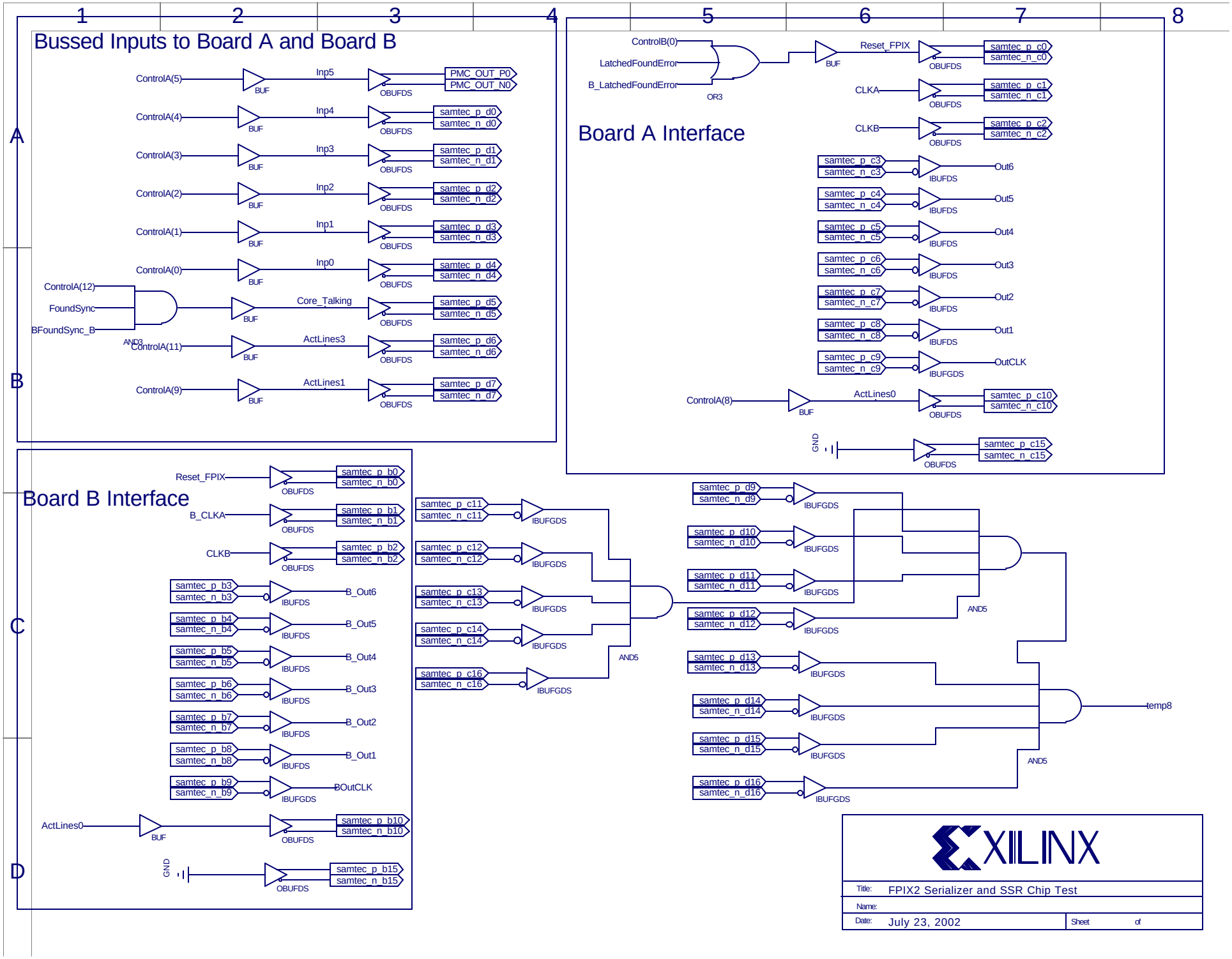
Bussed Inputs to Board A and Board B
ControlA(5)
BUF
Inp5
OBUFDS
PMC_OUT_P0
PMC_OUT_N0
ControlA(4)
Inp4
samtec_p_d0
samtec_n_d0
ControlA(3)
Inp3
samtec_p_d1
samtec_n_d1
ControlA(2)
Inp2
samtec_p_d2
samtec_n_d2
ControlA(1)
Inp1
samtec_p_d3
samtec_n_d3
ControlA(0)
Inp0
samtec_p_d4
samtec_n_d4
ControlA(12)
FoundSync
BFoundSync_B
AND3
Core_Talking
samtec_p_d5
samtec_n_d5
ControlA(11)
ActLines3
samtec_p_d6
samtec_n_d6
ControlA(9)
ActLines1
samtec_p_d7
samtec_n_d7
Board A Interface
ControlB(0)
LatchedFoundError
B_LatchedFoundError
OR3
Reset_FPIX
samtec_p_c0
samtec_n_c0
CLKA
samtec_p_c1
samtec_n_c1
CLKB
samtec_p_c2
samtec_n_c2
samtec_p_c3
samtec_n_c3
IBUFDS
Out6
samtec_p_c4
samtec_n_c4
Out5
samtec_p_c5
samtec_n_c5
Out4
samtec_p_c6
samtec_n_c6
Out3
samtec_p_c7
samtec_n_c7
Out2
samtec_p_c8
samtec_n_c8
Out1
samtec_p_c9
samtec_n_c9
IBUFGDS
OutCLK
ControlA(8)
ActLines0
samtec_p_c10
samtec_n_c10
GND
samtec_p_c15
samtec_n_c15
Board B Interface
Reset_FPIX
samtec_p_b0
samtec_n_b0
B_CLKA
samtec_p_b1
samtec_n_b1
CLKB
samtec_p_b2
samtec_n_b2
samtec_p_b3
samtec_n_b3
B_Out6
samtec_p_b4
samtec_n_b4
B_Out5
samtec_p_b5
samtec_n_b5
B_Out4
samtec_p_b6
samtec_n_b6
B_Out3
samtec_p_b7
samtec_n_b7
B_Out2
samtec_p_b8
samtec_n_b8
B_Out1
samtec_p_b9
samtec_n_b9
BOutCLK
ActLines0
samtec_p_b10
samtec_n_b10
samtec_p_b15
samtec_n_b15
samtec_p_c11
samtec_n_c11
samtec_p_c12
samtec_n_c12
samtec_p_c13
samtec_n_c13
samtec_p_c14
samtec_n_c14
samtec_p_c16
samtec_n_c16
AND5
samtec_p_d9
samtec_n_d9
samtec_p_d10
samtec_n_d10
samtec_p_d11
samtec_n_d11
samtec_p_d12
samtec_n_d12
samtec_p_d13
samtec_n_d13
samtec_p_d14
samtec_n_d14
samtec_p_d15
samtec_n_d15
samtec_p_d16
samtec_n_d16
temp8
XILINX
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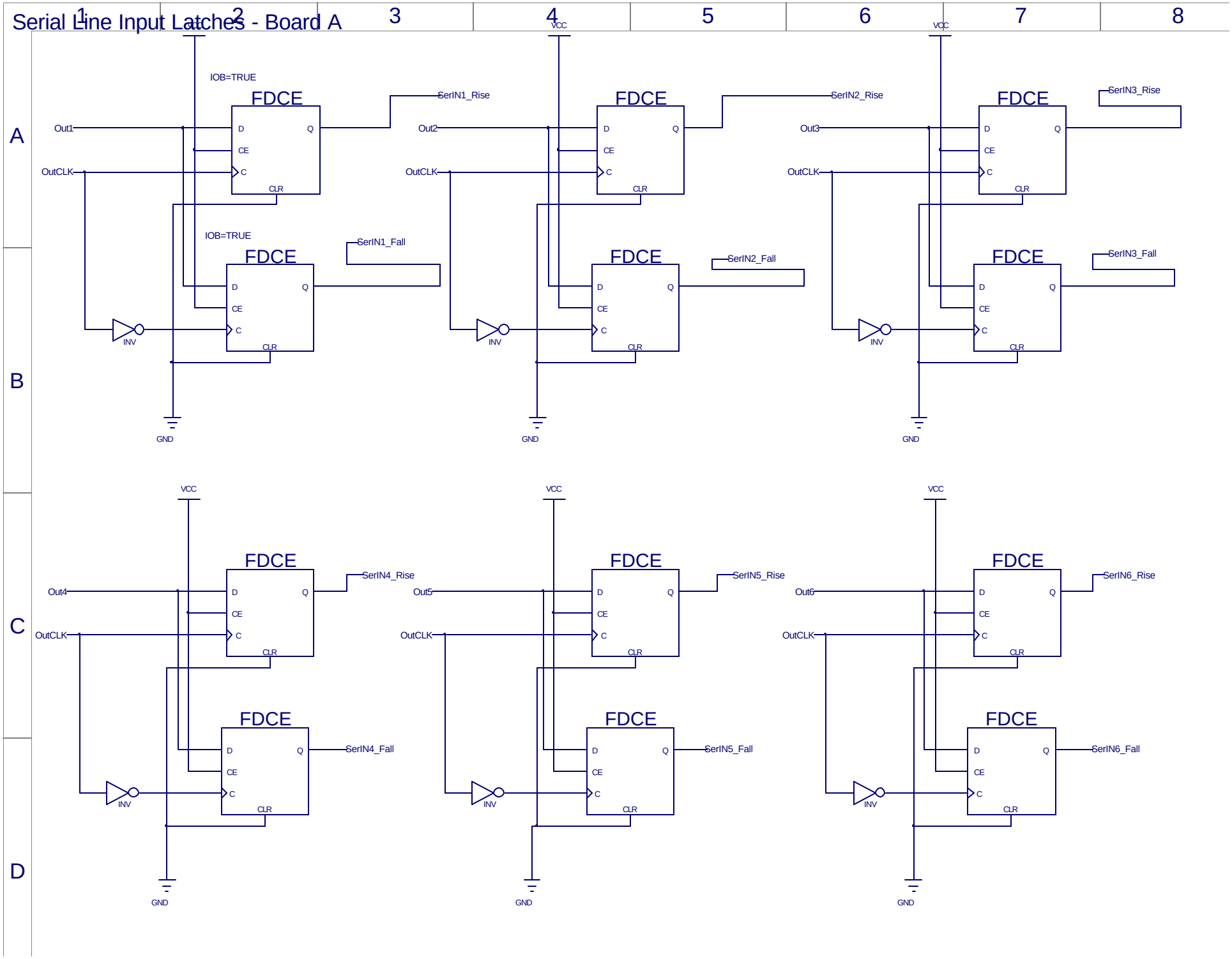
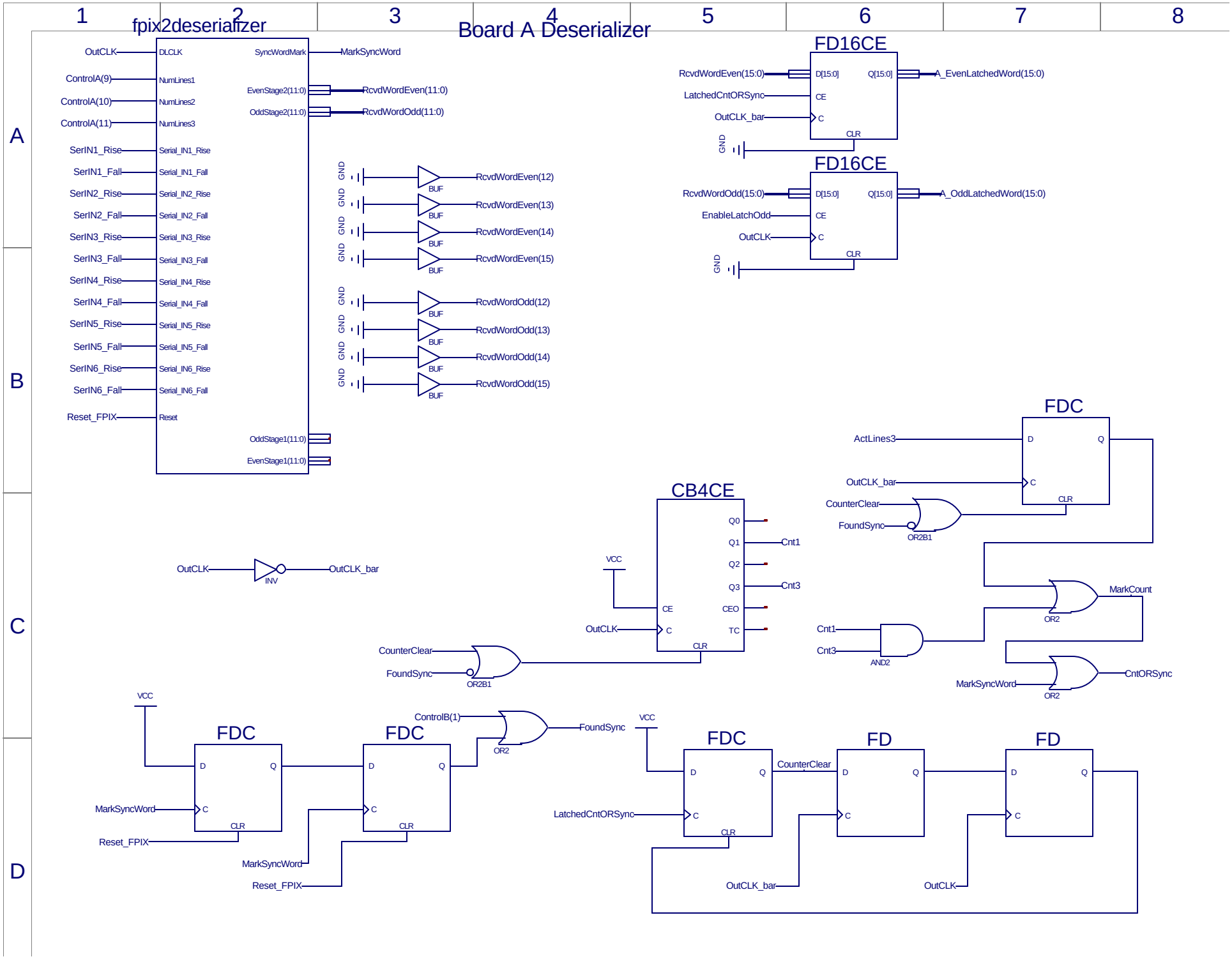
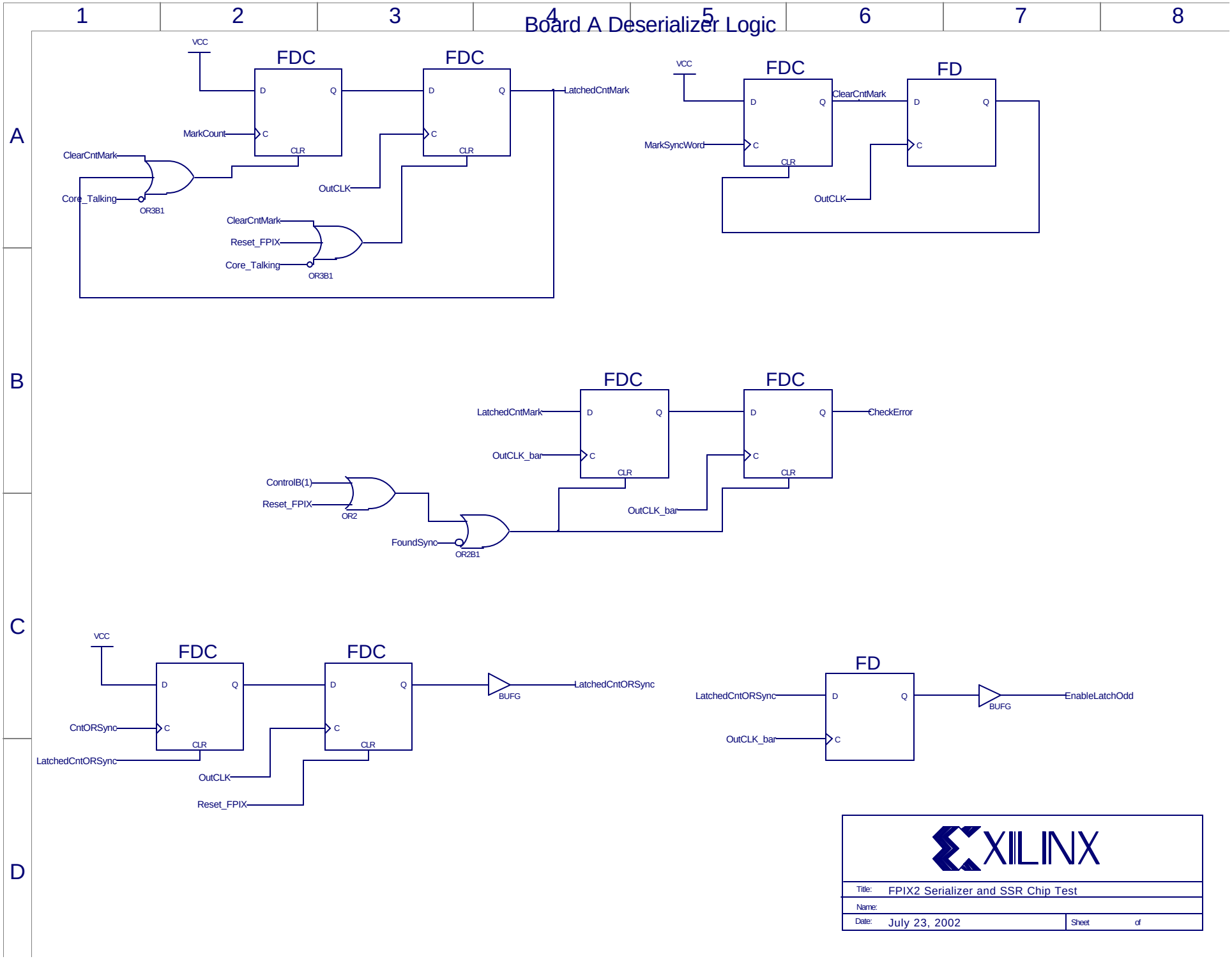
Serial Line Input Latches - Board A




Board A Deserializer
fpix2deserializer
OutCLK
DLCLK
ControlA(9)
NumLines1
ControlA(10)
NumLines2
ControlA(11)
NumLines3
SerIN1_Rise
Serial_IN1_Rise
SerIN1_Fall
Serial_IN1_Fall
SerIN2_Rise
Serial_IN2_Rise
SerIN2_Fall
Serial_IN2_Fall
SerIN3_Rise
Serial_IN3_Rise
SerIN3_Fall
Serial_IN3_Fall
SerIN4_Rise
Serial_IN4_Rise
SerIN4_Fall
Serial_IN4_Fall
SerIN5_Rise
Serial_IN5_Rise
SerIN5_Fall
Serial_IN5_Fall
SerIN6_Rise
Serial_IN6_Rise
SerIN6_Fall
Serial_IN6_Fall
Reset_FPIX
Reset
SyncWordMark
MarkSyncWord
EvenStage2(11:0)
RcvdWordEven(11:0)
OddStage2(11:0)
RcvdWordOdd(11:0)
OddStage1(11:0)
EvenStage1(11:0)
GND
BUF
RcvdWordEven(12)
RcvdWordEven(13)
RcvdWordEven(14)
RcvdWordEven(15)
RcvdWordOdd(12)
RcvdWordOdd(13)
RcvdWordOdd(14)
RcvdWordOdd(15)
FD16CE
RcvdWordEven(15:0)
D[15:0]
Q[15:0]
A_EvenLatchedWord(15:0)
LatchedCntORSync
CE
OutCLK_bar
C
CLR
FD16CE
RcvdWordOdd(15:0)
A_OddLatchedWord(15:0)
EnableLatchOdd
OutCLK
FDC
ActLines3
D
Q
OutCLK_bar
C
CLR
CounterClear
FoundSync
OR2B1
OutCLK
INV
OutCLK_bar
CB4CE
VCC
Q0
Q1
Cnt1
Q2
Q3
Cnt3
CE
CEO
OutCLK
C
TC
CLR
CounterClear
FoundSync
OR2B1
MarkCount
OR2
Cnt1
Cnt3
AND2
MarkSyncWord
OR2
CntORSync
VCC
FDC
D
Q
MarkSyncWord
C
CLR
Reset_FPIX
FDC
D
Q
C
CLR
MarkSyncWord
Reset_FPIX
ControlB(1)
OR2
FoundSync
VCC
FDC
D
Q
LatchedCntORSync
C
CLR
CounterClear
FD
D
Q
C
OutCLK_bar
FD
D
Q
C
OutCLK

Board A Deserializer Logic



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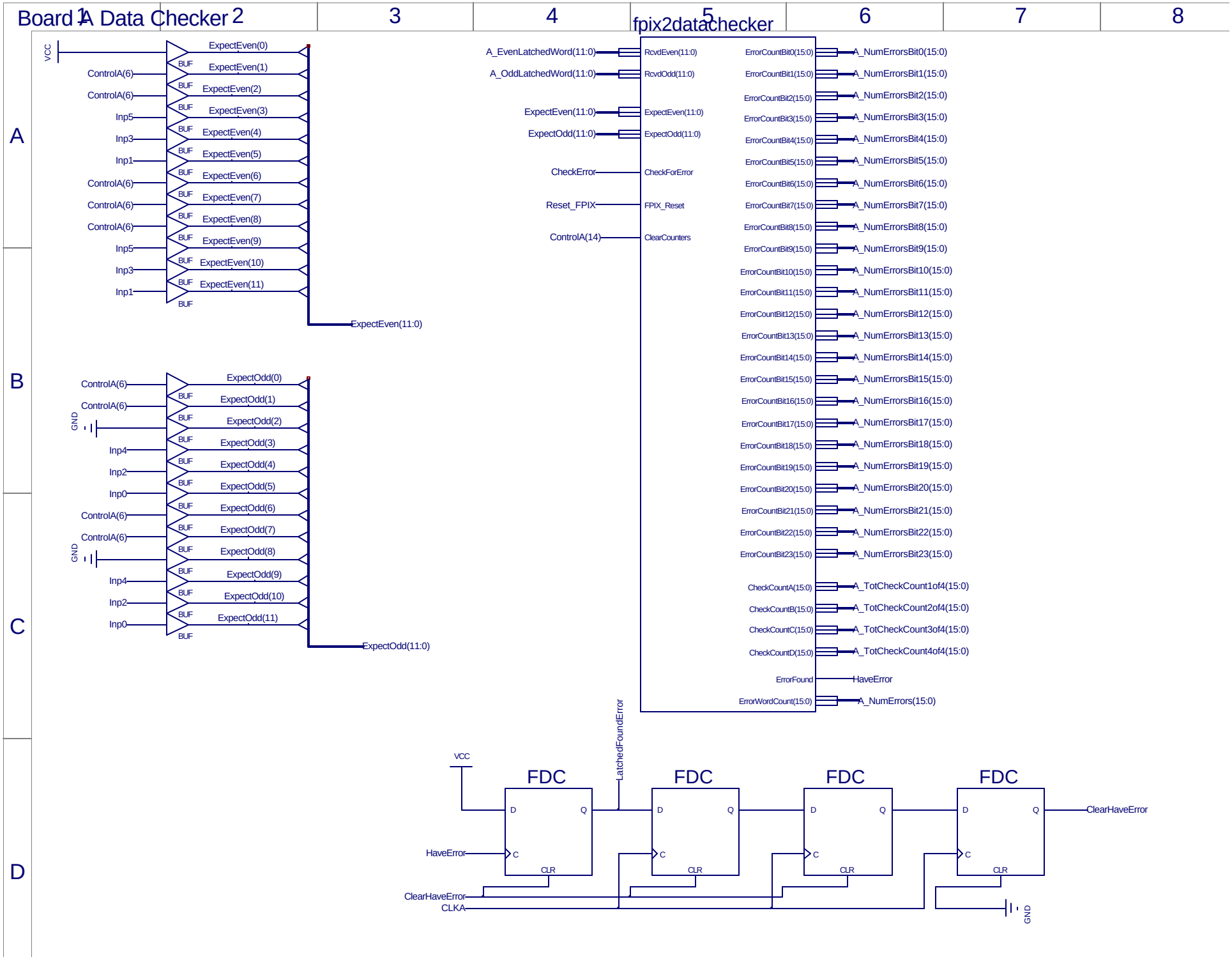
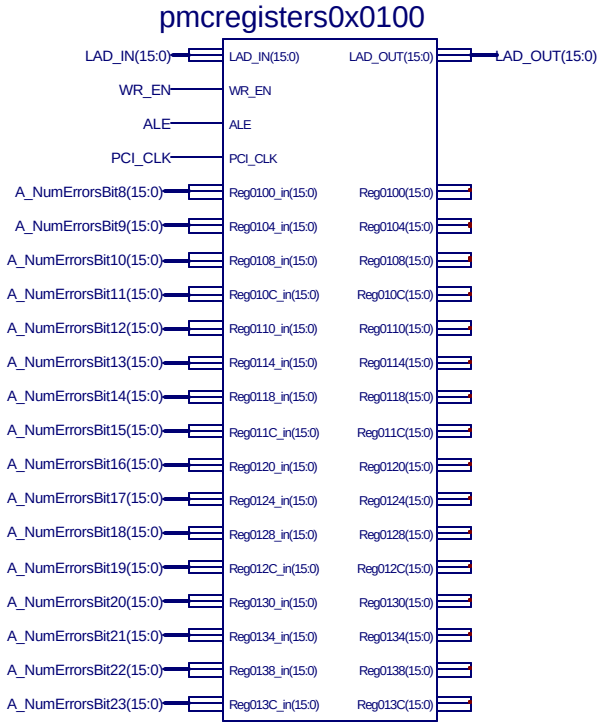
Board A Data Checker



Registers for Board A Errors



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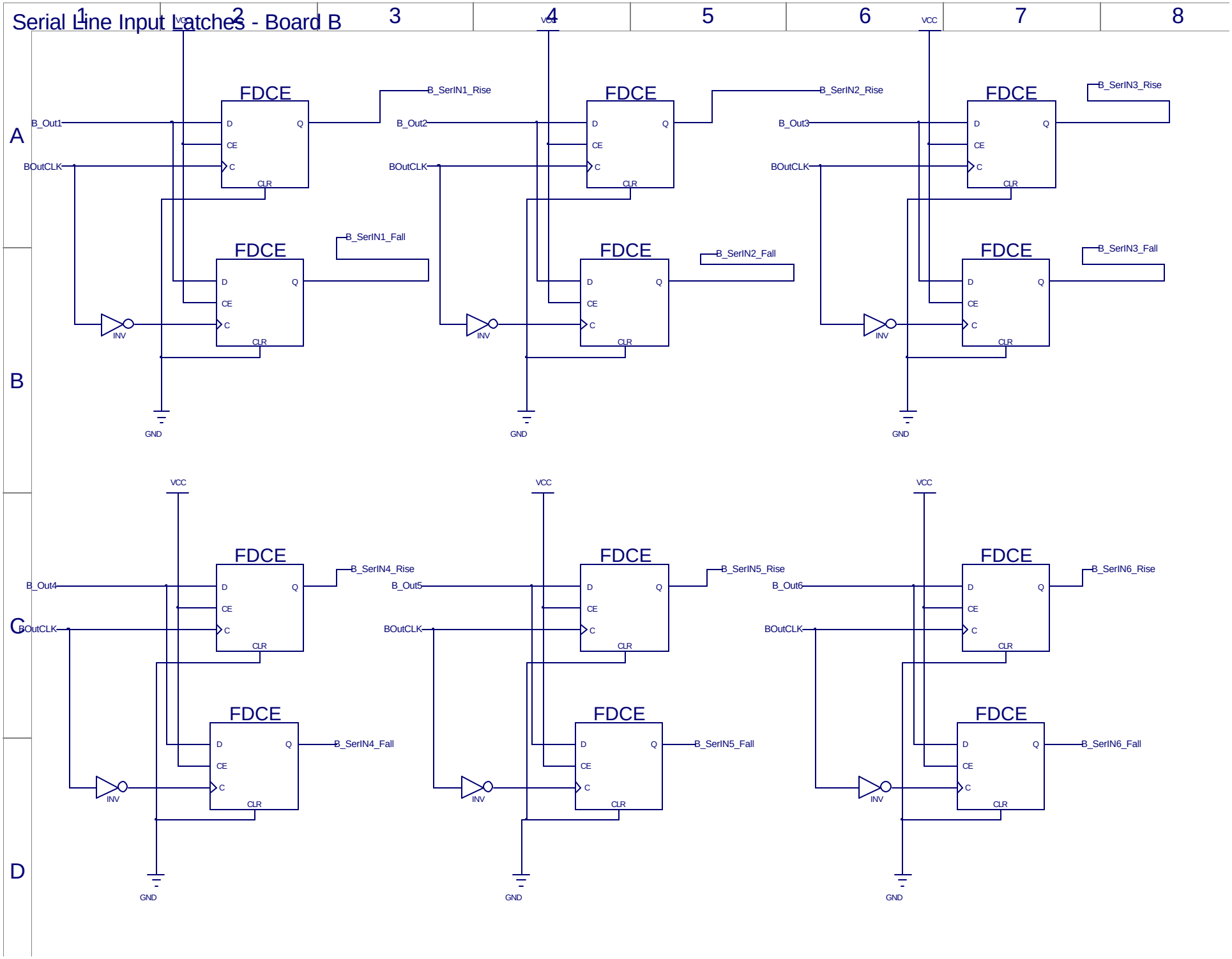
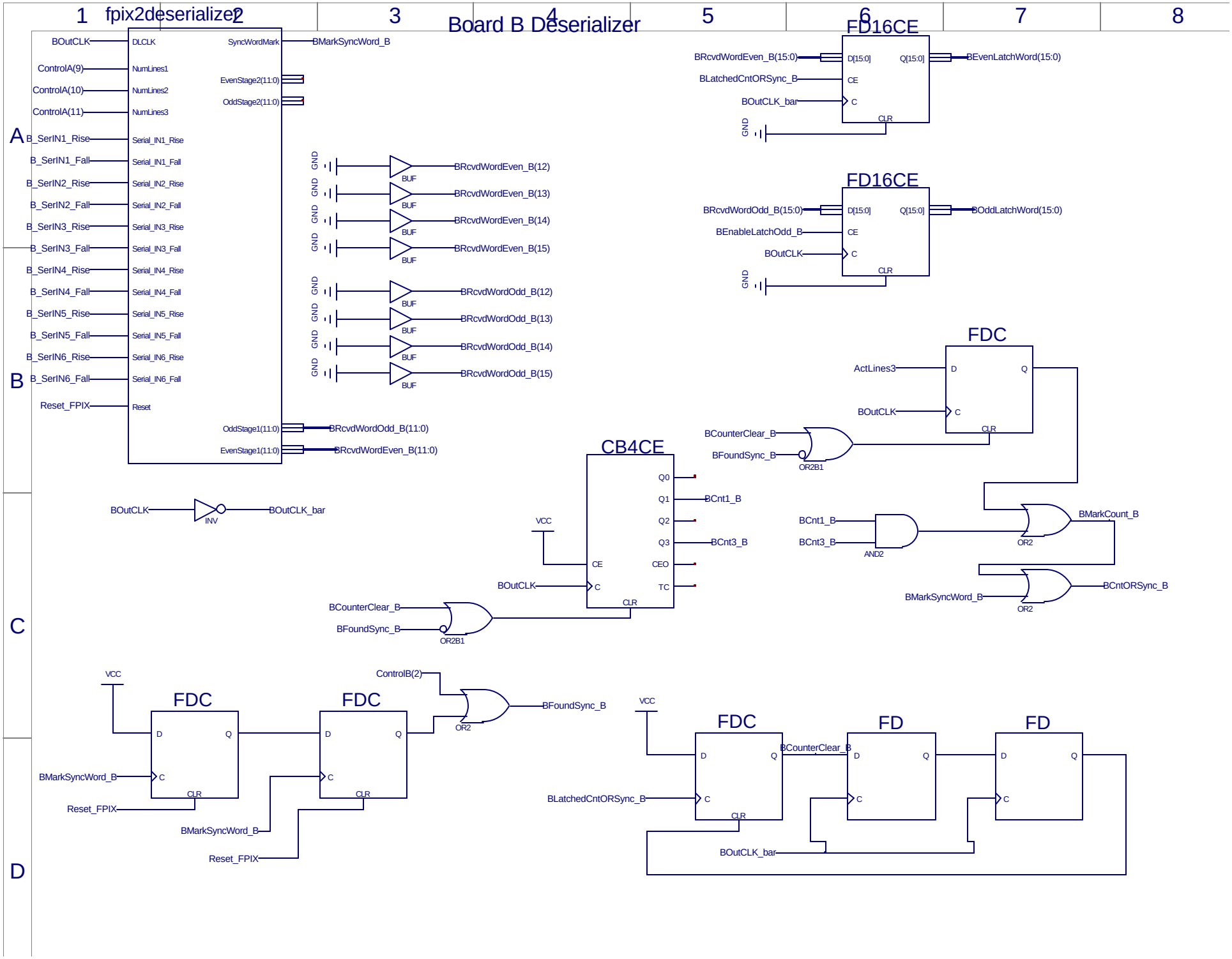
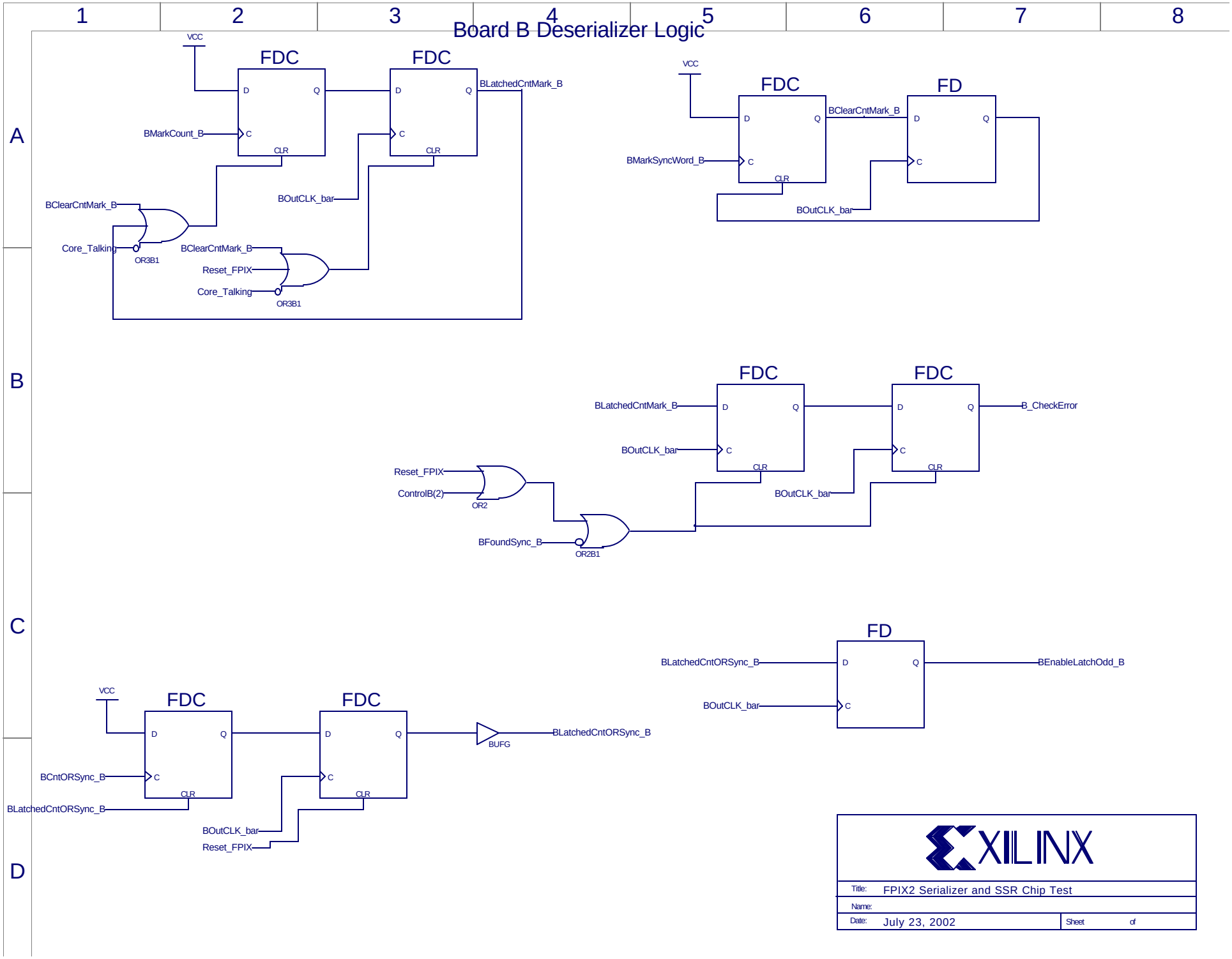
Serial Line Input Latches - Board B

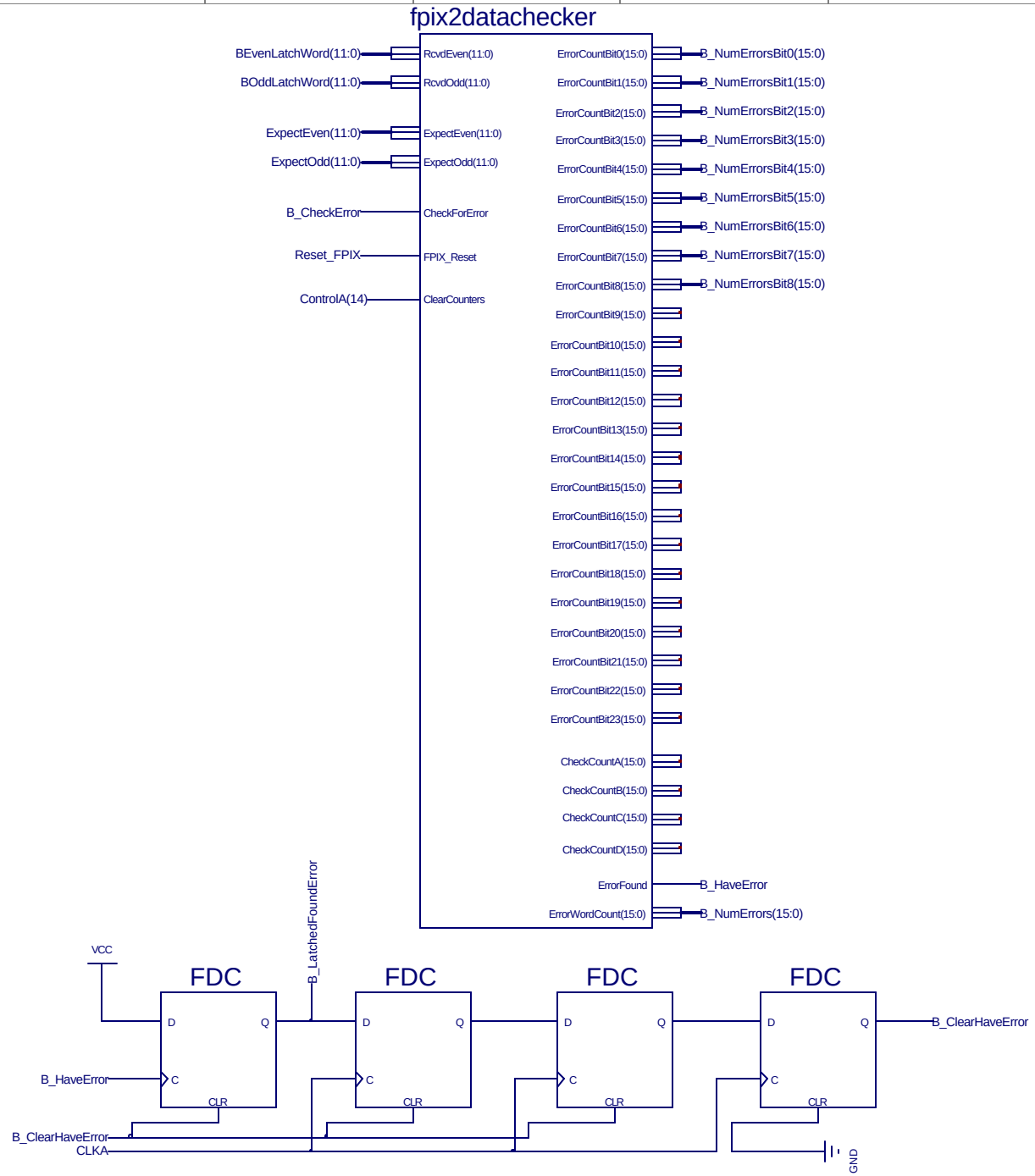



fpix2deserializer
Board B Deserializer
BOutCLK
ControlA(9)
ControlA(10)
ControlA(11)
B_SerIN1_Rise
B_SerIN1_Fall
B_SerIN2_Rise
B_SerIN2_Fall
B_SerIN3_Rise
B_SerIN3_Fall
B_SerIN4_Rise
B_SerIN4_Fall
B_SerIN5_Rise
B_SerIN5_Fall
B_SerIN6_Rise
B_SerIN6_Fall
Reset_FPIX
DLCLK
NumLines1
NumLines2
NumLines3
Serial_IN1_Rise
Serial_IN1_Fall
Serial_IN2_Rise
Serial_IN2_Fall
Serial_IN3_Rise
Serial_IN3_Fall
Serial_IN4_Rise
Serial_IN4_Fall
Serial_IN5_Rise
Serial_IN5_Fall
Serial_IN6_Rise
Serial_IN6_Fall
Reset
SyncWordMark
EvenStage2(11:0)
OddStage2(11:0)
OddStage1(11:0)
EvenStage1(11:0)
BMarkSyncWord_B
BRcvdWordOdd_B(11:0)
BRcvdWordEven_B(11:0)
GND
BUF
BRcvdWordEven_B(12)
BRcvdWordEven_B(13)
BRcvdWordEven_B(14)
BRcvdWordEven_B(15)
BRcvdWordOdd_B(12)
BRcvdWordOdd_B(13)
BRcvdWordOdd_B(14)
BRcvdWordOdd_B(15)
FD16CE
BRcvdWordEven_B(15:0)
BLatchedCntORSync_B
BOutCLK_bar
D[15:0]
Q[15:0]
CE
C
CLR
BEvenLatchWord(15:0)
FD16CE
BRcvdWordOdd_B(15:0)
BEnableLatchOdd_B
BOutCLK
BOddLatchWord(15:0)
FDC
ActLines3
D
Q
BOutCLK
C
CLR
BCounterClear_B
BFoundSync_B
OR2B1
BOutCLK
INV
BOutCLK_bar
CB4CE
VCC
Q0
Q1
Q2
Q3
CEO
TC
BCnt1_B
BCnt3_B
CE
BOutCLK
C
CLR
BCounterClear_B
BFoundSync_B
OR2B1
BCnt1_B
BCnt3_B
AND2
OR2
BMarkCount_B
BMarkSyncWord_B
OR2
BCntORSync_B
VCC
FDC
D
Q
BMarkSyncWord_B
C
CLR
Reset_FPIX
FDC
D
Q
C
CLR
BMarkSyncWord_B
Reset_FPIX
ControlB(2)
OR2
BFoundSync_B
VCC
FDC
D
Q
BCounterClear_B
BLatchedCntORSync_B
C
CLR
FD
D
Q
C
FD
D
Q
C
BOutCLK_bar

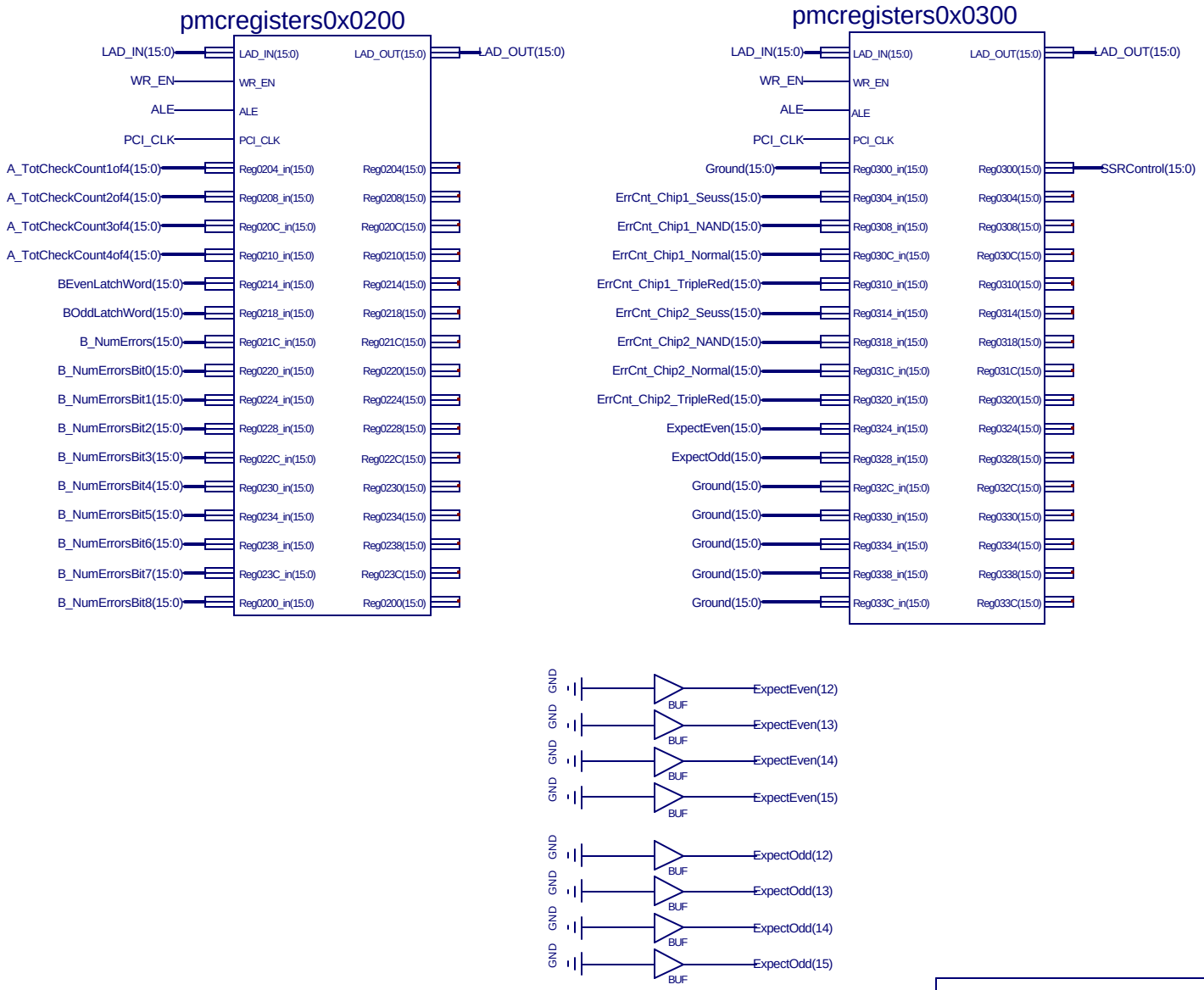
Board B Deserializer Logic



Board B Data Checker



Registers for Board B and SSR Errors and Control



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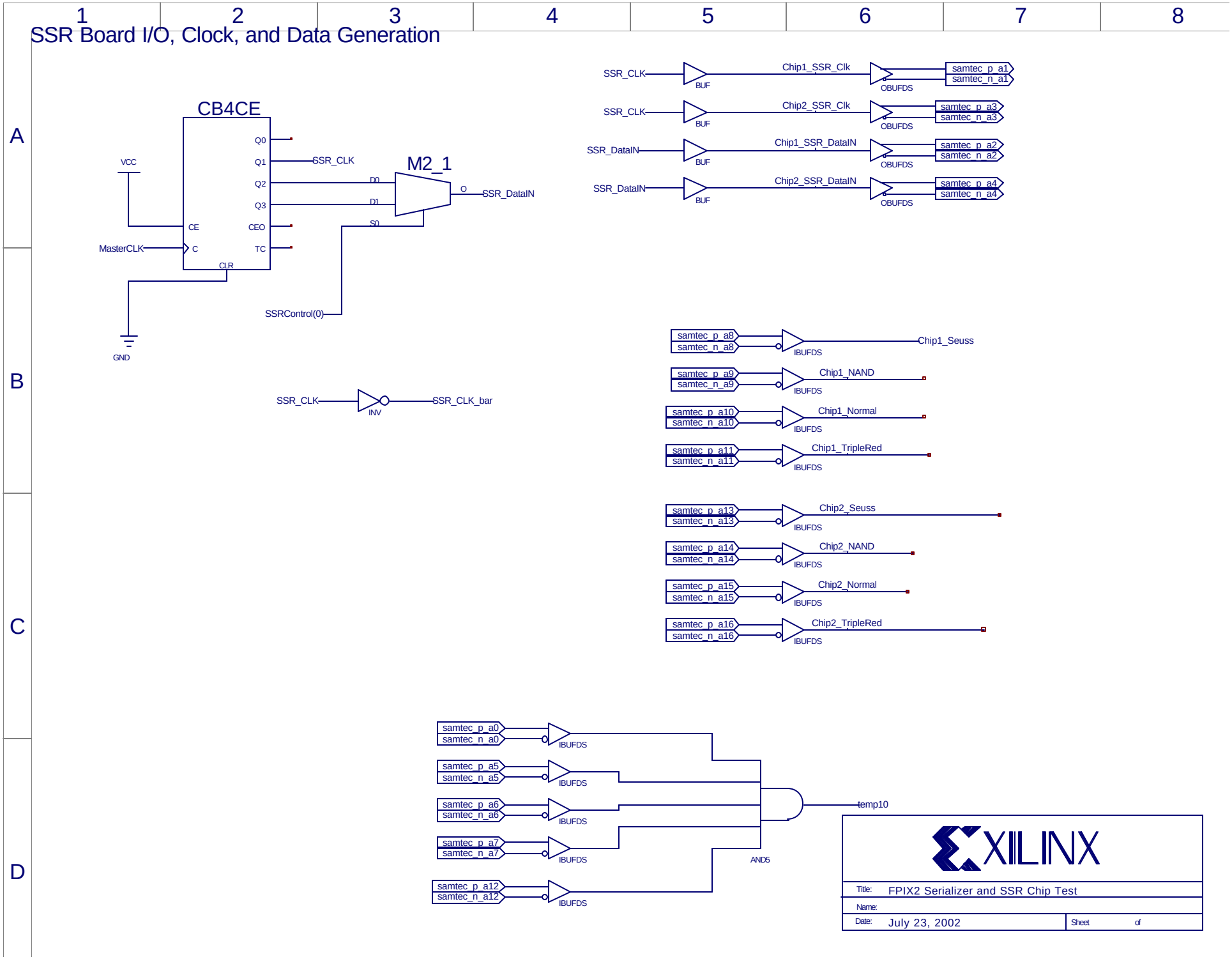
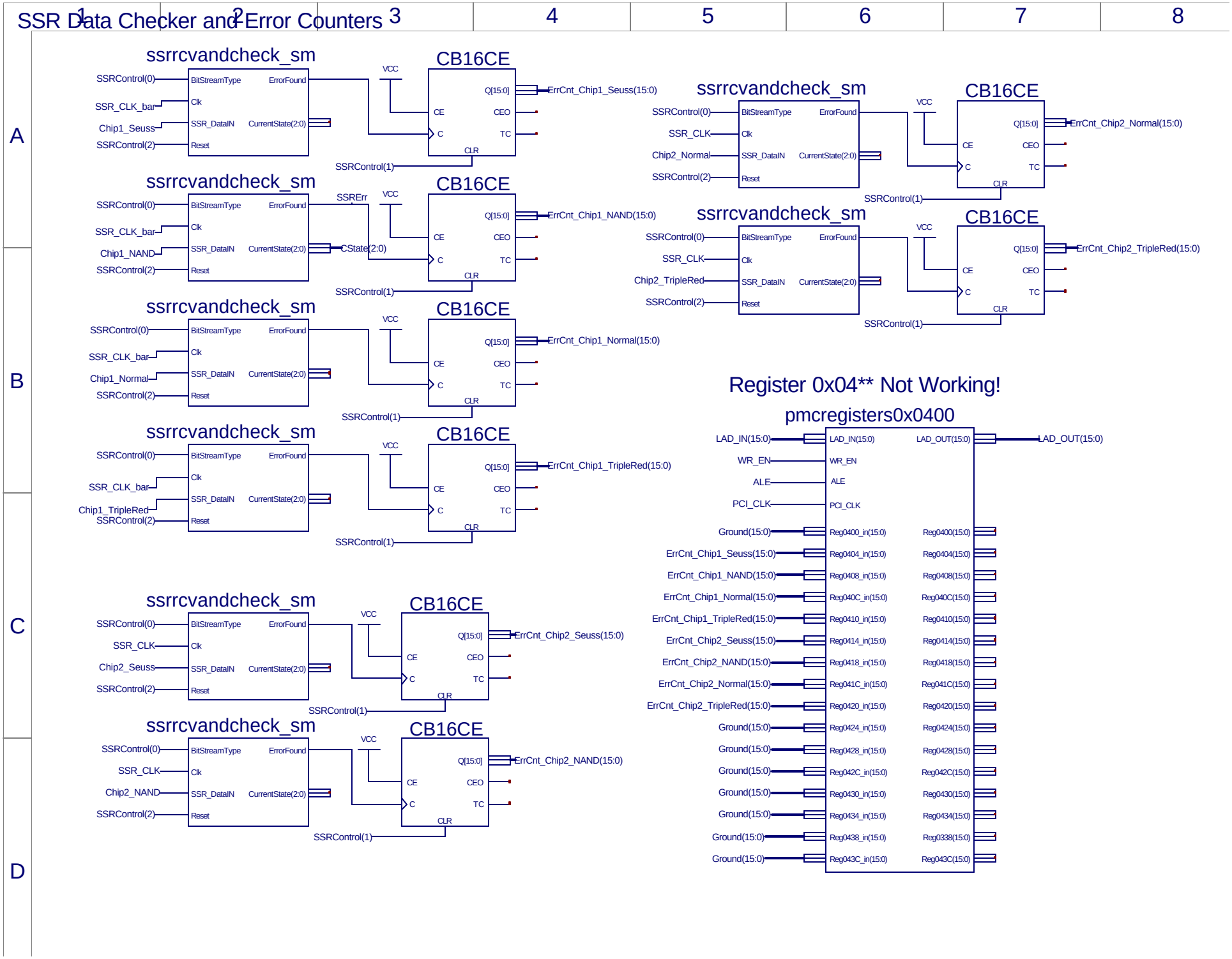
SSR Board I/O, Clock, and Data Generation



SSR Data Checker and Error Counters