

Fermi National Accelerator Laboratory

PIXEL DETECTOR PROJECT

FPIX Data Readout Design and Protocol for BTeV

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Table of Contents

1	INTRODUCTION	1
2	SYSTEM OVERVIEW	1
3	CLOCK GENERATION AT THE PDCB.....	2
3.1	Clock Frequency and Transmission Technique	2
3.2	Performance Limits	3
3.3	FPGA LVDS Drivers	4
4	DESIGN AT THE FPIX PERIPHERY	4
4.1	Serialization Clock Recovery	4
4.2	Core Clock Generation	5
4.3	Column Address Encoding	6
4.4	Core Data Word Mark	6
4.5	Data Word	7
4.6	Sync/Status Word	8
4.7	Data Latch Clock	8
4.8	Serialization Configurations	9
4.8.1	6 Serial Lines	9
4.8.2	4 Serial Lines	10
4.8.3	2 Serial Lines	10
4.8.4	1 Serial Line	11
5	DATA RECOVERY AT THE PDCB	11
5.1	Data Latch Clock and Serialized Data Alignment	11
5.2	Xilinx LVDS Receivers	11
5.3	Serial Data Recovery	11
5.4	Start Up Sequence	12
5.5	Expected Timing Margins.....	13
5.5.1	FPIX Serializer to Serializer Skew.....	13
5.5.2	Feethrough Board Trace Skew.....	13
5.5.3	Cable Induced Skew	13
5.5.4	PDCB Trace Skew.....	14
5.5.5	FPGA Skew.....	14
5.5.6	FPGA Data Latch Setup & Hold Requirements.....	14
5.5.7	Summary of Parameters	15

List of Figures

<i>Figure 1. Example FPIX module with 5 FPIX chips.</i>	<i>1</i>
<i>Figure 2. Clocks for Data Readout.</i>	<i>3</i>
<i>Figure 3. Unformatted core data word and formatted data word.</i>	<i>6</i>
<i>Figure 4. Sync/Status Word.</i>	<i>8</i>
<i>Figure 5. Waveforms for 6 serial line configuration.</i>	<i>9</i>
<i>Figure 6. Waveforms for 4 serial line configuration.</i>	<i>10</i>
<i>Figure 7. Waveforms for 2 serial line configuration.</i>	<i>10</i>
<i>Figure 8. Waveforms for 1 serial line configuration.</i>	<i>10</i>
<i>Figure 9. Receiver FPGA schematic.</i>	<i>12</i>
<i>Figure 10. Sources of signal skew.</i>	<i>13</i>
<i>Figure 11. Timing margin at the receiver FPGA.</i>	<i>14</i>

List of Tables

<i>Table 1. Clock frequencies and bandwidth for different configurations.</i>	<i>3</i>
<i>Table 2. DC Specifications for LVDS output drivers on Xilinx Virtex II FPGA.</i>	<i>4</i>
<i>Table 3. Column address encoding and equations.</i>	<i>5</i>
<i>Table 4. Illegal column addresses.</i>	<i>6</i>
<i>Table 5. Mapping of core data word bits to formatted data word bits.</i>	<i>7</i>
<i>Table 6. Status bit meaning.</i>	<i>8</i>
<i>Table 7. Xilinx Virtex II LVDS Receiver DC Specifications.</i>	<i>11</i>
<i>Table 8. Summary of timing parameters.</i>	<i>15</i>

1 Introduction

This document describes the FPIX peripheral data readout requirements and specifications for the BTeV pixel detector system at Fermilab. While the FPIX core is responsible for digitizing and time stamping the analog detector signal, the periphery is responsible for formatting the FPIX core data and serializing the data onto a configurable number of serial lines. A brief overview of the BTeV pixel detector system is given followed by sections describing the clocking scheme, data formatting, word alignment technique, the four serial configurations, data recovery at the receiver, as well as timing margins and how data errors should be handled.

2 System Overview

The BTeV Pixel detector system consists of 128x22 channel FPIX chips with each chip bump bonded a 128x22 array of silicon pixel sensors. Analog signals from the sensors are digitized, time stamped, and formatted into a 23 bit word by the FPIX core. The FPIX periphery is responsible for formatting the 23 bit core word and adding an extra bit for word alignment at the receiver. The 24 bit data word is serialized at the periphery by a configurable number of serial lines: 6, 4, 2, or 1. The periphery drives the serialized data and a Data Latch Clock (DLCLK) LVDS over copper to Pixel Data Combiner Boards (PDCBs) approximated 10m away.

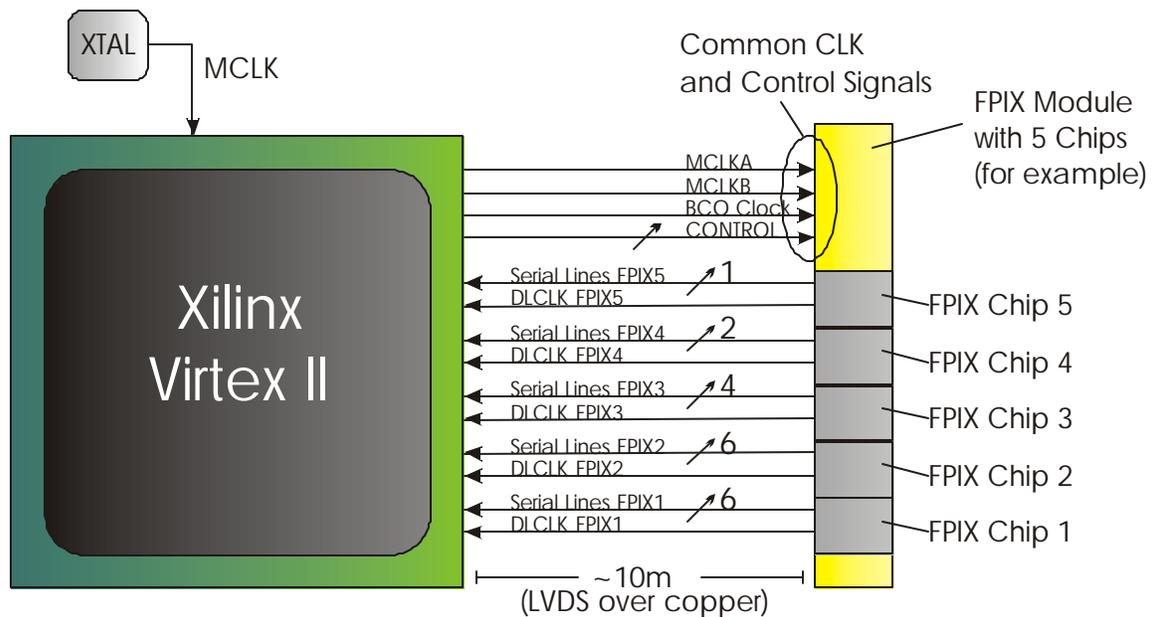


Figure 1. Example FPIX module with 5 FPIX chips.

Multiple FPIX chips and their sensors are grouped into modules. FPIX chips on a given module share common clocks (MCLKA, MCLKB, and BCO Clock) and a common control bus. Clocks and control signals come from an FPGA on the PDCB. While the clock and control signals are bussed, the serialized data path is point to point between each FPIX and the PDCB. FPIX chips on a given module can have differing numbers of serial lines. Each FPIX is capable of being configured to either 6, 4, 2, or 1 serial lines. The number of serial lines required depends on the expected hit rate the particular FPIX chip needs to support. Figure 1 diagrams an example FPIX module with 5 FPIX chips. Chip 1 in Figure 1 is configured for 6 serial lines while Chip 5 is configured for only 1 serial line. Each FPIX sends a DLCLK in parallel with its serialized data.

The Pixel detector system for BTeV consists of 30 pixel stations. Each station consists of two detector planes: a bend view and a non bend view. Each detector plane consists of multiple modules oriented in the same direction.

3 Clock Generation at the PDCB

The FPIX chip internally requires 3 clocks: bunch crossing clock (BCO clock), core clock (RCLK), and serialization clock (SCLK). The BCO clock is completely asynchronous to the both SCLK and RCLK and is part of the control section of FPIX. The BCO clock requirements are not discussed in this document. The PDCB is the source for FPIX's serialization clock (SCLK) and core clock (RCLK). For FPIX to recover a clean clock, the PDCB sends two clocks, 90° apart, at ½ the SCLK frequency (see Figure 2). The two clocks are received at the FPIX and are used to derive both SCLK and RCLK. This technique gives the PDCB full control of the both the frequency and duty cycle of the recovered SCLK.

3.1 Clock Frequency and Transmission Technique

The designed frequency of operation is a function of the maximum allowable FPIX core clock frequency and the maximum number of serializers per chip. Based on simulations, the maximum allowable FPIX core clock (RCLK) frequency is approximately 35Mhz. The designed maximum number of serializers per chip is six. The data formatting technique to be described in section 4.8 will show that with 6 serial lines, 4 bits of data need to be transmitted every 35Mhz. This results in a serialization clock frequency (SCLK) of 140Mhz (or, equivalently, 140Mbps). For FPIX chips configured with fewer serial lines, SCLK remains the same, but RCLK is decreased proportionately. All FPIX chips regardless of their configuration (in terms of number of serializers used) need to recover a 140Mhz SCLK. Table 1 summarizes the clock frequencies for each of the four serial configurations.

Both the FPIX SCLK and RCLK originate at the PDCB. An oscillator on the PDCB generates a master clock (MCLK) at a frequency equal to ½ SCLK. With SCLK at 140Mhz, MCLK frequency is 70Mhz. MCLK is sent to a Digital Clock Manager (DCM) inside a Xilinx Virtex II series (or equivalent) FPGA where a 90° phase shifted copy of MCLK is created. The DCM provides both the frequency itself and a 90deg phase shift of the CLK. Internal logic resources of the FPGA allow the user to fine adjust the 90°

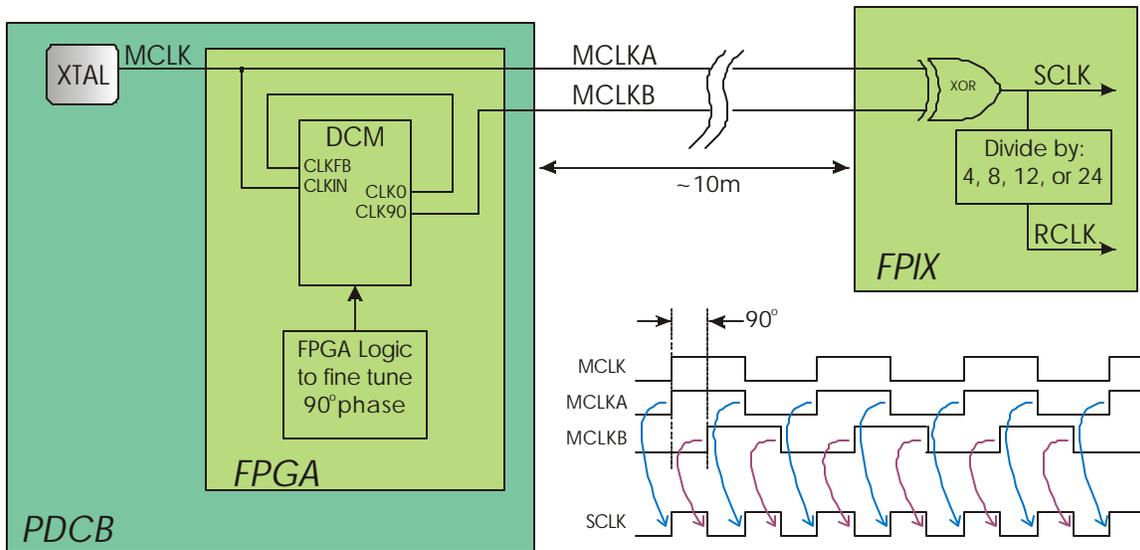


Figure 2. Clocks for Data Readout.

phase shift with Period/256 resolution ($\sim 56\text{ps}$ with 70MHz MCLK). This is important for adjusting the alignment of the return clock and serialized data as will be discussed in section 4. The 0° phase shifted (no phased shift) version of MCLK is called MCLKA and the 90° phase shifted version of MCLK is called MCLKB.

Both MCLKA and MCLKB are sent to the FPIX. Providing two phases of the same clock at $\frac{1}{2}$ the desired SCLK frequency allows for a simple recovery circuit at the FPIX (XOR of MCLKA and MCLKB) as well as limiting the switching frequency of signals along the approximately 10m cables connected the PDCB to the FPIX modules (see Figure 2).

3.2 Performance Limits

The Xilinx Virtex II DCM can handle an input and output frequency range from 24MHz to 180MHz (-4 speed grade parts in Low Frequency Mode). This is well within the expect 70MHz required MCLK. The synthesized 90° phase shifted MCLK is specified to have a maximum period jitter of $\pm 150\text{ps}$.

Configuration	Clock Frequency (MHz)				Bandwidth	
	MCLK	MCLKA	MCLKB	SCLK	RCLK	(Mbps)
6 serial	70.0	70.0	70.0	140.0	35.0	840.0
4 serial	70.0	70.0	70.0	140.0	23.3	560.0
2 serial	70.0	70.0	70.0	140.0	11.7	280.0
1 serial	70.0	70.0	70.0	140.0	5.8	140.0

Table 1. Clock frequencies and bandwidth for different configurations.

Xilinx Virtex II LVDS Output DC Specifications						
<i>DC Parameter</i>	<i>Symbol</i>	<i>Conditions</i>	<i>Min</i>	<i>Typ</i>	<i>Max</i>	<i>Units</i>
Output High	V _{OH}	100Ω Termination			1.475	V
Output Low	V _{OL}	100Ω Termination	.925			V
Differential Output	V _{ODIFF}	100Ω Termination	250	350	400	mV
Output Common Mode	V _{OCM}	100Ω Termination	1.125	1.2	1.275	V

Xilinx Virtex II Extended LVDS Output DC Specifications						
<i>DC Parameter</i>	<i>Symbol</i>	<i>Conditions</i>	<i>Min</i>	<i>Typ</i>	<i>Max</i>	<i>Units</i>
Output High	V _{OH}	100Ω Termination			1.70	V
Output Low	V _{OL}	100Ω Termination	.705			V
Differential Output	V _{ODIFF}	100Ω Termination	440		820	mV
Output Common Mode	V _{OCM}	100Ω Termination	1.125	1.2	1.275	V

Table 2. DC Specifications for LVDS output drivers on Xilinx Virtex II FPGA.

3.3 FPGA LVDS Drivers

The Xilinx Virtex II series FPGAs have dedicated LVDS drivers that will be used for transmitting the clock and control signals to the FPIX modules from the PDCB. The drivers are current mode drivers and can be configured as either standard 350mA LVDS or Extended LVDS. Table 2 describes the DC specifications for both of these LVDS configurations. The LVDS signal will be driven approximately 10m through 100Ω impedance balanced data cable as well as traces on the feedthrough PCB and traces on the FPIX module before reaching the FPIX chip. A 100Ω termination for each LVDS signal is required.

4 Design at the FPIX Periphery

The FPIX periphery is responsible for a) receiving the two phases of MCLK (MCLKA and MCLKB) from the PDCB, b) deriving the serializing clock, SCLK, from MCLKA and MCLKB, c) deriving a configurable (four possible) core clock, RCLK, frequency from SCLK, d) adding a leading '1' bit to the data for word alignment, e) encoding the column address (as specified in section 4.3), f) serializing the data into a configurable number of serial lines: either 6, 4, 2, or 1, and g) returning data latch clock for the receiver in parallel and 90° out of phase with the serialized data.

4.1 Serialization Clock Recovery

The recovered serialization clock, SCLK, will be used both for serialization of the core data and for creating the core clock, RCLK. SCLK is created from MCLKA and MCLKB via an XOR of the two clocks (see Figure 2). This simple SCLK recovery technique eliminates the need for any fixed analog delay at the FPIX. As long as MCLKA and MCLKB are 90° out of phase, the resulting SCLK should have a 50% duty cycle. The frequency can easily be changed at the PDCB and not disturb the 50% duty cycle. If a 50% duty cycle is not desired, then the PDCB FPGA's ability to fine tune the

phase shift of MCLKB can be used. As will be shown in section 5.5, a 50% duty cycle is important for good data latch clock to serialized data alignment.

4.2 Core Clock Generation

The FPIX core clock, RCLK, is a divided down version of the recovered SCLK. The degree of division depends on the FPIX serial line configuration. The reason for using different RCLK frequencies for the different serial configurations is to ensure that the peak bandwidth of data coming out of the FPIX core does not exceed the total bandwidth of the serializers. This eliminates the need for buffering the core data before it is serialized. Because FPIX can be configured to 6, 4, 2 or 1 serializer(s) the necessary division are 4, 6, 12, and 24. Table 1 describes the RCLK frequency and level of division for the 4 various serial configurations.

Core Column Number	Binary UnEncoded Column Address					Binary Encoded Column Address					Encoded Column Number	<u>Equations</u>
	a_{11}	a_{10}	a_9	a_8	a_7	b_{16}	b_{15}	b_{14}	b_{13}	b_{12}		
	0	0	0	0	0	0	1	1	0	1		
1	0	0	0	0	1	0	0	0	0	1	1	$b_{12} = a_7 + a_7 a_8 a_{10}$
2	0	0	0	1	0	0	0	0	1	0	2	$b_{13} = a_8 + a_7 a_8 a_{11}$
3	0	0	0	1	1	0	0	0	1	1	3	$b_{14} = a_9$
4	0	0	1	0	0	1	1	1	1	1	31	$b_{15} = a_{10} + a_7 a_8$
5	0	0	1	0	1	0	0	1	0	1	5	$b_{16} = a_{11} + a_7 a_8$
6	0	0	1	1	0	0	0	1	1	0	6	
7	0	0	1	1	1	0	0	1	1	1	7	
8	0	1	0	0	0	1	1	0	1	0	26	
9	0	1	0	0	1	0	1	0	0	1	9	
10	0	1	0	1	0	0	1	0	1	0	10	
11	0	1	0	1	1	0	1	0	1	1	11	
12	0	1	1	0	0	1	1	1	1	0	30	
13	0	1	1	0	1	0	1	1	0	1	13	
14	0	1	1	1	0	0	1	1	1	0	14	
15	0	1	1	1	1	0	1	1	1	1	15	
16	1	0	0	0	0	1	1	0	0	1	25	
17	1	0	0	0	1	1	0	0	0	1	17	
18	1	0	0	1	0	1	0	0	1	0	18	
19	1	0	0	1	1	1	0	0	1	1	19	
20	1	0	1	0	0	1	1	1	0	1	29	
21	1	0	1	0	1	1	0	1	0	1	21	

Table 3. Column address encoding and equations.

<i>Illegal Column Address</i>					<i>Illegal Column Number</i>
b_4	b_3	b_2	b_1	b_0	
0	0	0	0	0	0
0	0	1	0	0	4
0	1	0	0	0	8
0	1	1	0	0	12
1	0	0	0	0	16
1	0	1	0	0	20
1	0	1	1	0	22
1	0	1	1	1	23
1	1	0	0	0	24
1	1	1	0	0	28

Table 4. *Illegal column addresses.*

4.3 Column Address Encoding

Pixel columns 0 through 21 have a five bit address encoding according to Table 3. This encoding scheme insures there to be at least one ‘1’ in the first two least significant bits. This encoding coupled with the placement of the encoded 5 bit column address with LSB in bit position 12 (see Figure 3) guarantees that no back to back 24 bit data words contain 13 sequential 0’s. The purpose for doing this is described in section 5.3. There are 22 columns represented by a 5 bit column address. This results in 10 illegal column addresses as shown in Table 4.

4.4 Core Data Word Mark

A word mark bit will be appended to the least significant bit position of each 23 bit word. This bit is a guaranteed ‘1’ and will be used by the receiver FPGA to separate word boundaries. The additional word mark bit results in requiring the serializers to serialize 24 bits every RCLK cycle.

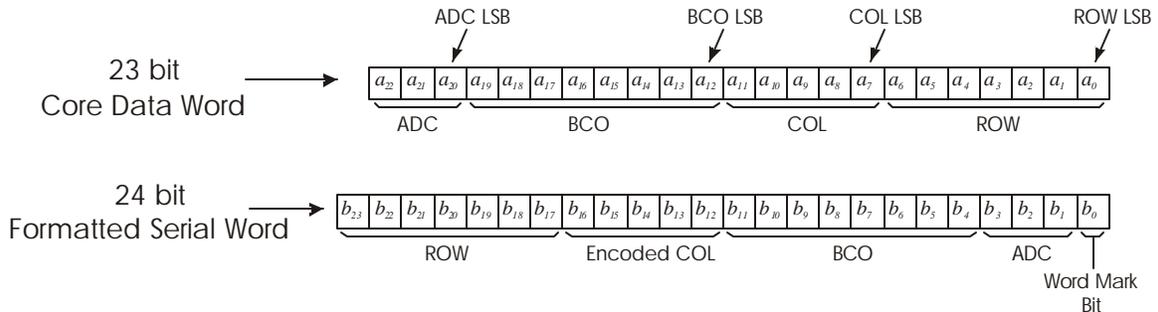


Figure 3. *Unformatted core data word and formatted data word.*

<i>Serialized</i>			<i>Description</i>
<i>Word</i>			
b_0	=	1	Word Mark
b_1	=	a_{20}	ADC bit 0
b_2	=	a_{21}	ADC bit 1
b_3	=	a_{22}	ADC bit 2
b_4	=	a_{12}	BCO bit 0
b_5	=	a_{13}	BCO bit 1
b_6	=	a_{14}	BCO bit 2
b_7	=	a_{15}	BCO bit 3
b_8	=	a_{16}	BCO bit 4
b_9	=	a_{17}	BCO bit 5
b_{10}	=	a_{18}	BCO bit 6
b_{11}	=	a_{19}	BCO bit 7
b_{12}	=	$a_7 + a_7 a_8 a_{10}$	Encoded COL bit 0
b_{13}	=	$a_8 + a_7 a_8 a_{11}$	Encoded COL bit 1
b_{14}	=	a_9	Encoded COL bit 2
b_{15}	=	$a_{10} + a_7 a_8$	Encoded COL bit 3
b_{16}	=	$a_{11} + a_7 a_8$	Encoded COL bit 4
b_{17}	=	a_0	ROW bit 0
b_{18}	=	a_1	ROW bit 1
b_{19}	=	a_2	ROW bit 2
b_{20}	=	a_3	ROW bit 3
b_{21}	=	a_4	ROW bit 4
b_{22}	=	a_5	ROW bit 5
b_{23}	=	a_6	ROW bit 6

Table 5. Mapping of core data word bits to formatted data word bits.

4.5 Data Word

Figure 3 shows the complete 24 bit data word that will be serialized and transmitted to the PDCB via 1, 2, 4, or 6 serial lines. Because of the placement and encoding of the 5 bit column address, coupled with the guaranteed leading '1' on each word, no more than 12 sequential 0s are possible. Table 5 shows the bit by bit mapping of the unformatted 23 bit core data word to the formatted 24 bit data word.

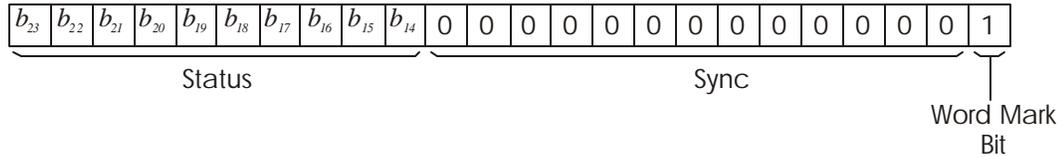


Figure 4. Sync/Status Word.

<i>Status Bit</i>	<i>Meaning</i>
b_{14}	<i>TBD</i>
b_{15}	<i>TBD</i>
b_{16}	<i>TBD</i>
b_{17}	<i>TBD</i>
b_{18}	<i>TBD</i>
b_{19}	<i>TBD</i>
b_{20}	<i>TBD</i>
b_{21}	<i>TBD</i>
b_{22}	<i>TBD</i>
b_{23}	<i>TBD</i>

Table 6. Status bit meaning.

4.6 Sync/Status Word

A special serial word that can be uniquely identified by the receiver as sync/status word is shown in Figure 4. The Sync/Status word is 24 bits (same as data word) and has a leading ‘1’ (word mark bit) followed by 13 ‘0’s. Because a sequence of 13 ‘0’s is impossible to appear anywhere except for the sync word, the receiver FPGA uses this as a master sync to align the word boundaries. The remaining 10 bits in the data word are available for status as described in Table 6.

The Sync/Status word should be available for transmission at anytime through a control command from the PDCB FPGA. The Sync/Status word should also be transmitted when the core is idle (no core data). If possible, the Sync/Status word should be transmitted after each token revolution through the core. Doing this will guarantee that the maximum data loss due to receiver data alignment errors is the amount of data in one core token pass revolution.

4.7 Data Latch Clock

A data latch clock (DLCLK) will be sent by FPIX in parallel with the serialized data regardless of the serial configuration. Both edges of DLCLK will be used by the receiver FPGA to latch the serialized data with data bit b_0 (word mark bit) always latched by a rising edge of DLCLK. Because both edges are used, the DLCLK switching frequency is

equal to $\frac{1}{2}$ SCLK frequency. In order to provide maximum setup and hold at the receiver FPGA, the edges of DLCLK should be 90° out of phase with the edges of the serial data. If the serialized data edges are synchronous to the rising edge of SCLK, then the DLCLK edges should be synchronous to the falling edges of SCLK. This allows the PDCB to control the DLCLK/serial data alignment by adjusting the phase relationship between MCLKA and MCLKB (as shown in Figure 2).

Using the frequencies in Table 1, the DLCLK switching frequency should be 70Mhz in all four configurations. Since FPIX should always be transmitting data (either a formatted core data word, or a sync/status word), DLCLK should effectively be a free running clock.

4.8 Serialization Configurations

FPIX will be configurable to operate using either 6, 4, 2 or 1 serial lines for transmission of the 24 bit formatted serial word. The individual serial links in each of the four configurations will operate at the same frequency (140 Mbps), but the core RCLK will be proportional to the bandwidth of the readout as described in section 3.1 (see Table 1). In each of the configurations, it is important that the word mark bit (b_0) be the first (in time) to appear on the serial line and that it corresponds to a rising edge of DLCLK. This fact is important for the receiver FPGA on the PDCB.

4.8.1 6 Serial Lines

FPIX chips configured with 6 serial lines will be used for chips requiring the highest bandwidth readout. This configuration allows the core to operate at its maximum frequency. Each of the 6 serializers will serialize 4 bits every RCLK cycle. This results in a SCLK to RCLK ratio of 4. With SCLK = 140Mbps, RCLK is 35Mhz. The maximum switching frequency of any serial line and DLCLK is 70MHz. Figure 5 diagrams the waveforms and bit positions for the 6 serial line configuration that FPIX should drive to the PDCB approximately 10m away.

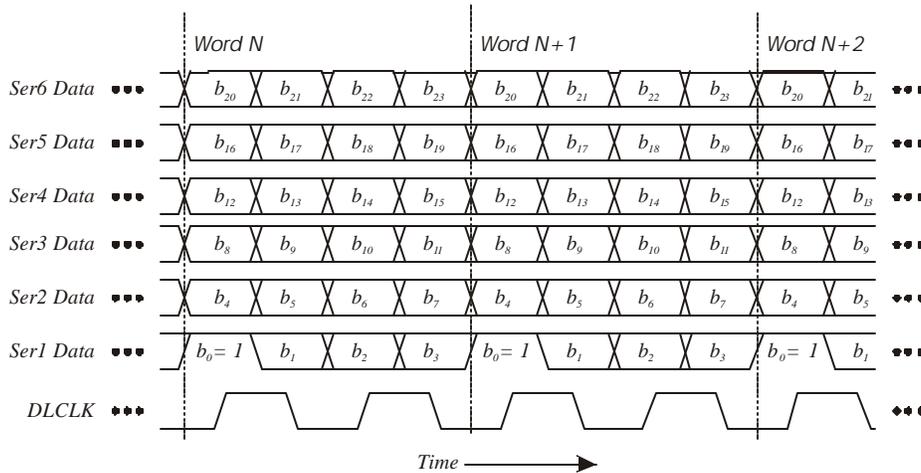


Figure 5. Waveforms for 6 serial line configuration.

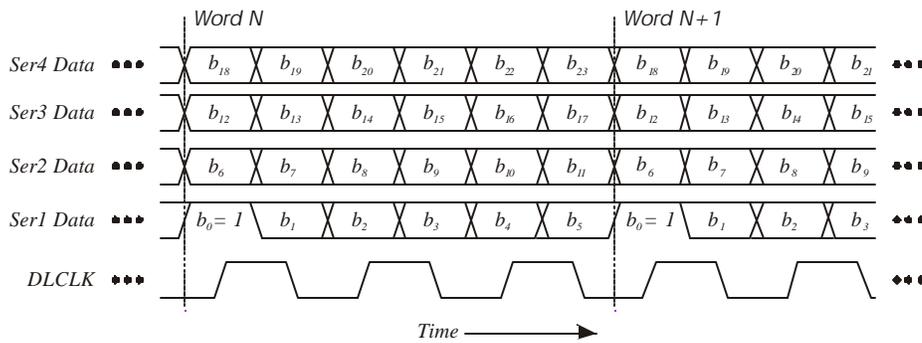


Figure 6. Waveforms for 4 serial line configuration.

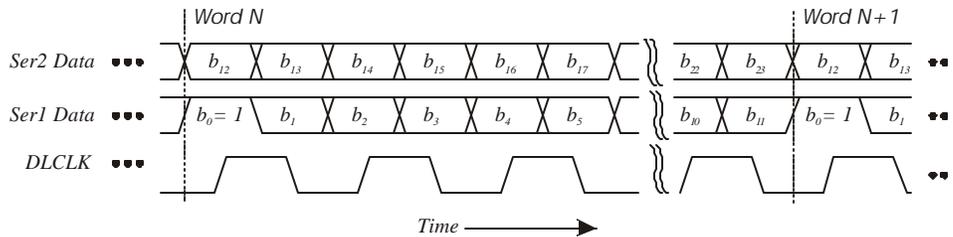


Figure 7. Waveforms for 2 serial line configuration.

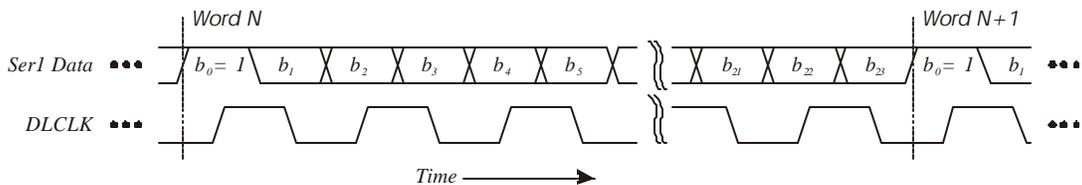


Figure 8. Waveforms for 1 serial line configuration.

4.8.2 4 Serial Lines

FPIX chips configured with 4 serial lines requires each of the 4 serializers to serialize 6 bits every RCLK. This results in a SCLK to RCLK ratio of 6. With SCLK = 140Mbps, RCLK is 23.3Mhz. Figure 6 diagrams the waveforms and bit positions for the 4 serial line configuration that FPIX should drive to the PDCB approximately 10m away.

4.8.3 2 Serial Lines

FPIX chips configured with 2 serial lines requires each of the 2 serializers to serialize 12 bits every RCLK. This results in a SCLK to RCLK ratio of 12. With SCLK = 140Mbps, RCLK is 11.67Mhz. Figure 7 diagrams the waveforms and bit positions for the 2 serial line configuration that FPIX should drive to the PDCB approximately 10m away.

4.8.4 1 Serial Line

FPIX chips configured with 1 serial lines requires the 1 serializer to serialize 24 bits every RCLK. This results in a SCLK to RCLK ratio of 24. With SCLK = 140Mbps, RCLK is 5.83Mhz. Figure 8 diagrams the waveforms and bit positions for the 1 serial line configuration that FPIX should drive to the PDCB approximately 10m away.

5 Data Recovery at the PDCB

The same FPGA that sends MCLKA and MCLKB (as well as the control signals) is responsible for receiving the serialized data from the FPIX chip. Both edges of the DLCLK are used by the FPGA to latch the incoming serial data. The receiving FPGA uses the sync/status word to forcibly determine where the 24 bit word boundaries are and uses the word mark bit (b_0) along with a counter to determine the word boundaries of the formatted data words. Logic in the FPGA checks for data error signatures and word alignment problems.

5.1 Data Latch Clock and Serialized Data Alignment

Because the DLCLK edges should be 90° out of phase with the serialized data edges, no analog delay components are necessary. In addition, the FPGA has the ability to adjust the DLCLK to serialized data phase relation by fine tuning the phase of MCLKB (relative to MCLKA) as discussed in section 3.1. This fine tuning can be used to optimize the timing margins for setup and hold in the FPGA.

5.2 Xilinx LVDS Receivers

FPIX will drive the serialized data and DLCLK using LVDS over approximately 10m to the PDCB. These differential signals are received directly by the FPGA LVDS receivers. Table 7 lists the Xilinx Virtex II LVDS receiver DC specifications.

5.3 Serial Data Recovery

The incoming serial data will be latched in the FPGA with both the rising and falling edges of DLCLK. The rising edges of DLCLK will latch the even numbered data bits while the falling edge will latch the odd numbered bits. The latched data is serially shifted until the entire 24 bit word is inside the FPGA. Figure 9 shows a schematic of what this might look like for receiving serial data from an FPIX configured with 6 serial lines. Once the entire word is inside, the 24 bit word is latched and placed in a 24 bit FIFO for further processing.

Xilinx Virtex II LVDS Receiver DC Specifications						
<i>DC Parameter</i>	<i>Symbol</i>	<i>Conditions</i>	<i>Min</i>	<i>Typ</i>	<i>Max</i>	<i>Units</i>
Differential Input Voltage	V_{IDIFF}	Common-mode input = 1.25V	100	350	NA	mV
Input Common-Mode Voltage	V_{ICM}	Differential input Voltage = ± 350 mV	.2	1.25	2.2	V

Table 7. Xilinx Virtex II LVDS Receiver DC Specifications.

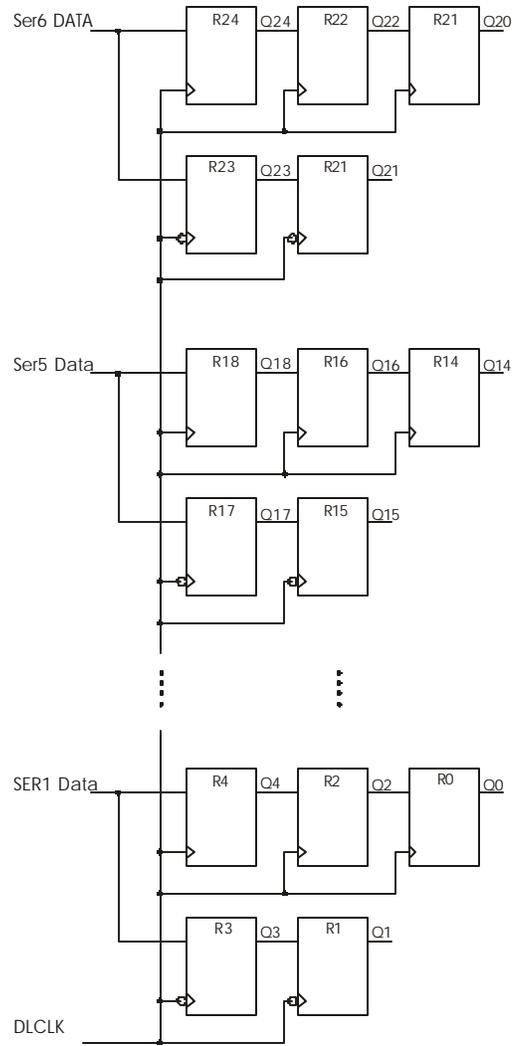


Figure 9. Receiver FPGA schematic.

Logic in the FPGA is continuously monitoring the serial shift registers. The logic looks for a '1' followed by 13 sequential '0's appearing anywhere in the received data which would indicate a sync/status word. Since a '1' followed by a sequence of 13 '0's can only appear in bit positions b_0 through b_{13} , the FPGA uses this as a master sync to set the word boundary. Once a master sync/status word has been detected, it uses a counter in conjunction with the leading word mark bit (b_0) to count the received bits of the next 24 bit words. The leading '1' at bit position b_0 is used to mark the boundary and verify the bit count is correct.

5.4 Start Up Sequence

For the receiver FPGA to properly receive the serialized data, it must establish a word boundary. By default, FPIX should transmit sync/status words until it receives acknowledgement from the receiver FPGA (via a control command) that data has been received and a word boundary has been established. It should only take one sync/status

word to establish the word boundary. After this, if no data transmission errors occur, the FPGA should be able to receive formatted serial words indefinitely.

5.5 Expected Timing Margins

Because the pixel readout system in the worst case (6 serial line configuration) will be transmitting 6 parallel serial line with a parallel data latch clock, the skew of each signal incurred between the FPIX chip and the receiver FPGA must be minimized. Figure 10 illustrates some of the sources of signal skew. Figure 11 shows how sources of signal skew impact the timing margin at the receiver FPGA.

5.5.1 FPIX Serializer to Serializer Skew

Skew of the serialized data caused by delays inside the FPIX should be minimized. Most importantly, the magnitude of the skew relative to the transmitted DLCLK should be minimized.

5.5.2 Feethrough Board Trace Skew

Skew will be caused by trace length mismatches in the feedthrough board as well as the flex circuit. This is difficult to quantify until a layout is complete, however, it should be small relative to the other skew sources.

5.5.3 Cable Induced Skew

The data cables connecting the feedthrough board to the PDCB can introduce skew by having inconsistent propagation delays from conductor pair to conductor pair. A previous study of a 100' 50 conductor pleated foil shielded cable suggests that with a 10m cable over a span of 7 conductor pairs a worst case skew of ~1.3ns should be accounted for.

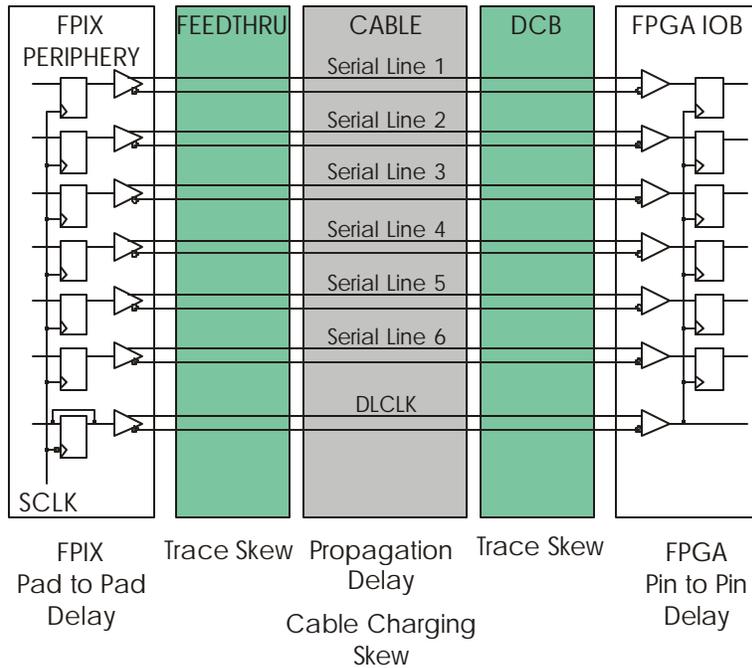


Figure 10. Sources of signal skew.

An additional phenomenon that manifests itself as skew from data edge to data edge in the same conductor pair is the cable charging effect. This effect causes the position (in time) of data edges to depend on the preceding data. For the DLCLK signal, there is no effect since the sequence of data is a periodic and continuous '1' then '0' (a free running clock). For the serial data lines, however, the sequence of '1's and '0's can be considered random. The magnitude of this effect on a pleated foil shielded cable has been measured in a previous study and is expected to be ~1.7ns.

5.5.4 PDCB Trace Skew

As with the feedthrough board, trace length mismatches on the PDCB will be the source of additional skew. However, it should be small relative to the other skew sources.

5.5.5 FPGA Skew

Internal delays in the received DLCLK to the serial data latches will need to be minimized. The magnitude of this effect depends on the layout of the FPGA.

5.5.6 FPGA Data Latch Setup & Hold Requirements.

The setup and hold requirements of the data latches that receive the serialized data will contribute to the timing margin. For the Xilinx Virtex II, the hold time is specified at 0ns and the setup time at 800ps.

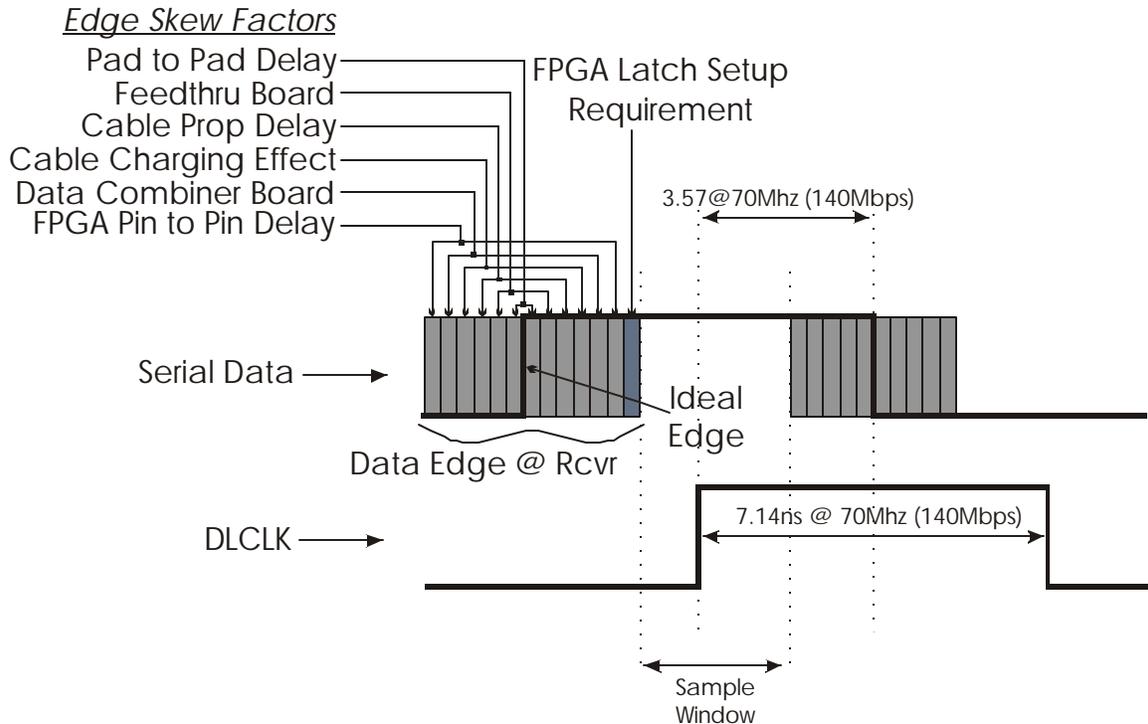


Figure 11. Timing margin at the receiver FPGA.

Parameter	Value
FPIX Serializer to Serializer Skew	250ps
Feethrough Board Trace Skew	250ps
Cable Induced Skew	1.3ns + 1.7ns
PDCB Trace Skew	250ps
FPGA Skew	250ps
FPGA Data Latch Setup & Hold Requirements	800ps
Sample Window (worst case)	2.34ns

Table 8. Summary of timing parameters.

5.5.7 Summary of Parameters

Table 8 summarizes the parameters and estimates a value of 250ps for those other than FPGA data latch setup and hold requirement and the cable induced skew. With these assumed values, the absolute worst case sample window is 2.34ns. It should be noted, however, that this does not take into account signal jitter.