



**Fermi National Accelerator Laboratory**

## **BTeV Front End Readout**

BTeV Timing, Monitoring, Control, and Combining  
(TMC<sup>2</sup>) IC

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**-PRELIMINARY-**

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## 1. Introduction

The BTeV Timing, Monitoring, Control and Combining (TMC<sup>2</sup>) IC is a component that will be implemented on several BTeV front end systems. The TMC<sup>2</sup> will have many responsibilities including: latching digitized detector data and tagging the data with the appropriate bunch crossing (BXNG) number, buffering and formatting the data for transmission to the next level of electronics (L1 buffer), receiving and decoding control commands as well as the 53Mhz system clock, controlling the analog front end components (e.g. DACs and ADCs), and returning monitoring information back to the BTeV Controls/Monitoring & Timing System. The TMC<sup>2</sup> will be implemented in an FPGA allowing for flexibility with design changes as the overall BTeV system evolves. The BTeV detector systems that will employ the TMC<sup>2</sup> in their front end readout include: RICH, Muon, EM Calorimeter, and Forward Tracker Straw. The TMC<sup>2</sup> may also be implemented in the Forward Tracker Silicon Microstrip detector readout system if radiation levels are shown to be tolerable.

Each of the four TMC<sup>2</sup> target applications (RICH, Muon, EM Calorimeter, and Straws) will require different firmware, however the general architecture and much of the firmware will be common. This commonality will reduce the engineering development and debug time and effort required to implement all four systems. Each of the four TMC<sup>2</sup> target applications may require different sized FPGAs due to their differences in channel count per front end board and the type of digitized data (e.g. overthreshold for Muon vs. 11 bits per channel for EM Calorimeter). Figure 1 shows the three main functional blocks of the TMC<sup>2</sup>.

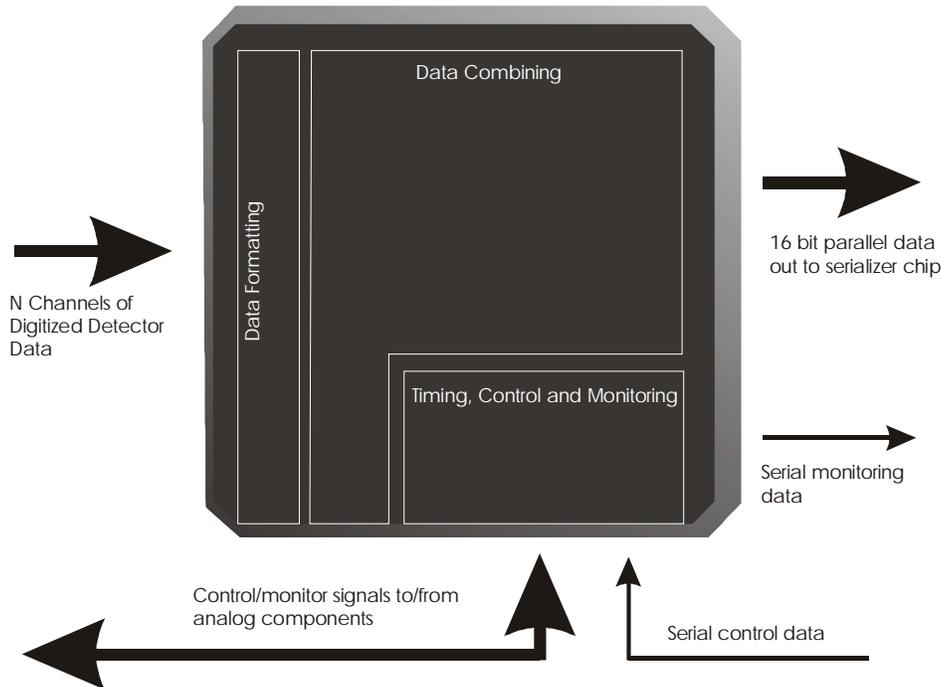


Figure 1. Main components of TMC<sup>2</sup>.

## 2. TMC<sup>2</sup> Functionality

This section describes the functionality of each of the three major TMC<sup>2</sup> functional blocks: Data Formatter, Data Combiner, and Timing, Control, and Monitoring.

### 2.1 Data Formatter Functionality

The Data Formatter block will be unique for each of the four target front end systems. The purpose of this block is to latch the incoming digitized data at a delayed time after the system bunch crossing clock (BCO clock). This programmable delay is set via the control link (at system initialization time) and allows for any latency in the analog readout electronics. The latched data is then parallel processed in groups of N channels (N depends on the target system) in Sub Data Formatters (see Figure 2). The Sub Data Formatters will recognize data from channels that are 'hit', byte align the data (if not already), and send the byte aligned data to an adjacent 16 bit wide FIFO in the Data Combiner block along with their respective channel address (or just address if overthreshold data) and BXNG. A word aligned one word EOR (0xFFFF) is then sent to the FIFO to separate the just processed BXNG data from the next BXNG data. The Sub Data Formatter must process all N channels within 132ns in order to be ready to latch data at the next BCO. Within 132ns of the delayed BCO, all of the detector data along with their respective channel addresses for one BXNG are contained in the first level of FIFOs at the Data Combiner. The Data Combiner merges these FIFOs.

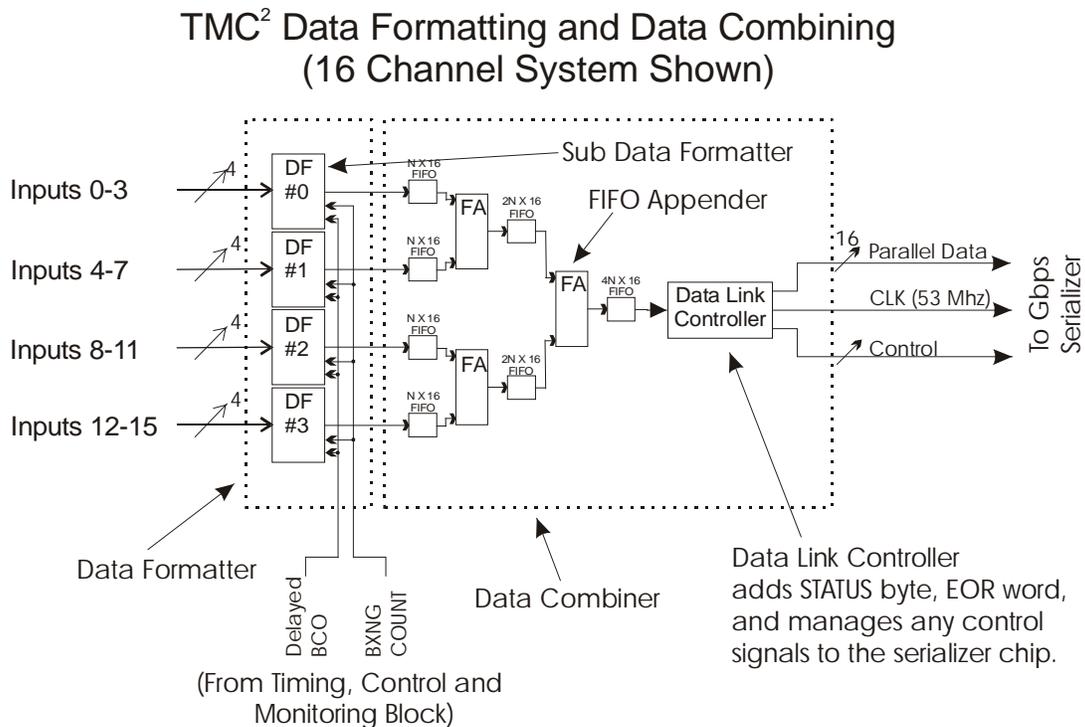


Figure 2. Data Formatter and Data Combiner arrangement.

## 2.2 Data Combiner Functionality

The Data Combiner block of the TMC<sup>2</sup> receives the byte aligned, formatted data from the Data Formatters and funnels them through a series of FIFO Appenders into a single FIFO which is sent to the Data Link Controller (see Figure 2). The FIFO Appenders (FAs) append the top FIFO with the bottom FIFO and outputs to another FIFO. The FAs also remove any filler words used to force a 16 bit word alignment at the previous stage that could be present in the appended output. The Data Link Controller inserts a STATUS byte into the data block before sending the entire block to the serializer (one block contains all data for one BXNG).

<b><i>RICH and Muon Data Block Format (256 channels Max)</i></b>		
<b><i>Description</i></b>	<b><i>Upper Byte</i></b>	<b><i>Lower Byte</i></b>
<b><i>HEADER</i></b>	BXNG	STATUS
<b><i>DATA</i></b>	Hit Address 1 (8 bits)	Hit Address 2 (8 bits)
.	.	.
.	.	.
<b><i>END OF RECORD</i></b>	EOR (FF)	EOR (FF)

<b><i>EM Calorimeter Data Block Format (31 channels Max)</i></b>		
<b><i>Description</i></b>	<b><i>Upper Byte</i></b>	<b><i>Lower Byte</i></b>
<b><i>HEADER</i></b>	BXNG	STATUS
<b><i>DATA</i></b>	Hit Address 1 (upper 5 bits) and mantissa (lower 3 bits)	8 bit ADC data
<b><i>DATA</i></b>	Hit Address 2 (upper 5 bits) and mantissa (lower 3 bits)	8 bit ADC data
.	.	.
.	.	.
<b><i>END OF RECORD</i></b>	EOR (FF)	EOR (FF)

<b><i>Straws Data Block Format (256 channels Max)</i></b>		
<b><i>Description</i></b>	<b><i>Upper Byte</i></b>	<b><i>Lower Byte</i></b>
<b><i>HEADER</i></b>	BXNG	STATUS
<b><i>DATA</i></b>	Hit Address 1 (8 bits)	TDC data (6 bits)
<b><i>DATA</i></b>	Hit Address 2 (8 bits)	TDC data (6 bits)
.	.	.
.	.	.
<b><i>END OF RECORD</i></b>	EOR (FF)	EOR (FF)

Figure 3. Data block formats for transmission to L1 Buffers.

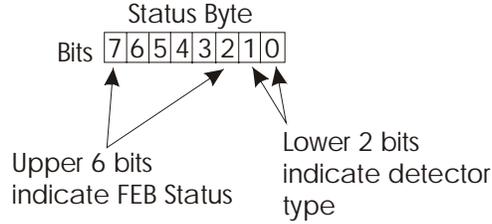


Figure 4. Status byte format.

The data output of the Data Combiner is 16 bits wide at 53Mhz (848Mbps). This data is sent directly to an encoder/serializer for serial optical transmission to the L1 Buffers. The format of a single data block depends on the target application (see Figure 3). The header and End of Record format, however, is always the same allowing for L1 buffers to be detector system independent.

The STATUS contains information such as the detector type and the status of the front end board readout. The format of the STATUS byte is shown in Figure 4. The meaning of the bits is shown in Figure 5. The detector type bits will be hardcoded in the firmware for the target application while the upper 6 status bits will be assigned to each data block by the Data Link Controller.

Other than in size, the Data Combiner should be identical for each target application. As can be seen from Figure 2, the Data Combiner architecture can be easily expanded or collapsed to accommodate any number of Sub Data Formatters.

<b>Status Word Detector Types (Lower 2 bits)</b>	
<i>Value</i>	<i>Meaning</i>
<i>0x00</i>	<i>RICH</i>
<i>0x01</i>	<i>Muon</i>
<i>0x02</i>	<i>EM Calorimeter</i>
<i>0x03</i>	<i>Straws</i>

<b>FEB Status (Upper 6 bits)</b>	
<i>Value</i>	<i>Meaning</i>
<i>0x01</i>	<i>Sparsified Data</i>
<i>0x02</i>	<i>Non-Sparsified Data</i>
<i>0x03</i>	<i>Normal</i>
<i>0x04</i>	<i>Test Pattern</i>
<i>0x05</i>	<i>Overflow Condition</i>
<i>0x06</i>	<i>TBD</i>
<i>.</i>	<i>.</i>
<i>.</i>	<i>.</i>
<i>.</i>	<i>.</i>

Figure 5. Status word lower 2 and upper 6 bit meaning.

## 2.3 Timing Control and Monitoring Functionality

The Timing Control and Monitoring functional block is responsible for a number of functions:

- Separate control data and 53Mhz clock from incoming serial control link.
- Decode control commands.
- Encode (Bi-Phase) and serialize data for the monitoring serial link.
- Provide a delayed version of BCO to Data Formatters.
- Manage BXNG counter.
- Provide control interface to auxiliary components on front end board (e.g. DACs, ADCs, etc.)
- Control initialization of any auxiliary components.
- Monitor and flag any over limit conditions (e.g. voltage, temperature, etc.).
- Reprogram EEPROM with new FPGA code downloaded from control link.

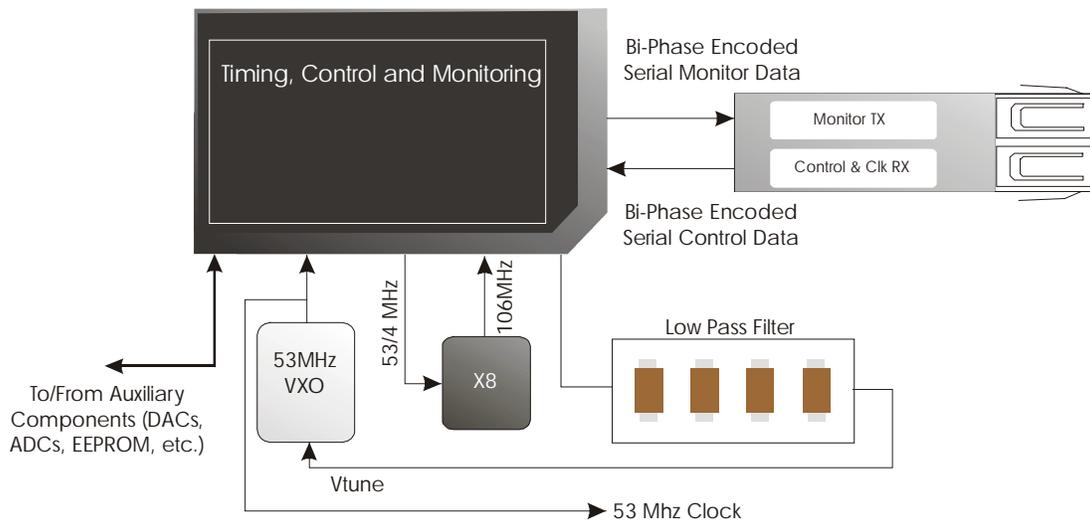


Figure 6. Timing Control and Monitoring components.

The decoding, clock recovery, and encoding design will be borrowed from the BTeV FPIX readout development (see Document # ESE-PIX-19991210 by Gustavo Cancelo). Figure 6 shows the external components (external to the TMC<sup>2</sup> FPGA) required for receiving the incoming bi-phase encoded control signal (optical connector and pin-diode, labeled *Control & Clk RX* in Figure 6), recovering the 53Mhz system clock (VXO, x8 clock multiplier) and transmitting the serialized monitoring data back to the BTeV Controls/Monitoring & Timing System (labeled *Monitor TX* in Figure 6). The incoming optical control data will be bi-phase encoded with a 106Mhz clock.

An example of possible control commands that may be implemented include:

- Send test pattern to L1 Buffer
- Send test pattern to Monitor Link
- Initialize front end component with following bit stream
- Disable channel N
- Set DAC to V Volts
- Acquire data
- Reset BXNG counter
- Initiate self test
- Download EEPROM with following bit stream
- Readout non-sparsified

An example of possible monitoring data that may be implemented include:

- Acquiring data
- Overflow condition detected
- Configuration bit stream return
- Self test PASS/FAIL

### 3. Performance Characteristics

This section describes the important performance characteristics that need to be considered and measured when developing the TMC<sup>2</sup>. Note that while performance of the Timing, Control and Monitoring functional block is important, this section focuses on the Data Combining performance. The Data Formatter functional block's most important performance metric is the time required to finish processing a single event; which must be less than 132ns. The performance of the Data Combiner will dictate how robust the front end system is to varying event sizes and occupancy distributions.

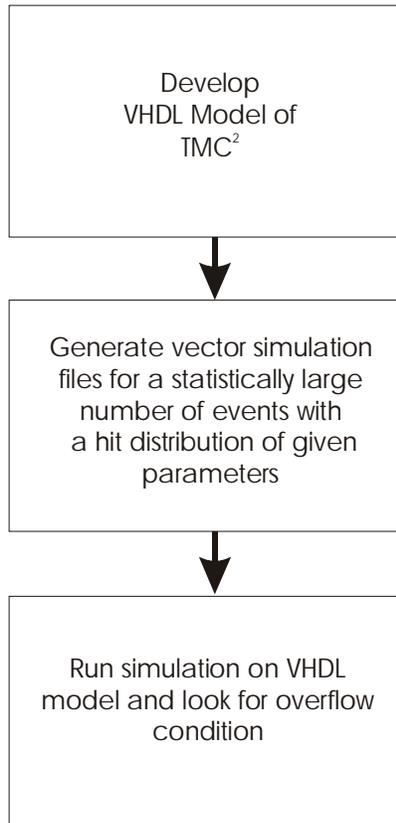
#### 3.1 Performance Metrics

The TMC<sup>2</sup> Data Combiner performance can be quantified with metrics such as:

- Maximum data rate out (in bits per second). This will be 848Mbps with 16 bits parallel out at 53Mhz.
- Data latency from input latch of Data Formatters to output on data link.
- Maximum sustainable average occupancy (same number of hits each event and same even spatial distribution of hits each event).
- Maximum sustainable average occupancy as a function of spatial distribution (same number of hits each event with same spatial distribution each event but not necessarily evenly distributed).
- Maximum sustainable average occupancy when hits follow a Poisson distribution (event to event and spatially).
- Maximum sustainable average occupancy when hits follow a Poisson distribution from event to event but spatially hit probabilities follow a Gaussian-like distribution.
- The maximum burst (burst means a single event with 100% occupancy) rate in terms of probability the TMC<sup>2</sup> can *absorb* without overflow.

#### 3.2 Performance Measurement Methodology

The TMC<sup>2</sup> will be developed in VHDL allowing for simulations to be executed on the design prior to any hardware prototyping. The performance metrics will be measured via simulations for all four target applications (RICH, Muon, EM Calorimeter, and Straws). This section will describe the method used to simulate a Muon 32 channel overthreshold system. While the discussion will focus on Muon, the methods and equations easily transfer to the other three system.



*Figure 7. TMC<sup>2</sup> Performance Testing Flow Chart.*

Figure 7 shows a flow chart describing the performance measurement process. The first step is generating a VHDL model that describes the behavior at the register transfer level. This model does not include any analog delays that may be present in the target FPGA, however, it is sufficient for this performance exercise. The second step is generating a test vector input file that will be fed into the VHDL model. This vector file is a sequential series of events 32 channels wide ('1' represents a hit, and a '0' represents no hit) and deep enough to have statistical confidence in the measured result. The measured result is a binary Pass/Fail where Pass implies no overflow condition occurred (no data was lost due to an overflowing FIFO) and Fail implies an overflow condition did occur somewhere during the simulation.

Before the simulation vector files can be generated, a method for describing the events must be created. Three important parameters are used to describe a sample of events: average occupancy, spatial distribution, and burst probability. A burst is defined as a single event with 100% occupancy. Spatial distribution describes how the hits are physically distributed on the front end board (e.g. each channel has an equal probability of being hit, or a certain small group of "hot" channels are much more likely to be hit than other channels). The average occupancy is the mean number of hits per event divided by the total number channels (32 for Muon).

The spatial distribution of the hits is modeled as a modified gaussian distribution. The probability density function (p.d.f.) used to describe the distribution is given as

$f(x)$  = Probability channel  $x$  will be hit on a given event.

$$f(x) = OccN \left( \prod_{x=0}^{N-1} \text{EXP} \left[ \frac{-(x-\mu)^2}{2\sigma^2} \right] \right)^{-1} \text{EXP} \left( \frac{-(x-\mu)^2}{2\sigma^2} \right)$$

↑
↑  
 Constant Coefficient      Function of x where x is channel number

Where,

- $Occ$  = Average occupancy (0 to 1)
- $N$  = Total number of channels (32 for Muon)
- $x$  = Channel number (0 to 31 for Muon)
- $\mu$  = Center of distribution (0 to 31)
- $\sigma$  = variance of distribution (0 to  $\infty$ )

It is important to note that the above p.d.f. behaves such that

$$\sum_{x=0}^{N-1} f(x) = OccN$$

For example, if Muon has an average occupancy ( $Occ$ ) of 5%, then the sum of each of the 32 probabilities must equal  $32 * .05 = 1.6$ , which implies 1.6 channels are hit (on average) per event.

Figure 8 shows this p.d.f. for a 32 channel Muon system with two different sets of  $\mu$  and  $\sigma$ . Both charts are with an average occupancy ( $Occ$ ) of 5% and 32 channels ( $N$ ). The chart on the left shows a very even distribution (large  $\sigma$ ) with each channel having an equal probability of being hit (5%). The chart on the right, however, shows a lop-sided distribution with the lower numbered channels being much more likely to be hit than the higher numbered channels.

Once the p.d.f. is calculated, and the assumption is made that events are mutually independent and follow a Poisson process, the next step is to generate a sequence of events. Figure 9 represents a run of 100 events with the p.d.f.s. shown in Figure 8. A single rectangular block represents a hit. In both cases, the probability of a burst was set to 2%. Figure 9 shows that the hits are evenly distributed across the front end on the left chart, but are clustered to the lower numbered channels on the right chart. Even though both charts represent the same average occupancy, the distribution of the data is much different and can have an impact on the possibility of the TMC<sup>2</sup> overflowing.

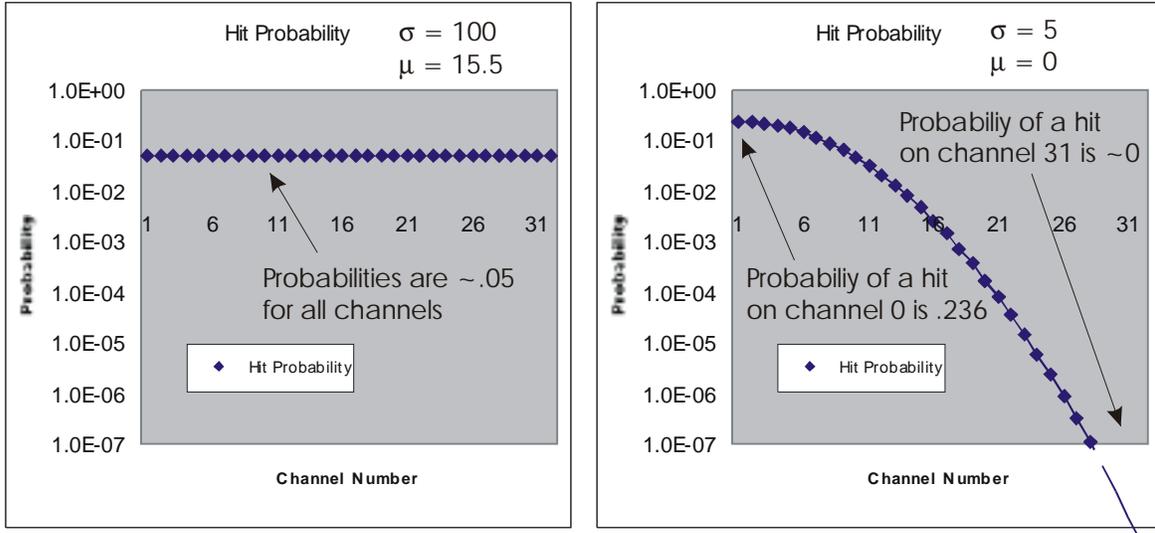


Figure 8. Example probability density functions with two different distribution parameters. Average occupancy is set to 5%.

It should be noted that the actual simulations will require much more than 100 events to prove the TMC<sup>2</sup> will not overflow for a given *Occ*,  $\mu$ , and  $\sigma$ . Once the vector files are generated they will be used to exercise the VHDL model. If the VHDL model shows the TMC<sup>2</sup> to have an overflow condition, it will be considered not capable of handling data with the given set of parameters.

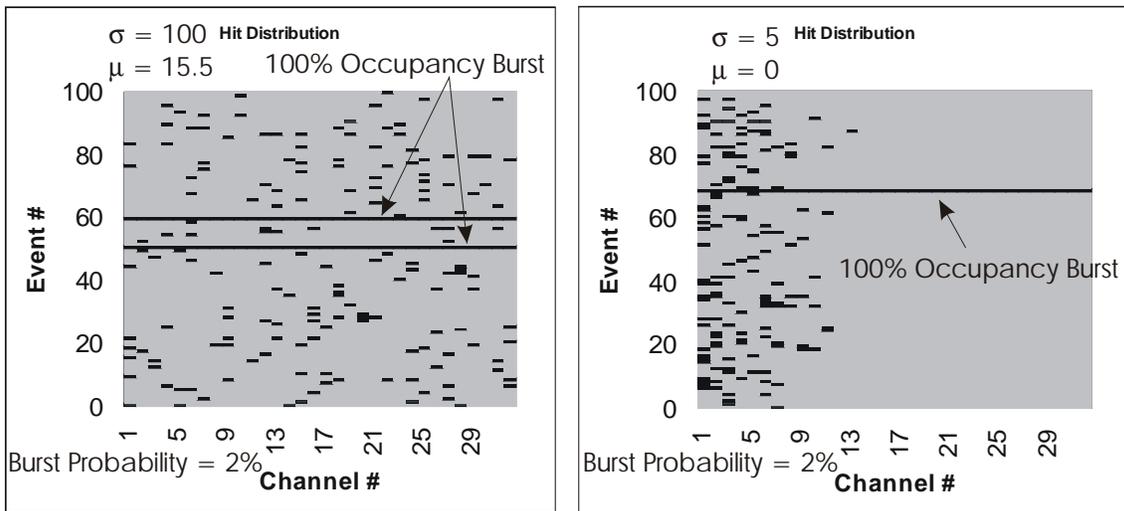


Figure 9. Results of 100 event simulation using p.d.fs. shown in Figure 8. Average occupancies set to 5% in both charts.

Accurate estimates for the actual average occupancies and distributions will depend on physics simulation results and detector geometry. The geometry and results of these physics simulations will be used to determine the appropriate  $Occ$ ,  $\mu$ , and  $\sigma$  parameters in the  $f(x)$  p.d.f. described in this section. It should be noted that physics simulations may show that the  $f(x)$  p.d.f. equation does not accurately describe hit distributions and a new equation may be needed. If so, the TMC<sup>2</sup> performance measurement process remains the same, but a new equation and set of parameters will be used to describe events.

### 3.3 Performance Summary

The VHDL model of the TMC<sup>2</sup> will be fully simulated with events that have occupancies and distributions like those expected to be found in the final BTeV system. Expected occupancies and distributions will be based on results from physics simulations. Results of simulating the TMC<sup>2</sup> will be used to modify the design (if needed), insure the TMC<sup>2</sup> design is adequate for the target BTeV front end readout systems, and provide a quantitative measurement of how much performance margin there is in the design.

#### 4. How the TMC<sup>2</sup> Fits Into the System

The TMC<sup>2</sup> plays an important role in the overall BTeV system. This section briefly describes how the TMC<sup>2</sup> might be placed on a Muon front end board and how the front end boards are linked to the Level 1 Buffers. The examples shown are for Muon, but the same concepts apply for RICH, EM Calorimeter, and Straws.

Figure 10 shows a possible 32 channel Muon front end board with out the tubes or PMTs. Charge from the PMTs is integrated and discriminated at the 8 channel ASDQ chip. The output of this chip is one overthreshold signal per channel which is sent directly into the TMC<sup>2</sup> Data Formatter. The Timing, Monitoring, and Control part of the TMC<sup>2</sup> must communicate the DACs and ADCs to set the ASDQ thresholds and read back ADC readings. The Data Combiner in the TMC<sup>2</sup> sends parallel data to the 8B/10B encoder chips where it is encoded and serialized then sent to the VCSEL/fiber connector assembly for transmission to the Level 1 Buffer.

Figure 11 shows a series of Muon front end boards and their connection to the Level 1 Buffers and the BTeV Monitoring, Timing, & Controls System. Note that there is a dedicated control and monitoring link set for each front end board. Data from six front end boards is sent to one Level 1 Buffer board where it is stored in memory until a trigger decision is made on whether to accept or reject a particular BXNG.

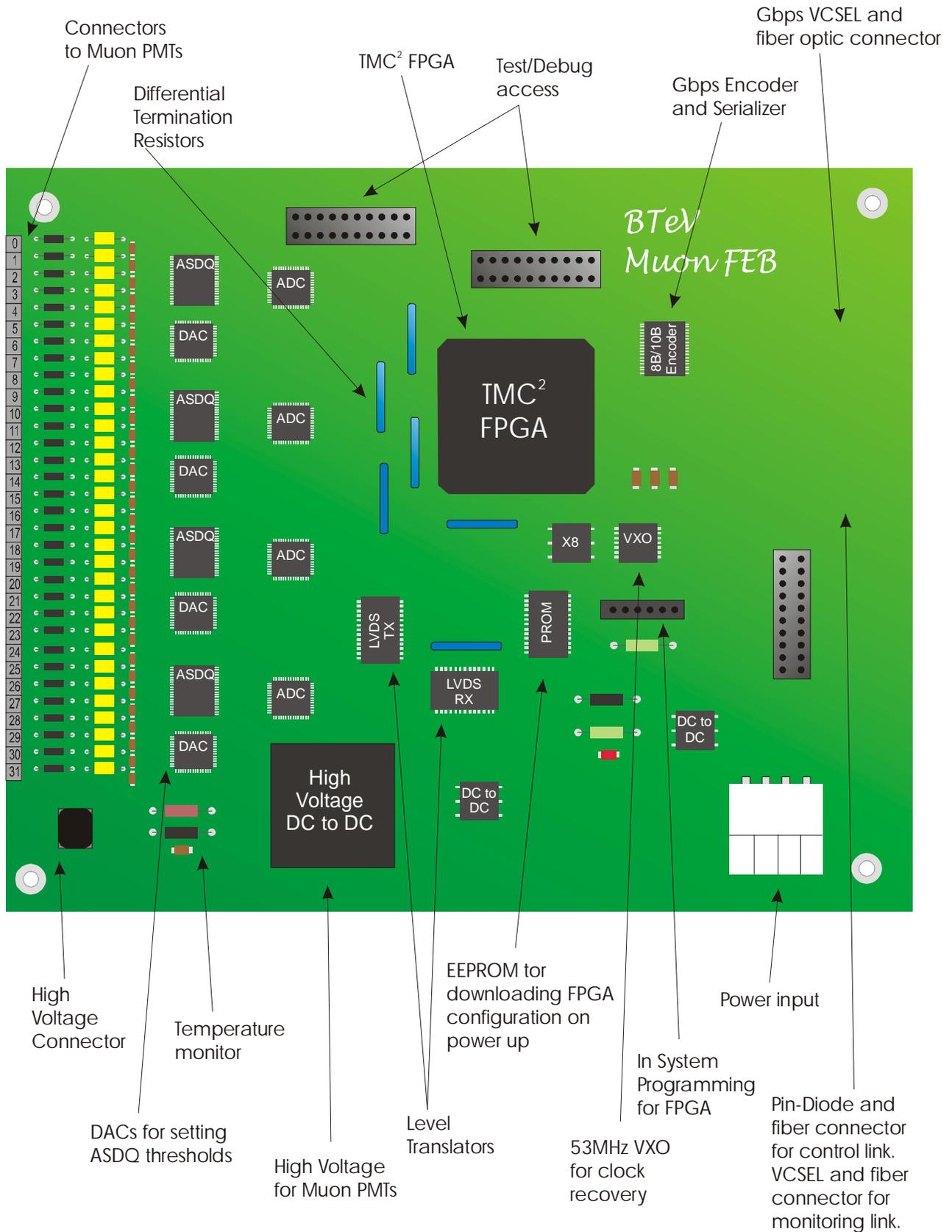


Figure 10. Possible arrangement of Muon front end board.

2160 Front End Boards Total.  
32 channels each front end board for a total of 69120 Muon system channels. Level 1 buffers receive data from 6 front end boards. Data links are Gbps. Monitoring and Control links are ~200Mbps.

Muon TMC<sup>2</sup> FPGA receives 32 channels of differential ASDQ overthreshold data.

Level 1 Buffer receives data and arranges data blocks with the same BXNG together. Data is held until it receives an accept or reject for a particular BXNG. Accepted BXNGs are sent to a data switch for distribution to the processing farm.

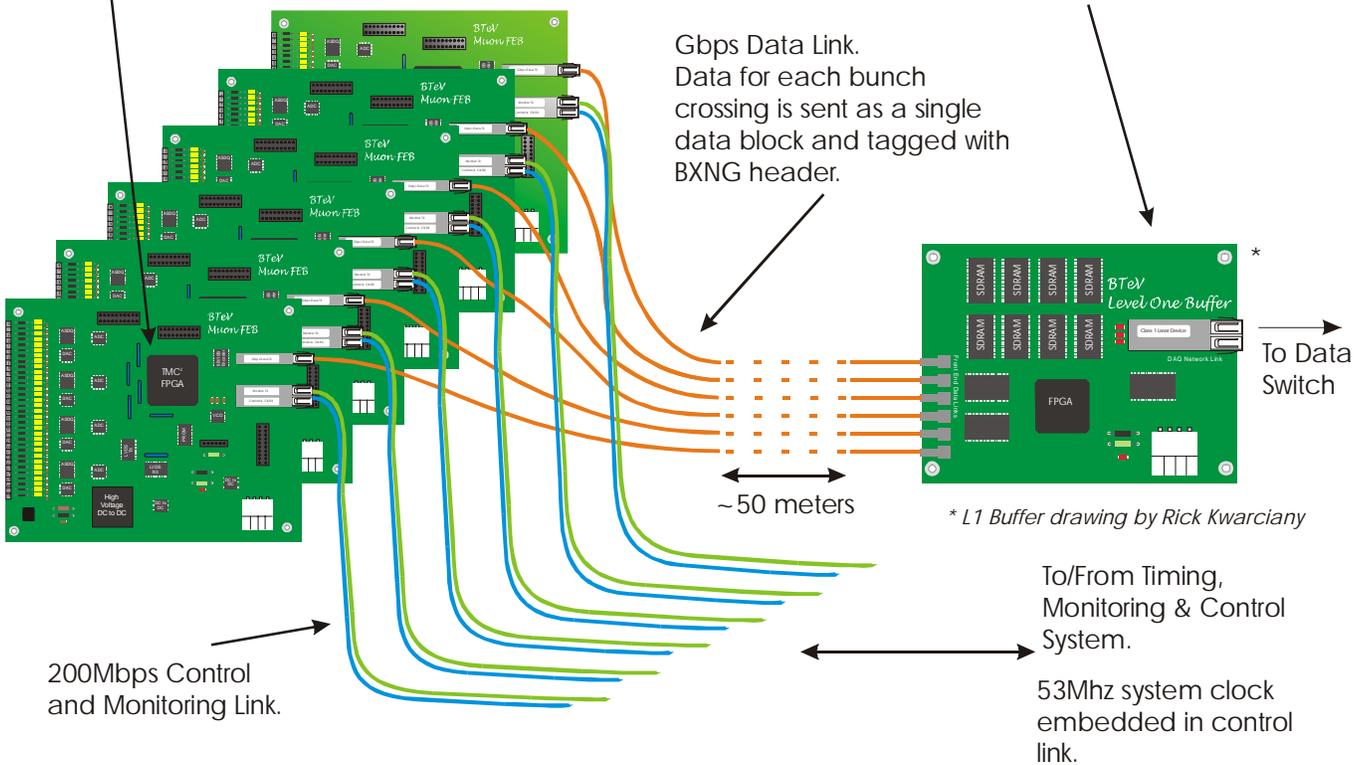


Figure 11. Example of Muon front end boards with TMC<sup>2</sup> and their connection to the Level 1 Buffer.

## 5. Summary

This document described the purpose and functionality of the BTeV TMC<sup>2</sup>, how it will be implemented, how its performance will be measured, and how it will fit into the overall system. The TMC<sup>2</sup> offers a common data combining architecture and data block format across each of its four target applications. This commonality should greatly reduce the engineering development and debug effort required to implement all four systems in addition to the maintenance of the BTeV front end readout electronics at run time.