

# D0 SCL Receiver Preliminary Specification

Original (2/22/98)

Revision 1 (2/27/98)

## **Revision 2 (9/4/98)**

The SCL Receiver specification uses a form factor resembling the proposed PC-MIP Type II mezzanine card standard. This standard uses the same connectors as the PMC mezzanine card standard, but total board area is 60% smaller (47 X 99 mm, approximately 7 square inches).

The proposed SCL receiver mezzanine card form factor differs from PC-MIP in the following ways;

- 1) the P3 connector is removed
- 2) the I/O connector space may be the full mezzanine card width

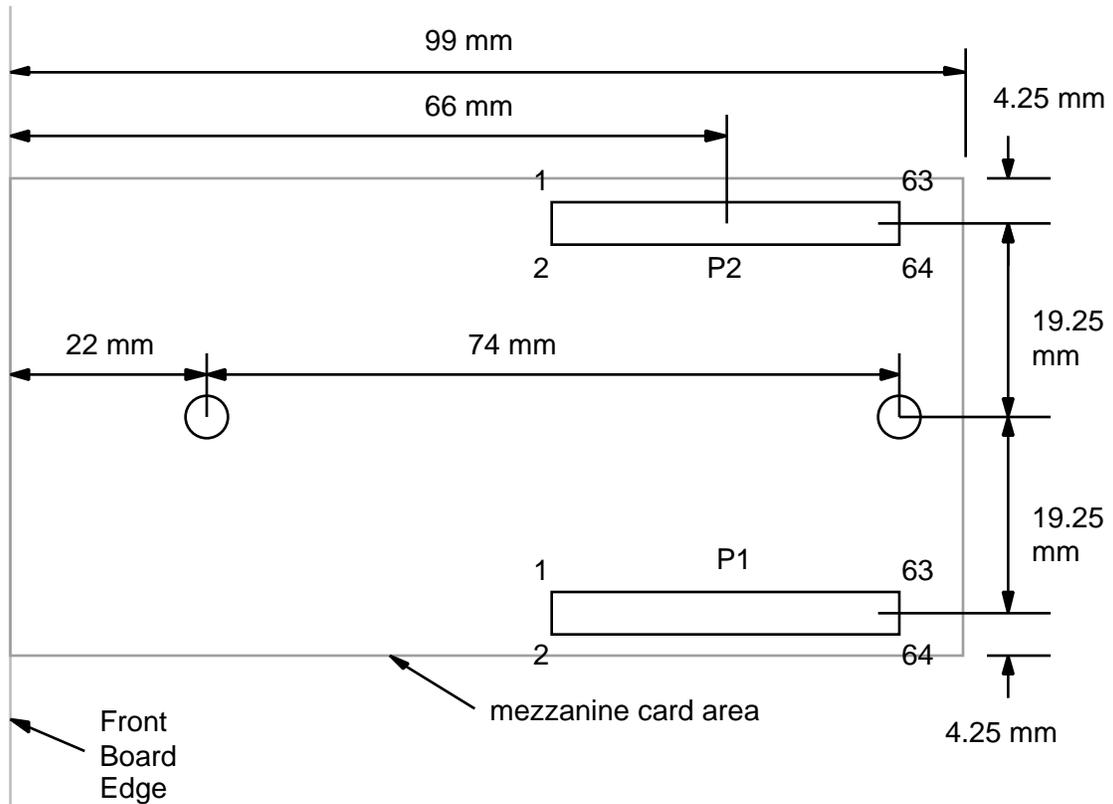
The host circuit board requires two identical SMT connectors. The following are suitable:

Molex 71436-0864 (<http://www.molex.com/product/micro/71436.html>)

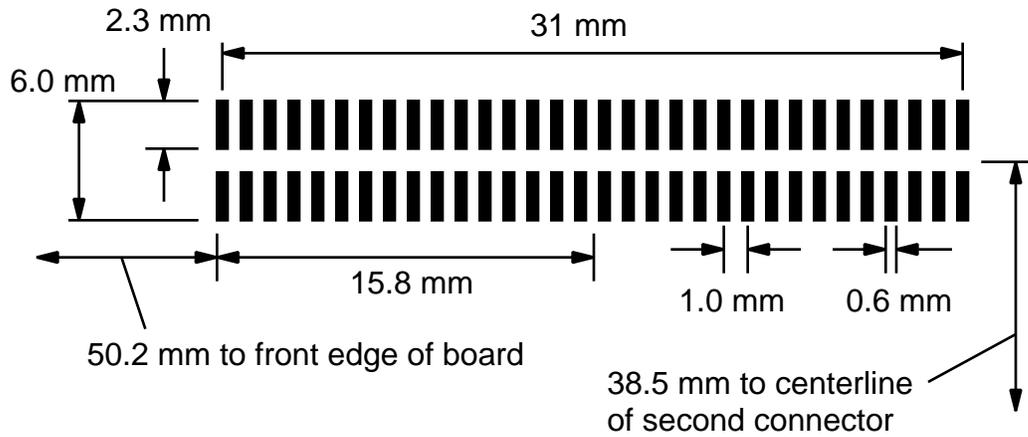
AMP 120532-1

**(Revision 2) - it has been pointed out that there is a potential for misalignment when using the originally specified connectors, if the connectors float during surface mounting. It may be preferable to use the connector version with PCB pegs (Molex 71436-0164) for more precise alignment. This requires adding two reference holes to each connector footprint (see above Molex URL for size and placement information).**

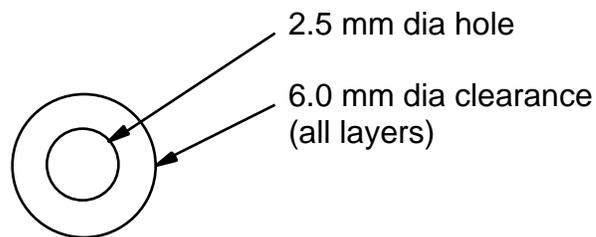
Layout recommendation for host circuit board (including 2 mounting holes, 2 SMT connectors and mezzanine card clearance area). See connector and mounting hole detail on following page.



P1 and P2 footprint (surface mount connectors). [see note on first page (revision 2) concerning addition of connector alignment holes]



Mounting hole detail. [ see note on next page for additional clearance requirement with .09 board thickness]





The following signal names have been assigned per the document "Serial Command Link Description, D-Zero Run II Trigger DAQ System", 24-April-1997;

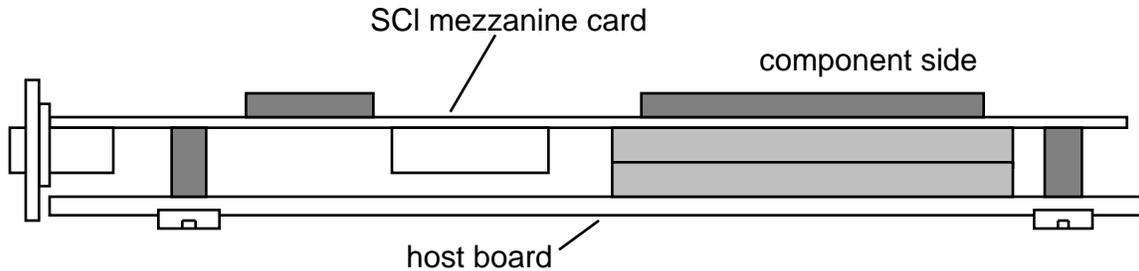
SCL_READY	Serial Command Link Ready Status
SCL_SYNCERROR	Serial Command Link Synchronization Error
SCL_DATAERROR	Serial Command Link Data Error
SCL_ACK	Acknowledge & Clear SCL Error Flags
CLK_53	53 Mhz Clock
CLK_7	7.5 Mhz Clock
CURRENT_TURN[15..0]	Current Turn Number
CURRENT_BX[7..0]	Current BX Number in this Turn
FIRST_PERIOD	First Period in a Turn Marker
BEAM_PERIOD	Period with Beam Marker
SYNC_GAP	Sync Gap Marker (no L1 Accepts)
COSMIC_GAP	Cosmic Gap Marker (only Cosmic L1 Accepts)
SPARE_PERIOD	Spare Period Marker
L1_PERIOD	Period with L1 Accept Issued
L1_ACCEPT	L1 Accept to this Geo Section
L1_TURN[15..0]	Level 1 Turn Number
L1_BX[7..0]	Level 1 BX Number in this Turn
L1_QUAL[15..0]	L1 Accept Qualifiers / Geo Section L3 Transfer Number
L2_PERIOD	Period with L2 Decision Issued
L2_REJECT	This Geo Section L2 Reject
L2_ACCEPT	This Geo Section L2 Accept
INIT_SECTION	Initialize Geographic Section Flag
L1_BUSY	Busy L1 Status
L2_BUSY	Busy L2 Status
L1_ERROR	Error L1 Flag
L2_ERROR	Error L2 Flag
INIT_ACK	Init_Ack Signal to Hub-End
SYNC_LOST	SCL Receiver Synchronization Lost
SPARE_STATUS[1..0]	Spare Status Signals to Hub-End

The following is a suggested (arbitrary) P1/P2 pin assignment. All signals are TTL, low drive.

	P1	P2
1	+5V	+5V
2	+5V	+5V
3	SCL_READY	INIT_SECTION
4	SCL_SYNCERROR	SCL_ACK
5	GND	GND
6	CURRENT_TURN[0]	L1_TURN[0]
7	CURRENT_TURN[1]	L1_TURN[1]
8	CURRENT_TURN[2]	L1_TURN[2]
9	CURRENT_TURN[3]	L1_TURN[3]
10	GND	GND
11	CURRENT_TURN[4]	L1_TURN[4]
12	CURRENT_TURN[5]	L1_TURN[5]
13	GND	GND
14	CURRENT_TURN[6]	L1_TURN[6]
15	CURRENT_TURN[7]	L1_TURN[7]
16	CURRENT_TURN[8]	L1_TURN[8]
17	CURRENT_TURN[9]	L1_TURN[9]
18	GND	GND
19	CURRENT_TURN[10]	L1_TURN[10]
20	CURRENT_TURN[11]	L1_TURN[11]
21	GND	GND
22	CURRENT_TURN[12]	L1_TURN[12]
23	CURRENT_TURN[13]	L1_TURN[13]
24	CURRENT_TURN[14]	L1_TURN[14]
25	CURRENT_TURN[15]	L1_TURN[15]
26	GND	GND
27	CURRENT_BX[0]	L1_BX[0]
28	CURRENT_BX[1]	L1_BX[1]
29	GND	GND
30	CURRENT_BX[2]	L1_BX[2]
31	CURRENT_BX[3]	L1_BX[3]
32	CURRENT_BX[4]	L1_BX[4]
33	CURRENT_BX[5]	L1_BX[5]
34	GND	GND
35	CURRENT_BX[6]	L1_BX[6]
36	CURRENT_BX[7]	L1_BX[7]
37	GND	GND
38	FIRST_PERIOD	L1_QUAL[0]

39	BEAM_PERIOD	L1_QUAL[1]
40	L1_PERIOD	L1_QUAL[2]
41	L1_ACCEPT	L1_QUAL[3]
42	GND	GND
43	SPARE_PERIOD	L1_QUAL[4]
44	L2_PERIOD	L1_QUAL[5]
45	GND	GND
46	L2_REJECT	L1_QUAL[6]
47	L2_ACCEPT	L1_QUAL[7]
48	SCL_DATAERROR	L1_QUAL[8]
49	reserved (NC)	L1_QUAL[9]
50	GND	GND
51	L1_BUSY	L1_QUAL[10]
52	L1_ERROR	L1_QUAL[11]
53	GND	GND
54	L2_BUSY	L1_QUAL[12]
55	L2_ERROR	L1_QUAL[13]
56	INIT_ACK	L1_QUAL[14]
57	SYNC_LOST	L1_QUAL[15]
58	GND	GND
59	SPARE_STATUS[0]	SYNC_GAP
60	SPARE_STATUS[1]	COSMIC_GAP
61	GND	GND
62	GND	GND
63	GND	GND
64	CLK_53	CLK_7

Mezzanine card height is approximately 8 mm. Most of the components are mounted on the top side of the card. Height of the card plus components will not exceed 13.7 mm.



The SCL receiver duplicates the University of Arizona serial data link receiver, with additional on-card demultiplexing. The demultiplexing logic consists of a single Altera 9xxx (208 pin QFP) which will be in-circuit reprogrammable through JTAG.

The SCL receiver local reference clock will be provided by an on-board 53.1 MHz oscillator. Available standard frequencies of 53.125 and 53.088 MHz may be suitable (although they exceed the +/-100 ppm receiver specification). The CLK\_53 output will be driven by the local reference clock when the receiver is not synchronized.

+3.3 Volt power for the receiver will be supplied by an on-board linear regulator.

The front panel status connector will be (subject to change) a 21 pin Micro-D Subminiature (<http://www.molex.com/product/ultimate/8-18.html>). This provides 16 pins for the eight differential RS-485 status signals plus 5 pins for a JTAG front-panel interface.

Drivers for the eight RS-485 signals will be bidirectional (they may be programmed as either input control, or output status signals).

All outputs will be valid 15 ns before the rising edge of CLK\_7 and will remain valid for 15 ns after the rising edge of CLK\_7.