

**Fermi National Accelerator Laboratory**

## **D0 Trigger Distribution System**

### **Serial Link Fanout (SLF)**

--PRELIMINARY--

January 13, 2000

Bill Haynes, Thinh Pham,  
Neal Wilcer and Ted Zmuda

---

1	GENERAL INFORMATION.....	1
1.1	System Introduction .....	1
1.2	Description .....	1
2	THEORY OF OPERATION AND OPERATING MODES .....	2
2.1	Basic Features & Operation .....	2
3	DIAGNOSTIC/DEVELOPMENT SOFTWARE .....	3
3.1	Description of Hardware Test Platform .....	3
3.2	Description of Software Test Platform.....	3
4	INTERFACE SPECIFICATIONS .....	4
4.1	Front Panel Input.....	4
4.2	VME J2 Backplane Inputs.....	4
4.3	VME J3 Backplane Inputs.....	4
4.4	JTAG Programming Connectors .....	4
4.5	Front Panel LEDs .....	4
4.6	DIP Switch Settings .....	5
5	ELECTRICAL & MECHANICAL SPECIFICATIONS .....	6
5.1	Packaging & Physical Size.....	6
5.2	PC Board Construction.....	6
5.3	Power Requirements .....	6
5.4	Cooling Requirements.....	6
6	SAFETY FEATURES & QUALITY ASSURANCE PROCEDURES.....	7
6.1	Module Fusing & Transient Suppression.....	7
	APPENDICES.....	8
A1	List of Component Documentation .....	8
A2	Schematics.....	8
A3	CPLD Equations.....	8
A4	Parts List.....	9

## 1 GENERAL INFORMATION

### 1.1 System Introduction

The D-Zero Trigger DAQ System is used to send L1 and L2 trigger and timing information to 128 geographic sections. This system will also carry status information from these 128 geographic sections back to the L1 and L2 frameworks. The D-Zero Trigger DAQ System consists of 5 modules and a custom J3 backplane installed in a VIPA VME subrack. The 5 modules that make up the system are the Trigger Hub Controller (THC), Trigger Status Concentrator (TSC), Serial Link Fanout (SLF) and the Serial Command Link Receiver (SCLR).

### 1.2 Description

In the D-Zero Trigger DAQ System, a VME controller, a Trigger Hub Controller (THC) and 16 Serial Link Fanout (SLF) boards occupy the front end of a VIPA VME 9U subrack with a custom J3 backplane. The Serial Link Fanout (SLF) is a 9Ux400mm printed circuit board with a form factor based on the VIPA VME standard. The SLF is the host board for eight University of Arizona, Serial Transmitter Daughter Boards. The Serial Link Fanout receives trigger and timing information from the Hub-End and together with the Serial Transmitter Daughter Boards distribute this information to the 128 geographic sections (Figure 1). The serial data arriving at each geographic section is then received by a Serial Command Link Receiver (SCLR).

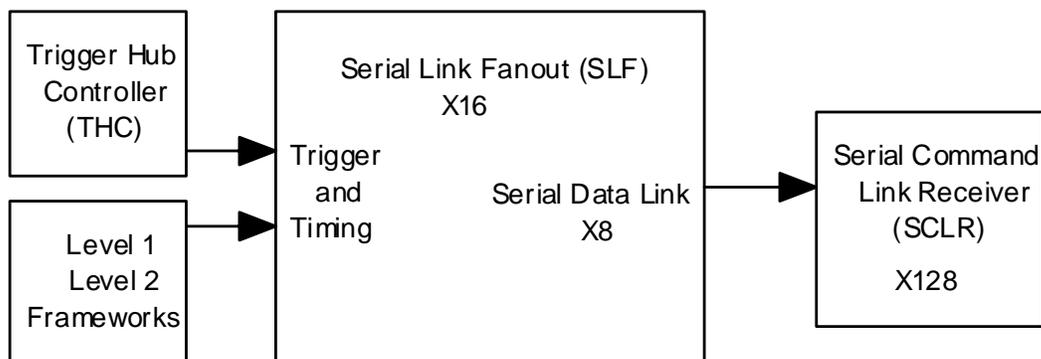


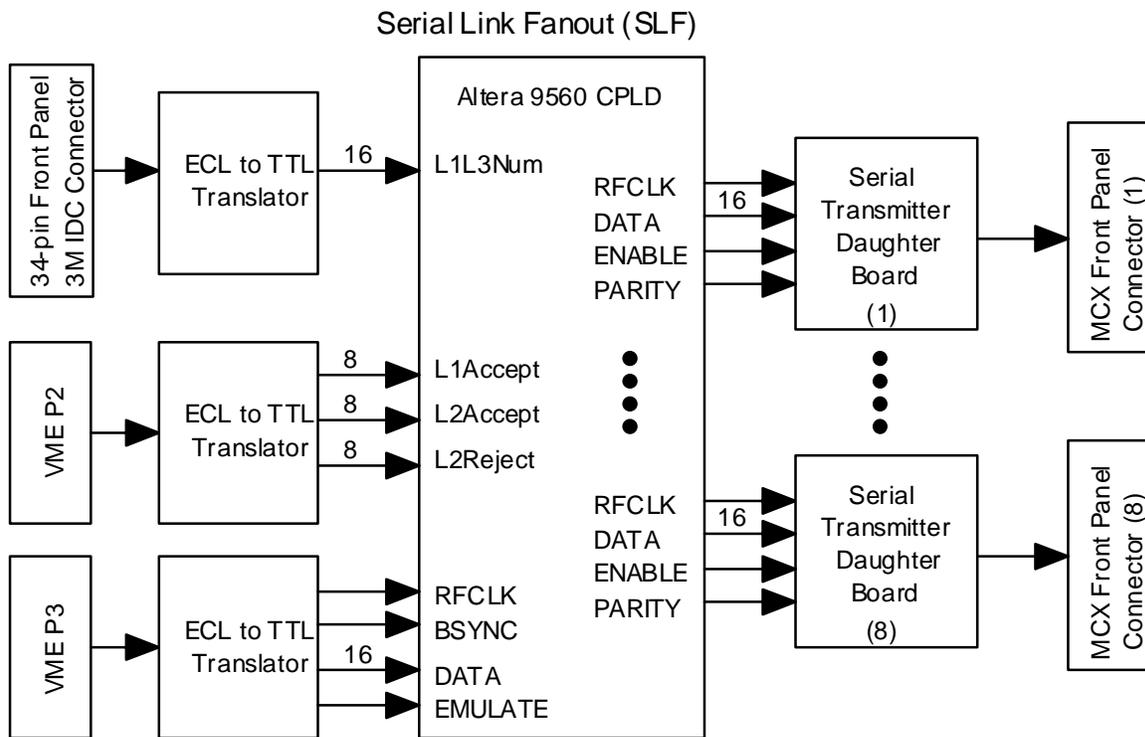
Figure 1

## 2 THEORY OF OPERATION AND OPERATING MODES

### 2.1 Basic Features & Operation

The SLF receives parallel trigger and timing information from the Hub-End through three different ports on the board (Figure 2). Information enters the SLF through a connector on the front panel and from the VME P2 and P3 connectors. The L1-L3 Number from the Level 1 Frameworks enters the board through a 34-pin connector on the front panel. The L1 Accept, L2 Accept and L2 Reject from the Level 1 and Level 2 Frameworks enters the board on the VME P2 connector via the Trigger Status Concentrator (TSC). The remaining trigger and timing information comes from the Trigger Hub Controller (THC) and enters the board on the VME P3 connector via the custom J3 backplane. The incoming data is first translated from ECL to TTL and is then passed on to an Altera 9560 CPLD. The CPLD splits the trigger and timing information into 16-bit wide data busses that carry the information to the eight Serial Link Transmitter Daughter Boards. The information is serialized and then exits the board through eight MCX Type jacks on the front panel.

The SLF has two modes of operation “Normal or “Emulation Mode”. The 9560 CPLD controls the flow of the information for the two operating modes. In “Normal Mode” the trigger and timing information comes from the Level1 and Level2 Frameworks and the Trigger Hub Controller (THC). In “Emulation Mode” all of the trigger and timing information comes from the Trigger Hub Controller (THC) on the J3 backplane. In either mode the 9560 CPLD routes the necessary information to all Serial Transmitter Daughter Boards.



### **3 DIAGNOSTIC/DEVELOPMENT SOFTWARE**

#### **3.1 Description of Hardware Test Platform**

The hardware test platform for the SLF consists mainly of the modules that will be used in the D-Zero Trigger Distribution System. Starting at the beginning of the data path, the modules are the Trigger Hub Controller (THC), the Serial Link Fanout (SLF), the Serial Command Link Receiver (SCLR) and finally the Serial Receiver Test Module (SRTM). To start a test sequence, the THC is loaded with a block of data over the VME bus using a Bit3. The Bit3 also loads the same data block into a memory buffer on the SRTM. The THC and SRTM are then triggered by a command from the Bit3 and the data is transferred through the system where it arrives at the SRTM and is compared with the buffer for errors.

#### **3.2 Description of Software Test Platform**

The software test platform is a Microsoft Excel based program that was provided by D-Zero.

## **4 INTERFACE SPECIFICATIONS**

### **4.1 Front Panel Input**

The SLF receives the L1-L3 Number from the Hub-End on a right angle header (J22) located on the front panel. These signals are for the current 132ns period and are registered on the SLF by the rising edge of the BSYNC signal. Refer to the Serial Link Fanout schematic for the current pin assignments and to the PCB drawing for connector location.

### **4.2 VME J2 Backplane Inputs**

The SLF receives the Level1-Accept, Level2-Accept and Level2-Reject from the Hub-End on the VME J2 backplane user defined I/O pins from the Trigger Status Concentrator (TSC). These signals are for the current 132ns period and are registered on the SLF by the rising edge of the BSYNC signal. Refer to the Serial Link Fanout schematic for the current pin assignments and to the PCB drawing for connector location.

### **4.3 VME J3 Backplane Inputs**

The SLF receives trigger and timing information on the VME J3 custom backplane from the Trigger Hub Controller (THC). Refer to the Serial Link Fanout schematic for the current pin assignments and to the PCB drawing for connector location.

### **4.4 JTAG Programming Connectors**

The SLF has two JTAG connectors for programming of the onboard devices. The first JTAG connector (J4) is for simultaneously programming the eight University of Arizona Serial Transmitter Daughter Boards if the need arises. The second connector (J5) is for programming the SLF's two Altera CPLDs U4 and U8. Refer to the Serial Link Fanout schematic for the current pin assignments and to the PCB drawing for connector and component locations.

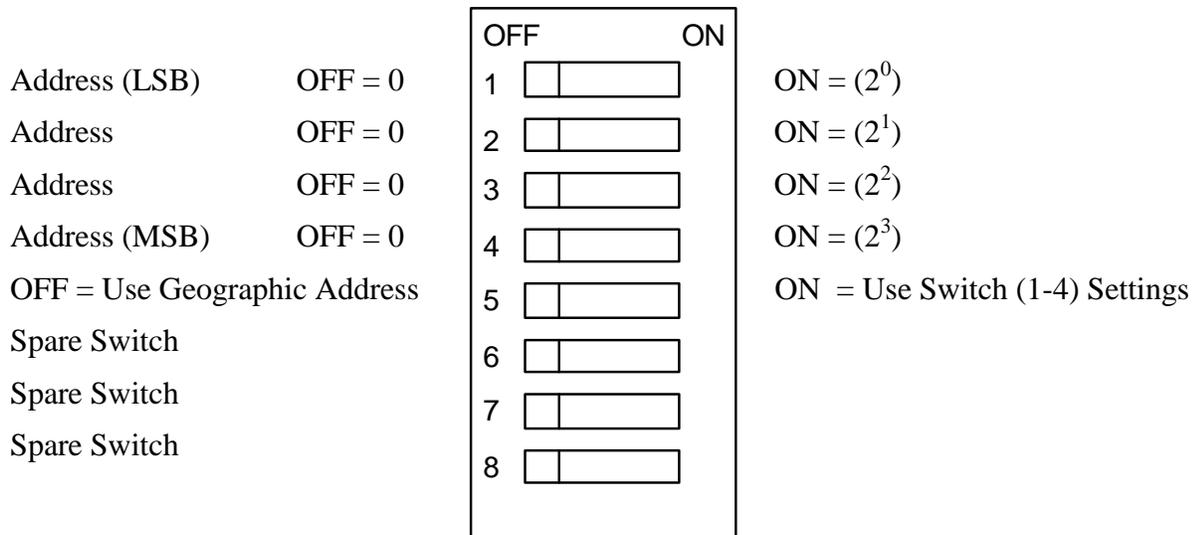
### **4.5 Front Panel LEDs**

The SLF front panel has a 7-segment display that shows the address of the module. This address is derived from decoding the VME geographic address pins. The address range is from 0 to F. This same address is also passed through pins on the backplane to the Trigger Status Concentrator (TSC) in the aligning transition module slot.

The SLF has 6 LED's on the front panel. The top four LEDs are green. The second LED from the bottom is yellow and bottom LED is red. The functions for the LEDs from top to bottom are as follows: +3.3V power, +5V power, -5.2V power, -2V power, BSYNC and Error. The BSYNC LED (yellow) is on when the 7 MHz clock is present. The error LED (red) will turn on when the CPLD state machine is out of synchronization with the 7 MHz (BSYNC) clock.

#### 4.6 DIP Switch Settings

The SLF uses the geographic address pins on the VME bus backplane to set its address. The SLF also has a single eight position DIP switch (Figure 3) that can be used to manually set the module address. The default setting is to use geographic addressing which calls for all switches to be in the OFF position. If it becomes necessary to manually set the module address, care must be taken not to assign the same address to multiple modules. The address appearing on the 7-segment display is also given to the Trigger Status Concentrator (TSC) in the transition module slot opposite the SLF. Assigning the same address to multiple modules will cause problems. Switch positions 1 through 4 set the hexadecimal address of the module. Switch position 5 sets the addressing mode to use the VME geographic addressing (OFF) or to use the switch position (1-4) settings (ON). When switch position 5 is set to ON, the display decimal point will turn on to indicate that mode.



**Figure 3**

## **5 ELECTRICAL & MECHANICAL SPECIFICATIONS**

### **5.1 Packaging & Physical Size**

The SLF is a 9Ux400 VIPA VME module. Refer to the printed circuit board fabrication drawing for component locations and board dimensions. The PCB fabrication document (SLF\_Fab.pdf) is available on the web.

### **5.2 PC Board Construction**

The SLF printed circuit board has 8 layers. The board has 3 signal layers, a +5V power plane, a +3.3V power plane, a -5.2V power plane, a -2V power plane and 1 ground plane. The board thickness is 0.093 +/- 0.008 in.

### **5.3 Power Requirements**

The power requirements are +5V @ 2A, +3.3V @ 5A, -5.2V @ 2A and -2V @ 2A.

### **5.4 Cooling Requirements**

The general cooling requirements are to provide at least 12 CFM of airflow for each SLF module installed in a VIPA VME subrack.

## 6 SAFETY FEATURES & QUALITY ASSURANCE PROCEDURES

### 6.1 Module Fusing & Transient Suppression

The SLF has fusing and transient surge suppression on all incoming power. The locations of the fuses and corresponding power are as follows (Figure 4): F1 is +3.3V power, F2 is +5V power, F3 is -5.2V power and F4 is -2V power. All incoming power passes through ferrite beads (L1-L4) to help suppress noise.

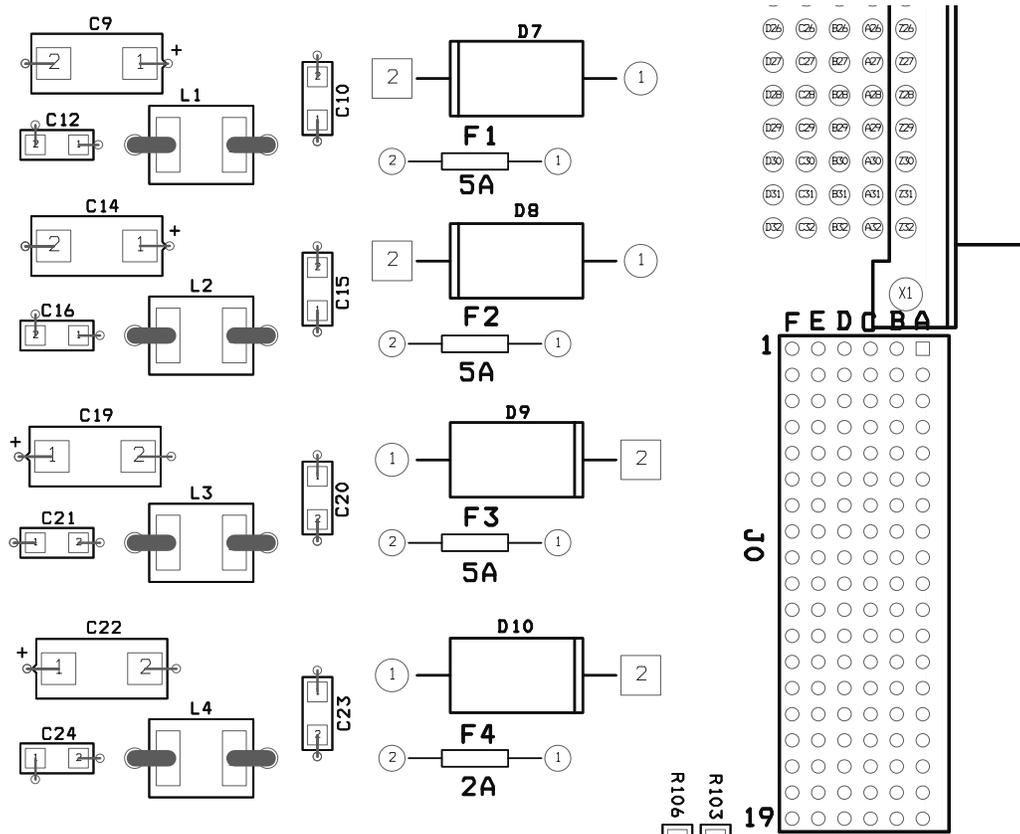


Figure 4

**APPENDICES****A1 List of Component Documentation**

SLF Specifications – SLF\_Spec.pdf

SLF Schematic – SCLR\_Schematic.pdf

SLF CPLD Equations – SLF\_VHDL.pdf and SLF\_ADDR\_DECODE.pdf

SLF PCB Fabrication – SLF\_Fab.pdf

SLF Front Panel Drawing – SLF\_Fpanel.pdf

**A2 Schematics**

The SLF schematic is available on the web in pdf format.

**A3 CPLD Equations**

The VHDL files for the two Altera CPLDs (U4 and U8) are available on the web in pdf format.

**A4 Parts List**

SLF PARTS LIST (Rev. 1 9/9/1999)				Number
ITEM	Manufacturer Part No.	Manufacturer	Part Description	per Board
1	EPM9560ARC208-10	Altera	Altera FPGA 208-pin RQFP (Do Not Order)	1
2	EPM7032SLC44-15	Altera	Altera FPGA, 44-pin PLCC	1
3	MC10H605FN	Motorola	Registered Hex ECL/TTL Translator, 28-pin PLCC	10
4	MC10H116P	Motorola	ECL Triple Line Receiver, 16-pin DIP	1
5	MC10H125P	Motorola	Quad MECL-to-TTL Translator, 16-pin DIP	1
6	MC10H643FN	Motorola	Dual Supply ECL-TTL 1:8 Clock Driver, 28-pin PLCC	1
7	SN74LS123D	TI	Dual One Shot, 16-pin SOIC	1
8	SN74LS244DW	TI	Octal Buffer, 20-pin SOIC	1
9	90HBW08S	Grayhill	Switch, 8 Position DIP, SMT Package	1
10	1N5908 or ICTE-5	Motorola	1500-WATT Transient Voltage Suppressor, Thru-hole	4
11	ECJ-3VB1C104K	Panasonic	0.1 uF Multilayer Ceramic Capacitor, SMT 1206	93
12	ECJ-3VB1C224K	Panasonic	0.22 uF Multilayer Ceramic Capacitor, SMT 1206	26
13	293D476X9010D2T	Sprague	Sprague 47uF Tantalum SMT Cap	6
14	HU-1M5750-401JT	Ceratech	Ferrite Bead, 6A @ 400 Ohms, SMT 5750 Package	4
15	ERJ-8GEYJ51	Panasonic	Resistor 51 Ohm 5% Thick Film 1206 Package	69
16	ERJ-8GEYJ110	Panasonic	Resistor 110 Ohm 5% Thick Film 1206 Package	1
17	ERJ-8GEYJ180	Panasonic	Resistor 180 Ohm 5% Thick Film 1206 Package	1
18	ERJ-8GEYJ200	Panasonic	Resistor 200 Ohm 5% Thick Film 1206 Package	16
19	ERJ-8GEYJ270	Panasonic	Resistor 270 Ohm 5% Thick Film 1206 Package	12
20	ERJ-8GEYJ1.0K	Panasonic	Resistor 1000 Ohm 5% Thick Film 1206 Package	10
21	ERJ-8GEYJ4.7K	Panasonic	Resistor 4700 Ohm 5% Thick Film 1206 Package	14
22	ERJ-8GEYJ22K	Panasonic	Resistor 22K Ohm 5% Thick Film 1206 Package	2
23	ERJ-8GEYJ1.0M	Panasonic	Resistor 1M Ohm 5% Thick Film 1206 Package	4
24	5300H5	Chicago Miniature	Green LED, Front Panel, PCB Mount	4
25	5300H7	Chicago Miniature	Yellow LED, Front Panel, PCB Mount	1
26	5300H1	Chicago Miniature	Red LED, Front Panel, PCB Mount	1
27	HDSP-F501	Hewlett Packard	Numeric Display, 10-pin	1
28	299-93-310-10-001	Mil-Max	Socket, 10-Pin, Right Angle Mount for Numeric Display	1
29	251005	TRACOR	5A Picofuse	4
30	2-331272-2	AMP	Mini-Spring Socket, for 5A Picofuse	8
31	3431-5002	3M	Latch/Eject Right Angle Header, 34-pin	1
32	02-01-160-2101	Harting	VME DIN Right Angle Connector, 5 Row 160 pin Male	3
33	64784	Erni	VME P0, B-95 Female 2mm Right Angle Connector	1
34	SFM-115-02-S-D-LC	Samtec	30 Pin Connector with locking clip, SMT Package	8
35	SFM-105-02-S-D-LC	Samtec	10 Pin Connector with locking clip, SMT Package	8
36	2510-6002UB	3M	Low Profile Header, 10-pin Thru-hole	2
37	3684427	RITTAL	Rittal 9U Front Panel Kit with Injector/Extractor Handles	1
38	3685619	RITTAL	PCB Holder, Front Panel Support	1
39	3606610	RITTAL	Holder/Front Panel Mounting Screw	1
40	3654320	RITTAL	Holder/PCB Mounting Screw	1
41	133-3303-401	Johnson Components	Straight Crimp Type Bulkhead Jack, MCX Type	8
42	133-3403-001	Johnson Components	Straight Crimp Type Plug, MCX Type	8
43	LMR100A-PVC	Times Microwave	0.100" Diameter Low Loss, Low Smoke Coax Cable	1
44	None	None	Fabricate 8.25 inch length Cable with Items 41, 42 and 43	8