Fermi National Accelerator Laboratory

D0 Trigger Distribution System

Serial Command Link Receiver (SCLR)

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1 GENERAL INFORMATION

1.1 System Introduction

The D-Zero Trigger DAQ System is used to send L1 and L2 trigger and timing information to 128 geographic sections. This system will also carry status information from these 128 geographic sections back to the L1 and L2 frameworks. The D-Zero Trigger DAQ System consists of 5 modules and a custom J3 backplane installed in a VIPA VME subrack. The 5 modules that make up the system are the Trigger Hub Controller (THC), Trigger Status Concentrator (TSC), Serial Link Fanout (SLF) and the Serial Command Link Receiver (SCLR).

1.2 Description

The Serial Command Link Receiver (SCLR) is a mezzanine card with a form factor based on the PC_MIP Type II mezzanine card standard. The board's design is derived from the University of Arizona, Serial Receiver Daughter Board. The SCLR mounts on a host board and decodes the information it receives from the Hub-End for each Geographic Section. Serial trigger and timing information is sent to the SCLR by a University of Arizona, Serial Transmitter Daughter Board mounted on the Serial Link Fanout (Figure 1). The SCLR receives this serial trigger and timing information at 1.062Gbits/sec over LMR-200 coaxial cable. The SLCR decodes and de-multiplexes this information and provides it to the host board as 75-bit wide data at a 7.59MHz rate through the mezzanine card to host board TTL interface. The host board also returns 8-bits of status information to the SCLR through the TTL interface. The SCLR then translates these signals to RS-485 and returns them back to the Hub-End via the Trigger Status Concentrator (TSC).

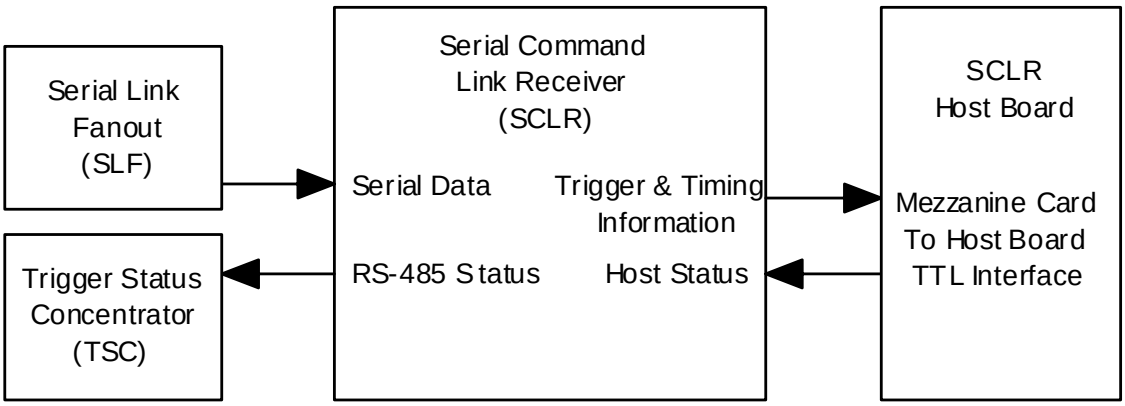

Figure 1

2 THEORY OF OPERATION AND OPERATING MODES

2.1 Basic Features & Operation

Serial trigger and timing information enters the SLCR through a MCX type connector on the board front edge (Figure 2). The data is converted from serial to 20-bit wide parallel by the AMCC serial interface chip. The parallel data then enters a 9000 series Altera CPLD which performs 10B/8B decoding and further de-multiplexes this information and provides it to the host board as 75-bit wide data at a 7.59MHz rate. Data is transferred between the SCLR and host board through two identical 64-pin connectors that serve as the TTL interface. The SCLR also receives 8-bits of status information from the host board through this TTL interface. These status signals are converted to differential RS-485 on the SCLR and are sent through a high density, 26-pin connector mounted on the board front edge. The RS-485 status signals travel over 26-conductor twisted pair cable to the Hub-End via the Trigger Status Concentrator (TSC).

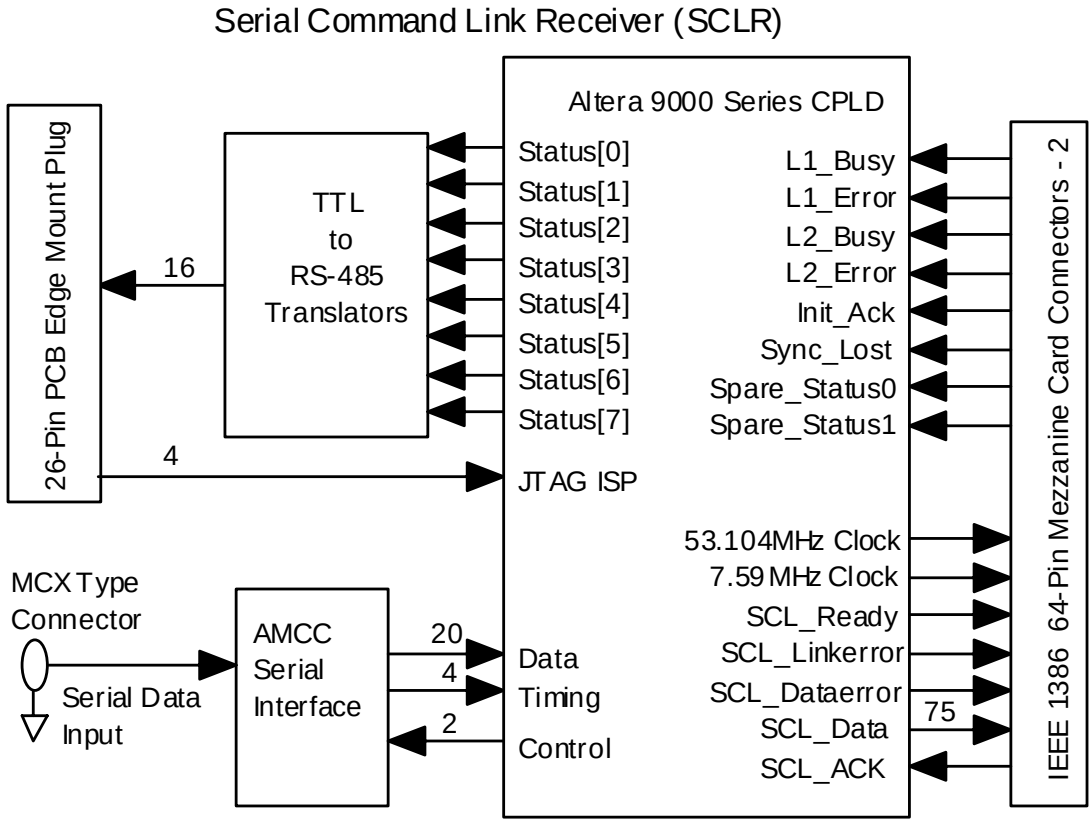

Figure 2

3 DIAGNOSTIC/DEVELOPMENT SOFTWARE

3.1 Description of Hardware Test Platform

The hardware test platform for the SCLR consists mainly of the modules that will be used in the D-Zero Trigger Distribution System. Starting at the beginning of the data path, the modules are the Trigger Hub Controller (THC), the Serial Link Fanout (SLF), the Serial Command Link Receiver (SCLR) and finally the Serial Receiver Test Module (SRTM). To start a test sequence, the THC is loaded with a block of data over the VME bus using a Bit3. The Bit3 also loads the same data block into a memory buffer on the SRTM. The THC and SRTM are then triggered by a command from the Bit3 and the data is transferred through the system where it arrives at the SRTM and is compared with the buffer for errors.

3.2 Description of Software Test Platform

The software test platform is a Microsoft Excel based program that was provided by D-Zero.

4 INTERFACE SPECIFICATIONS

4.1 SCLR to Host TTL Interface

The SCLR has two identical 64-pin connectors that serve as a TTL interface to a host board. The following is a list of the signals between the SCLR and the host board and a brief description of their function. These signals and their names have been assigned per the document "Serial Command Link Description, D-Zero Run II Trigger DAQ System", 24-April-1997.

4.1.1 Signal Descriptions

SCL_ACK (input): This is an active high (true) signal that serves as the reset as well as the command to clear error flags for the SCLR. Whenever the host board asserts this signal high (true), the SCLR will assert SCL_SYNCERROR high (true) and go through a 12ms initialization sequence where it will attempt to lock on to the serial input data stream. If serial input frequency lock is successful, SCL_SYNCERROR will go low (false) so trigger and timing information cycles can start.

SCL_READY (output): This is an active high (true) signal that indicates the serial input is receiving valid trigger and timing information from the Hub-End. When this signal is low (false) the SCLR is receiving serial link synchronization patterns from the SLF. These patterns are sent to maintain frequency lock on the serial link when no trigger and timing information is being sent.

SCL_SYNCERROR (output): This is an active high (true) signal that indicates the receiver has lost frequency lock with the incoming serial data stream. Since loss of frequency lock can occur at any time, this signal can go high (true) at any time and it is not qualified by any other signal. This signal will also go high (true) on power up. The host board is required to set SCL_ACK high (true) to clear this error flag.

SCL_DATAERROR (output): This is an active high (true) signal that indicates the current frame has failed parity check. This signal is not latched, it is high (true) only while the frame that cause the error is present (132ns) on the outputs. This signal is valid 6ns after the rising edge of CLK_7.

CLK_53 (output): This is a free running clock that can have 2 sources. If the SCLR is receiving valid information through the serial input, then this clock will be recovered from the data on the serial input. The frequency will be determined by the clock frequency given to the serial link transmitter by the Hub-End. If the serial cable is not plugged into the SCLR or it has lost lock with the transmitter, then this clock will be provided by an onboard oscillator. The frequency of this oscillator is 53.104MHz.

CLK_7 (output): This clock is present only if the SCLR is receiving valid data and timing information through the serial input. The frequency of this clock is 7.59MHz. The rising edge of this clock is a strobe signal indicating to the host board that all of the outputs are being updated with the information contained in the current frame. This information will be valid 6ns after the rising edge of CLK_7.

The following signals are the trigger and timing information contained in a 132ns period. These SCLR outputs are updated once every 132ns and are valid 6ns after the rising edge of CLK_7.

CURRENT_TURN[15..0] (output): The Current Turn Number.

CURRENT_BX[7..0] (output): The Current Beam Crossing Number in this Turn.

FIRST_PERIOD (output): The First period in a Turn Marker.

BEAM_PERIOD (output): The Period with Beam Marker.

SYNC_GAP (output): The Sync Gap Marker (no L1 Accepts).

COSMIC_GAP (output): The Cosmic Gap Marker (only Cosmic L1 Accepts).

SPARE_PERIOD (output): The Spare Period Marker.

L1_PERIOD (output): The Period with L1 Accept issued.

L1_ACCEPT (output): The L1 Accept issued to this Geographic Section.

L1_TURN[15..0] (output): The L1 Turn Number.

L1_BX[7..0] (output): The L1 Beam Crossing Number in this Turn.

L1_QUAL[15..0] (output): The L1 Accept Qualifier Number / Geographic Section L3 Transfer Number.

L2_PERIOD (output): The Period with L2 Decision issued.

L2_ACCEPT (output): The L2 Accept issued to this Geographic Section.

L2_REJECT (output): The L2 Reject issued to this Geographic Section.

INIT_SECTION (output): The initialize flag issued to this Geographic Section.

The following status signals are continuously driven to TTL levels by the host board and are received by the SCLR. The signals are then translated to RS-485 and are sent to the Trigger Status Concentrator (TSC).

L1_BUSY (input): The L1 Busy Status.

L2_BUSY (input): The L2 Busy Status.

L1_ERROR (input): The L1 Error Flag.

L2_ERROR (input): The L2 Error Flag.

INIT_ACK (input): The Initialize Acknowledge returned to the Hub-End.

SYNC_LOST (input): The host board returning SCLR synchronization lost flag to the Hub-End.

SPARE_STATUS[1..0] (input): The spare status signals to the Hub-End.

4.1.2 Pin Assignment

Table 1

Pin #	P1 Signal	Type	P2 Signal	Type
1	+5V	Power	+5V	Power
2	+5V	Power	+5V	Power
3	SCL_READY	Output	INIT_SECTION	Output
4	SCL_SYNCERROR	Output	SCL_ACK	Input
5	GND	Ground	GND	Ground
6	CURRENT_TURN[0]	Output	L1_TURN[0]	Output
7	CURRENT_TURN[1]	Output	L1_TURN[1]	Output
8	CURRENT_TURN[2]	Output	L1_TURN[2]	Output
9	CURRENT_TURN[3]	Output	L1_TURN[3]	Output
10	GND	Ground	GND	Ground
11	CURRENT_TURN[4]	Output	L1_TURN[4]	Output
12	CURRENT_TURN[5]	Output	L1_TURN[5]	Output
13	GND	Ground	GND	Ground
14	CURRENT_TURN[6]	Output	L1_TURN[6]	Output
15	CURRENT_TURN[7]	Output	L1_TURN[7]	Output
16	CURRENT_TURN[8]	Output	L1_TURN[8]	Output
17	CURRENT_TURN[9]	Output	L1_TURN[9]	Output
18	GND	Ground	GND	Ground
19	CURRENT_TURN[10]	Output	L1_TURN[10]	Output
20	CURRENT_TURN[11]	Output	L1_TURN[11]	Output
21	GND	Ground	GND	Ground
22	CURRENT_TURN[12]	Output	L1_TURN[12]	Output
23	CURRENT_TURN[13]	Output	L1_TURN[13]	Output
24	CURRENT_TURN[14]	Output	L1_TURN[14]	Output
25	CURRENT_TURN[15]	Output	L1_TURN[15]	Output
26	GND	Ground	GND	Ground
27	CURRENT_BX[0]	Output	L1_BX[0]	Output
28	CURRENT_ BX[1]	Output	L1_BX[1]	Output
29	GND	Ground	GND	Ground
30	CURRENT_ BX[2]	Output	L1_BX[2]	Output
31	CURRENT_ BX[3]	Output	L1_BX[3]	Output
32	CURRENT_ BX[4]	Output	L1_BX[4]	Output

Pin #	P1 Signal	Type	P2 Signal	Type
33	CURRENT_ BX[5]	Output	L1_BX[5]	Output
34	GND	Ground	GND	Ground
35	CURRENT_ BX[6]	Output	L1_BX[6]	Output
36	CURRENT_ BX[7]	Output	L1_BX[7]	Output
37	GND	Ground	GND	Ground
38	FIRST_PERIOD	Output	L1_QUALFIER[0]	Output
39	BEAM_PERIOD	Output	L1_QUALFIER[1]	Output
40	L1_PERIOD	Output	L1_QUALFIER[2]	Output
41	L1_ACCEPT	Output	L1_QUALFIER[3]	Output
42	GND	Ground	GND	Ground
43	SPARE_PERIOD	Output	L1_QUALFIER[4]	Output
44	L2_PERIOD	Output	L1_QUALFIER[5]	Output
45	GND	Ground	GND	Ground
46	L2_REJECT	Output	L1_QUALFIER[6]	Output
47	L2_ACCEPT	Output	L1_QUALFIER[7]	Output
48	SCL_DATAERROR	Output	L1_QUALFIER[8]	Output
49	RESERVED	No Connect	L1_QUALFIER[9]	Output
50	GND	Ground	GND	Ground
51	L1_BUSY	Input	L1_QUALFIER[10]	Output
52	L1_ERROR	Input	L1_QUALFIER[11]	Output
53	GND	Ground	GND	Ground
54	L2_BUSY	Input	L1_QUALFIER[12]	Output
55	L2_ERROR	Input	L1_QUALFIER[13]	Output
56	INIT_ACK	Input	L1_QUALFIER[14]	Output
57	SYNC_LOST	Input	L1_QUALFIER[15]	Output
58	GND	Ground	GND	Ground
59	SPARE_STATUS[0]	Input	SYNC_GAP	Output
60	SPARE_STATUS[1]	Input	COSMIC_GAP	Output
61	GND	Ground	GND	Ground
62	GND	Ground	GND	Ground
63	GND	Ground	GND	Ground
64	CLK_53	Output	CLK_7	Output

4.2 Serial Input

The SCLR has a MCX type right angle jack receptacle (Johnson #133-3701-321) mounted on the front edge of the printed circuit board. The SCLR receives serial trigger and timing information on a coaxial cable at 1.062Gbits/sec from the Hub-End via the Serial Link Fanout (SLF) through this connector (Figure 3).

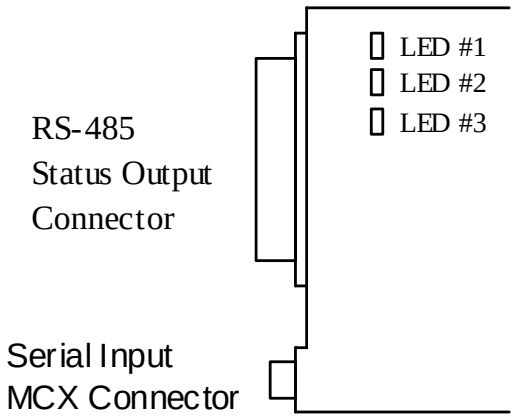

Figure 3

4.3 Status Output

The SCLR has a high density, 26-pin connector (Robinson Nugent # P50E-026-P1-SR1-TG) mounted on the front edge of the printed circuit board (Figure 2). The SCLR receives 8-bits of status information through the TTL interface from the host board. The status signals are converted to differential RS-485 and sent through this connector to the Hub-End via the Trigger Status Concentrator (TSC). The current signal assignment for this status information is shown in Table 2.

This connector is also used for in-system programming of the on-board CPLD. A separate card is available to adapt the RS-485 Status Connector to an Altera Bit Blaster or Byte Blaster.

4.3.1 Status Connector Pin Assignments

Table 2

Pin #	Signal Name	Pin #	Signal Name	Description
1	L1_BUSY	2	L1_BUSY*	RS-485, Level 1 Busy to Hub-End
3	L1_ERROR	4	L1_ERROR*	RS-485, Level 1 Error to Hub-End
5	L2_BUSY	6	L2_BUSY*	RS-485, Level 2 Busy to Hub-End
7	L2_ERROR	8	L2_ERROR*	RS-485, Level 2 Error to Hub-End
9	SYNC_LOST	10	SYNC_LOST*	RS-485, Serial Link Synchronization Lost to Hub-End
11	INIT_ACK	12	INIT_ACK*	RS-485, Initialization Acknowledge to Hub-End
13	SPARE[0]	14	SPARE*[0]	RS-485, Spare Status to Hub-End
15	SPARE[1]	16	SPARE*[1]	RS-485, Spare Status to Hub-End
17	Shorted to 18	18	Shorted to 17	TSC check for disconnected cable
19	NC	20	NC	No PCB Connection/Spare pins
Pin #	**Signal**	**Description**		
21	+5V (Fused)	Power for CPLD in-system programming hardware		
22	TCK	CPLD JTAG BST interface for in-system programming		
23	TMS	CPLD JTAG BST interface for in-system programming		
24	TDI	CPLD JTAG BST interface for in-system programming		
25	TDO	CPLD JTAG BST interface for in-system programming		
26	GND	PCB Ground		

4.4 LED Indicators

The SCLR has 3 surface mount LED's near the RS-485 connector (Figure 2). LED #1 is the +5V power indicator. LED #2 is the +3.3V power indicator. The function of LED #3 is programmable. Currently, LED #3 is programmed to be on when the SCLR is receiving valid trigger and timing information.

5 ELECTRICAL & MECHANICAL SPECIFICATIONS

5.1 Packaging & Physical Size

Figure 4 shows the recommended layout for the host printed circuit board.

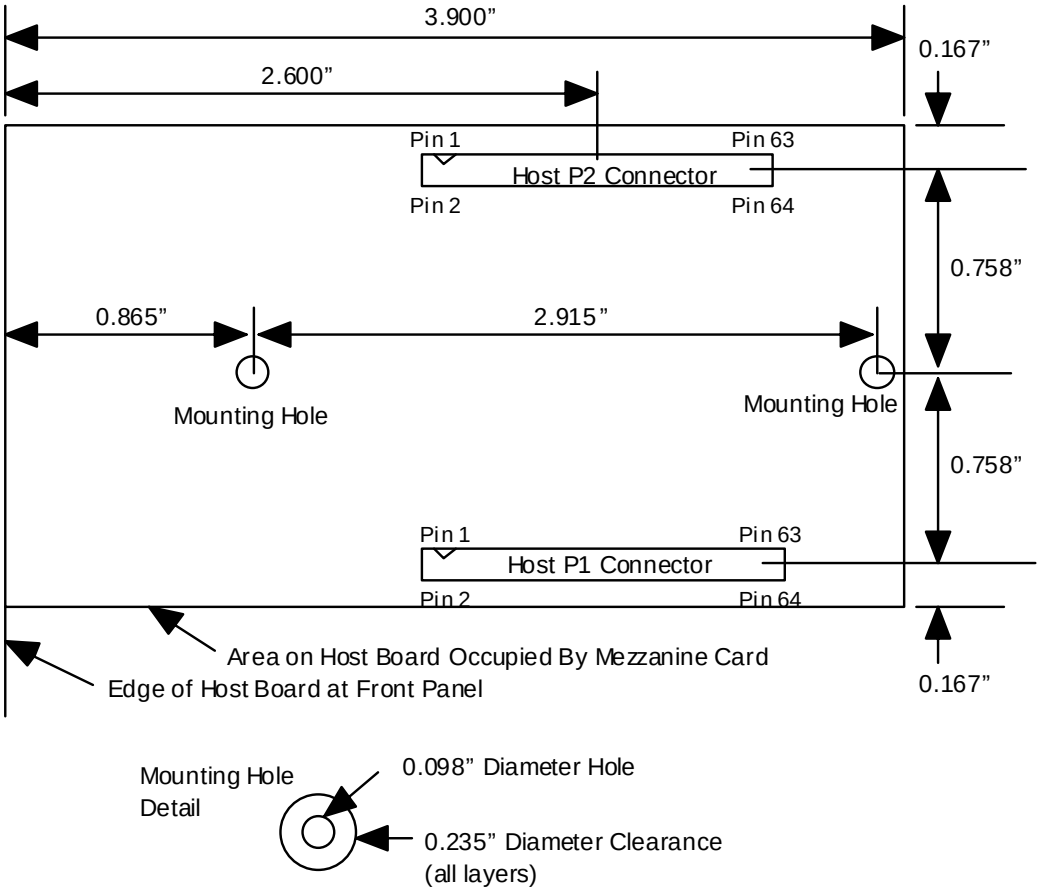

Figure 4

If the recommended layout guidelines are followed, the front edge of the SCLR printed circuit board will line up with the edge of the host printed circuit board at the front panel. This layout will make the I/O connectors on the SCLR accessible through the host front panel.

There are two manufacturers for the two identical 64-pin surface mount connectors for P1 and P2 on the host board. It is recommended that the host board use the surface mount connectors with the locator posts for more precise alignment. The surface mount connectors without the locator posts may float during assembly and cause insertion/extraction problems.

Vendor	**Part Number with Locator Posts**
AMP	71436-0164
Molex	120525-1

The specifications and recommended printed circuit board layout for these connectors are available on the manufacturers web site.

Figure 5 shows the dimensions (in inches) of the I/O connectors and their positions when the SCLR is mounted on the host board.

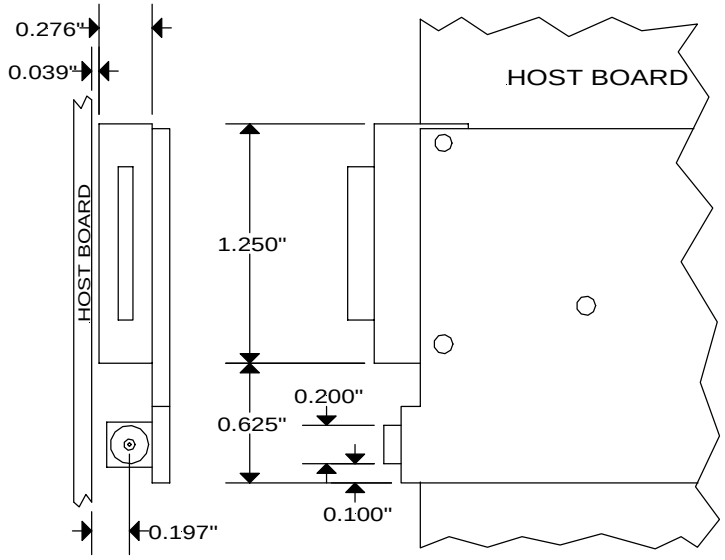

Figure5

Figure 6 shows the overall dimensions (in inches) of the SCLR printed circuit board. The figure also shows the two mounting holes that attach it to the host board. The mounting hardware for the SCLR consists of two 8mm threaded spacers and four 2.5mm screws. This mounting hardware will be provided with the board.

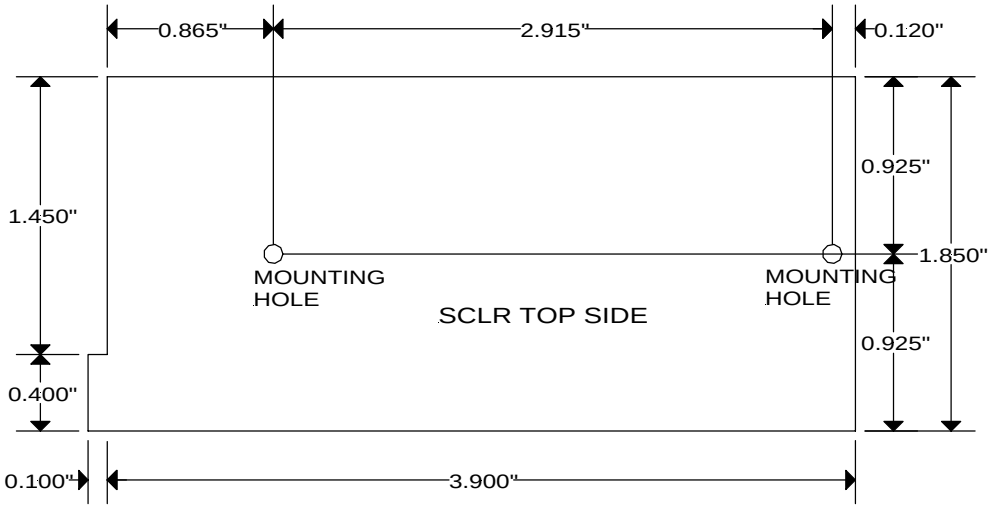

Figure 6

5.2 PC Board Construction

The SCLR printed circuit board has 8 layers. The board has 4 signal layers, a +5V power plane, a +3.3V power plane and 2 ground planes. The board thickness is 0.063 +/- 0.008 in.

5.3 Power Requirements

The host board is required to supply +5V @ 2A to the SCLR.

5.4 Cooling Requirements

There are no special cooling requirements for the SCLR.

6 SAFETY FEATURES & QUALITY ASSURANCE PROCEDURES

5.3 Module Fusing & Transient Suppression

The SCLR does not fuse the incoming +5V power from the host board. The SCLR relies on the host board fusing for protection. However, the SCLR does have transient suppression on the +5V power.

The CPLD on the SCLR uses the RS-485 Output Status Connector (Figure 2) for In-system programming. To implement this option one of the pins on the connector has to provide +5V power to the programmer hardware. The SCLR does fuse this pin to protect the RS-485 Output Status cable in case of a short circuit condition.

A APPENDICES

A1 List of Component Documentation

SCLR Specifications – SCLR_Spec.pdf

SCLR Schematic – SCLR_Schematic.pdf

SCLR CPLD Equations – SCLR_VHDL.pdf

SCLR PCB Fabrication – SCLR_Fab.pdf

A2 Schematics

The SCLR schematic is available on the web in pdf format.

A3 CPLD Equations

The CPLD equations are available on the web in pdf format.

A4 Timing Diagrams

Figure 7 shows the power on initialization sequence. SCL_SYNCERROR will go high (true) when power is first applied to the SCLR. This signal will remain high (true) until the host board asserts SCL_ACK high (true) for a minimum of 38ns (H2). The SCLR will then go through a 12ms (D2) initialization cycle where it will attempt to lock on to the incoming serial data. If the initialization cycle is successful, SCL_SYNCERROR will go low (false) and the data cycle can start.

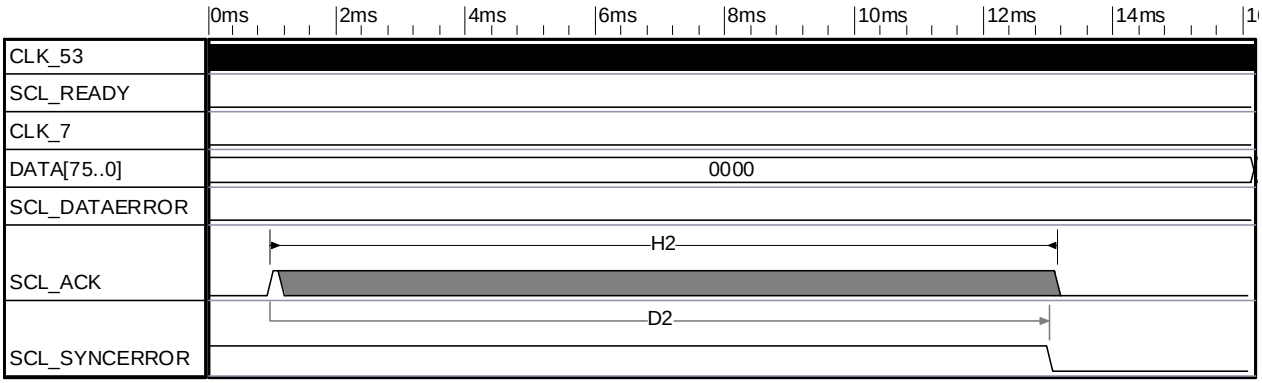

Figure 7

Figure 8 shows the timing for data cycles. First, SCL_READY goes high (true) 4ns (D0) after CLK_53 when valid trigger and timing information arrive on the serial link. Second, when the current frame has completely arrived, the trigger and timing signals change state and are stable 6ns (D1) after CLK_7 goes high (true). All 75 trigger and timing signals hold for 132ns (H0) until the next frame arrives. Figure 8 also shows the timing for a frame error. The SCL_DATAERROR will transition high (true) 6ns (D2) after CLK_7 on a data frame that fails parity check and will transition low (false) 6ns (D3) after CLK_7 on the next data frame that passes parity check. Finally, if trigger and timing information stops arriving on the serial link, SCL_READY will go low and CLK_7 will remain low (false).

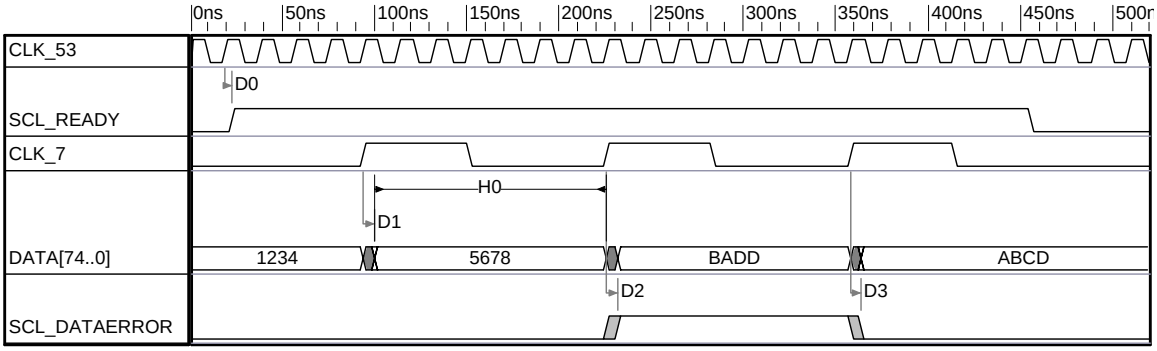

Figure 8

A5 Parts List

			Serial Command Link Receiver (SCLR) Parts List 10/3/1999	
				Number
	Manufacturer	Manufacturer	Part Description	per
ITEM	Part No.			Board
1	EPM9320ARC208-10	Altera	Altera CPLD 208-pin RQFP	1
2	S2043B-10	Applied Micro Circuits	High Speed Serial Receiver, 52 pin PQFP	1
3	IVA-05208	Hewlett Packard	MMIC 1.5GHz Variable Gain Amplifier, SO-8 Package	1
4	DS3696AM	National Semiconductor	RS-485 Transceiver, 8-pin SOIC	8
5	LM3940IMP-3.3	National Semiconductor	5V to 3.3V Regulator, SOT-223 Package	1
6	JITO-2-DC3AE-53.104MHz	Fox Electronics	53.104 MHz Oscillator, MIN-6 SMD	1
7	ECU-V1H101JCG	Panasonic or Equivalent	100 pF SMT Capacitor 0805 Package, NPO	17
8	ECU-V1H100DCN	Panasonic or Equivalent	10pF SMT Capacitor 0805 Package, NPO	1
9	ECU-V1H471JCX	Panasonic or Equivalent	470 pF SMT Capacitor 0805 Package, NPO	10
10	ECU-V1H103KBG	Panasonic or Equivalent	.01uF SMT Capacitor 0805 Package, X7R	9
11	ECJ-2VF1E104Z	Panasonic or Equivalent	0.1 uF SMT Bypass Capacitor SMT 0805 Package, Y5V	25
12	ECJ-2VF1E224Z	Panasonic or Equivalent	0.22 uF SMT Bypass Capacitor SMT 0805 Package, Y5V	20
13	293D476X9010D2T	Sprague or Equivalent	Sprague 47uF Tantalum SMT Cap	2
14	ELJ-ND27NKF	Panasonic or Equivalent	Inductor 27nH 10% SMT 0805 Package	1
15	HI2220P601R	Steward	Ferrite Chip, 4Amp, 600 Ohms, SMT 2220 Package	1
16	LI0805D121R	Steward	Ferrite Chip, 400mA, 120 Ohms, SMT 0805 Package	3
17	ERJ-6ENF13.0	Panasonic or Equivalent	Resistor 13.0 Ohm 1% Thick Film 0805 Package	1
18	ERJ-6ENF51.1	Panasonic or Equivalent	Resistor 51.1 Ohm 1% Thick Film 0805 Package	2
19	ERJ-6ENF100	Panasonic or Equivalent	Resistor 100 Ohm 1% Thick Film 0805 Package	10
20	ERJ-6ENF182	Panasonic or Equivalent	Resistor 182 Ohm 1% Thick Film 0805 Package	3
21	ERJ-6GEYJ2.2KV	Panasonic or Equivalent	Resistor 2.2K Ohm 5% Thick Film 0805 Package	2
22	ERJ-6GEYJ270V	Panasonic or Equivalent	Resistor 270 Ohm 5% Thick Film 0805 Package	1
23	ERJ-6GEYJ1.0KV	Panasonic or Equivalent	Resistor 1.0K Ohm 5% Thick Film 0805 Package	4
24	ERJ-6GEYJ10KV	Panasonic or Equivalent	Resistor 10K Ohm 5% Thick Film 0805 Package	4
25	133-3701-321	Johnson Conponents	Right Angle PCB Mount Coax Connector, MCX Type	1
26	P50E-026-P1-SR1-TG	Robinson Nugent	RN PAK-50 Board Mount Right Angle IDC Plug	1
27	P25E-026-S-TG	Robinson Nugent	RN PAK-50 P25E Series 50 Mil IDC Socket	1
28	71439-0164 or 120521-1	Molex or AMP	IEEE 1386 Mezzanine 64-pin SMT Connector with locator posts	2
29	160-1169-1-ND	DigiKey or Equivalent	Green SMT LED 1206 Package	2
30	160-1170-1-ND	DigiKey or Equivalent	Yellow SMT LED 1206 Package	1
31	MINISMDC035-2	Raychem	PolySwitch Resettable Fuse, 6V @ 0.35A	1
32	923345-01	3M	0.100" Wire Jumper	4
33	ERJ-6GEYJ1.5KV	Panasonic or Equivalent	Resistor 1.5K Ohm 5% Thick Film 0805 Package	2
34	2.5mmX8mm	Maryland Metrics	Threaded Spacer, 2.5mm Thread, 8mm Length	2
35	2.5mmX4mm	Maryland Metrics	Binder Head Screw, 2.5mm Thread, 4mm Length	4