D0 Trigger Pinout

TSC Pinout

		Z row	A row	B row	C row	D row
	1	MPR	D00	*BBSY	D08	VPC
	2	GND	D01	*BCLR	D09	GND
	3	MCLK	D02	*ACFAIL	D10	+V1
	4	GND	D03	*BGIN0	D11	+V2
	5	MSD	D04	*BGOUT0	D12	RSVU
	6	GND	D05	*BGIN1	D13	-V1
	7	MMD	D06	*BGOUT1	D14	-V2
	8	GND	D07	*BGIN2	D15	RSVU
	9	MCTL	GND	*BGOUT2	GND	GAP*
	10	GND	SYSCLK	*BGIN3	*SYSFAIL	GA0*
	11	RESP*	GND	*BGOUT3	*BERR	GA1*
	12	GND	*DS1	*BR0	*SYSRESET	+3.3V
	13	RSVBUS	*DS0	*BR1	*LWORD	GA2*
	14	GND	*WRITE	*BR2	AM5	+3.3V
	15	RSVBUS	GND	*BR3	A23	GA3*
P1/J1	16	GND	*DTACK	AM0	A22	+3.3V
	17	RSVBUS	GND	AM1	A21	GA4*
	18	GND	*AS	AM2	A20	+3.3V
	19	RSVBUS	GND	AM3	A19	RSVBUS
	20	GND	*IACK	GND	A18	+3.3V
	21	RSVBUS	*IACKIN	SERCLK	A17	RSVBUS
	22	GND	*IACKOUT	*SERDAT	A16	+3.3V
	23	RSVBUS	AM4	GND	A15	RSVBUS
	24	GND	A07	*IRQ7	A14	+3.3V
	25	RSVBUS	A06	*IRQ6	A13	RSVBUS
	26	GND	A05	*IRQ5	A12	+3.3V
	27	RSVBUS	A04	*IRQ4	A11	LI/I*
	28	GND	A03	*IRQ3	A10	+3.3V
	29	RSVBUS	A02	*IRQ2	A09	LI/O*
	30	GND	A01	*IRQ1	A08	+3.3V
	31	RSVBUS	-12V	+5 STDBY	+12V	GND
	32	GND	+5V	+5V	+5V	VPC

	1	UD	+GSL2A0	+5V	-GSL2A0	UD
	2	GND	+GSL2A1	GND	-GSL2A1	UD
	3	UD	+GSL2A2	RESERVED	-GSL2A2	UD
	4	GND	+GSL2A3	A24	-GSL2A3	UD
	5	UD	+GSL2A4	A25	-GSL2A4	UD
	6	GND	+GSL2A5	A26	-GSL2A5	UD
	7	UD	+GSL2A6	A27	-GSL2A6	UD
	8	GND	+GSL2A7	A28	-GSL2A7	UD
	9	UD	+GSL2R0	A29	-GSL2R0	UD
P2/J2	10	GND	+GSL2R1	A30	-GSL2R1	UD
	11	UD	+GSL2R2	A31	-GSL2R2	UD
	12	GND	+GSL2R3	GND	-GSL2R3	UD
	13	UD	+GSL2R4	+5V	-GSL2R4	UD
	14	GND	+GSL2R5	D16	-GSL2R5	UD
	15	UD	+GSL2R6	D17	-GSL2R6	UD
	16	GND	+GSL2R7	D18	-GSL2R7	UD
	17	UD	+GSL1A0	D19	-GSL1A0	UD
	18	GND	+GSL1A1	D20	-GSL1A1	UD
	19	UD	+GSL1A2	D21	-GSL1A2	UD
	20	GND	+GSL1A3	D22	-GSL1A3	UD
	21	UD	+GSL1A4	D23	-GSL1A4	UD
	22	GND	+GSL1A5	GND	-GSL1A5	UD
	23	UD	+GSL1A6	D24	-GSL1A6	UD
	24	GND	+GSL1A7	D25	-GSL1A7	UD
	25	UD		D26		UD
	26	GND		D27		UD
	27	UD		D28		UD
	28	GND		D29		UD
	29	UD		D30		UD
	30	GND		D31		UD
	31	UD		GND		GND
	32	GND		+5V		VPC

	1	TSC_Addr0	MODADDR0	+RFClk		GND
	2	TSC_Addr1	MODADDR1	-RFClk		GND
	3	TSC_Addr2	MODADDR2	Dat0		GND
	4	TSC_Addr3	MODADDR3	Dat1		GND
	5	TSC_Addr4	/SLF_IN	GND		GND
	6	TSC_Addr5		GND		GND
	7	TSC_Addr6		Dat2		GND
	8	TSC_Addr7		Dat3		GND
	9	TSC_Addr8		Dat4		
P3/J3	10	TSC_Addr9		GND		
	11	TSC_Addr10		GND		
	12	TSC_Addr11		+Bsync		
	13	TSC_DS		-Bsync		
	14	TSC_RW		Dat5		
	15	TSC_BS		Dat6		
	16	TSC_Rst		Dat7		
	17	/STATSEL		GND		TSC_Dat0
	18	TSC_Init_Ack		GND		TSC_Dat1
	19	TSC_GB_Err		Dat8		TSC_Dat2
	20	TSC_IRQ		Dat9		TSC_Dat3
	21	TSC_StatAck		+RawBsync		TSC_Dat4
	22			-RawBsync		TSC_Dat5
	23			GND		TSC_Dat6
	24			GND		TSC_Dat7
	25	GND		Dat10		TSC_Dat8
	26	GND		Dat11		TSC_Dat9
	27	GND		Dat12		TSC_Dat10
	28	GND		Dat13		TSC_Dat11
	29	GND		Dat14		TSC_Dat12
	30	GND		Dat15		TSC_Dat13
	31	GND		EMU		TSC_Dat14
	32	GND				TSC_Dat15

SLF Pinout

		Z row	A row	B row	C row	D row
	1	MPR	D00	*BBSY	D08	VPC
	2	GND	D01	*BCLR	D09	GND
	3	MCLK	D02	*ACFAIL	D10	+V1
	4	GND	D03	*BGIN0	D11	+V2
	5	MSD	D04	*BGOUT0	D12	RSVU
	6	GND	D05	*BGIN1	D13	-V1
	7	MMD	D06	*BGOUT1	D14	-V2
	8	GND	D07	*BGIN2	D15	RSVU
	9	MCTL	GND	*BGOUT2	GND	GAP*
	10	GND	SYSCLK	*BGIN3	*SYSFAIL	GA0*
	11	RESP*	GND	*BGOUT3	*BERR	GA1*
	12	GND	*DS1	*BR0	*SYSRESET	+3.3V
	13	RSVBUS	*DS0	*BR1	*LWORD	GA2*
	14	GND	*WRITE	*BR2	AM5	+3.3V
	15	RSVBUS	GND	*BR3	A23	GA3*
P1/J1	16	GND	*DTACK	AM0	A22	+3.3V
	17	RSVBUS	GND	AM1	A21	GA4*
	18	GND	*AS	AM2	A20	+3.3V
	19	RSVBUS	GND	AM3	A19	RSVBUS
	20	GND	*IACK	GND	A18	+3.3V
	21	RSVBUS	*IACKIN	SERCLK	A17	RSVBUS
	22	GND	*IACKOUT	*SERDAT	A16	+3.3V
	23	RSVBUS	AM4	GND	A15	RSVBUS
	24	GND	A07	*IRQ7	A14	+3.3V
	25	RSVBUS	A06	*IRQ6	A13	RSVBUS
	26	GND	A05	*IRQ5	A12	+3.3V
	27	RSVBUS	A04	*IRQ4	A11	LI/I*
	28	GND	A03	*IRQ3	A10	+3.3V
	29	RSVBUS	A02	*IRQ2	A09	LI/O*
	30	GND	A01	*IRQ1	A08	+3.3V
	31	RSVBUS	-12V	+5 STDBY	+12V	GND
	32	GND	+5V	+5V	+5V	VPC

	1	UD	+GSL2A0	+5V	-GSL2A0	UD
	2	GND	+GSL2A1	GND	-GSL2A1	UD
	3	UD	+GSL2A2	RESERVED	-GSL2A2	UD
	4	GND	+GSL2A3	A24	-GSL2A3	UD
	5	UD	+GSL2A4	A25	-GSL2A4	UD
	6	GND	+GSL2A5	A26	-GSL2A5	UD
	7	UD	+GSL2A6	A27	-GSL2A6	UD
	8	GND	+GSL2A7	A28	-GSL2A7	UD
	9	UD	+GSL2R0	A29	-GSL2R0	UD
P2/J2	10	GND	+GSL2R1	A30	-GSL2R1	UD
	11	UD	+GSL2R2	A31	-GSL2R2	UD
	12	GND	+GSL2R3	GND	-GSL2R3	UD
	13	UD	+GSL2R4	+5V	-GSL2R4	UD
	14	GND	+GSL2R5	D16	-GSL2R5	UD
	15	UD	+GSL2R6	D17	-GSL2R6	UD
	16	GND	+GSL2R7	D18	-GSL2R7	UD
	17	UD	+GSL1A0	D19	-GSL1A0	UD
	18	GND	+GSL1A1	D20	-GSL1A1	UD
	19	UD	+GSL1A2	D21	-GSL1A2	UD
	20	GND	+GSL1A3	D22	-GSL1A3	UD
	21	UD	+GSL1A4	D23	-GSL1A4	UD
	22	GND	+GSL1A5	GND	-GSL1A5	UD
	23	UD	+GSL1A6	D24	-GSL1A6	UD
	24	GND	+GSL1A7	D25	-GSL1A7	UD
	25	UD		D26		UD
	26	GND		D27		UD
	27	UD		D28		UD
	28	GND		D29		UD
	29	UD		D30		UD
	30	GND		D31		UD
	31	UD		GND		GND
	32	GND		+5V		VPC

	1	TSC_Addr0	MODADDR0	+RFClk		GND
	2	TSC_Addr1	MODADDR1	-RFClk		GND
	3	TSC_Addr2	MODADDR2	Dat0		GND
	4	TSC_Addr3	MODADDR3	Dat1		GND
	5	TSC_Addr4	/SLF_IN	GND		GND
	6	TSC_Addr5		GND		GND
	7	TSC_Addr6		Dat2		GND
	8	TSC_Addr7		Dat3		GND
	9	TSC_Addr8		Dat4		
P3/J3	10	TSC_Addr9		GND		
	11	TSC_Addr10		GND		
	12	TSC_Addr11		+Bsync		
	13	TSC_DS		-Bsync		
	14	TSC_RW		Dat5		
	15	TSC_BS		Dat6		
	16	TSC_Rst		Dat7		
	17	/STATSEL		GND		TSC_Dat0
	18	TSC_Init_Ack		GND		TSC_Dat1
	19	TSC_GB_Err		Dat8		TSC_Dat2
	20	TSC_IRQ		Dat9		TSC_Dat3
	21	TSC_StatAck		+RawBsync		TSC_Dat4
	22			-RawBsync		TSC_Dat5
	23			GND		TSC_Dat6
	24			GND		TSC_Dat7
	25	GND		Dat10		TSC_Dat8
	26	GND		Dat11		TSC_Dat9
	27	GND		Dat12		TSC_Dat10
	28	GND		Dat13		TSC_Dat11
	29	GND		Dat14		TSC_Dat12
	30	GND		Dat15		TSC_Dat13
	31	GND		EMU		TSC_Dat14
	32	GND				TSC_Dat15

THC Pinout

		Z row	A row	B row	C row	D row
	1	MPR	D00	*BBSY	D08	VPC
	2	GND	D01	*BCLR	D09	GND
	3	MCLK	D02	*ACFAIL	D10	+V1
	4	GND	D03	*BGIN0	D11	+V2
	5	MSD	D04	*BGOUT0	D12	RSVU
	6	GND	D05	*BGIN1	D13	-V1
	7	MMD	D06	*BGOUT1	D14	-V2
	8	GND	D07	*BGIN2	D15	RSVU
	9	MCTL	GND	*BGOUT2	GND	GAP*
	10	GND	SYSCLK	*BGIN3	*SYSFAIL	GA0*
	11	RESP*	GND	*BGOUT3	*BERR	GA1*
	12	GND	*DS1	*BR0	*SYSRESET	+3.3V
	13	RSVBUS	*DS0	*BR1	*LWORD	GA2*
	14	GND	*WRITE	*BR2	AM5	+3.3V
	15	RSVBUS	GND	*BR3	A23	GA3*
P1/J1	16	GND	*DTACK	AM0	A22	+3.3V
	17	RSVBUS	GND	AM1	A21	GA4*
	18	GND	*AS	AM2	A20	+3.3V
	19	RSVBUS	GND	AM3	A19	RSVBUS
	20	GND	*IACK	GND	A18	+3.3V
	21	RSVBUS	*IACKIN	SERCLK	A17	RSVBUS
	22	GND	*IACKOUT	*SERDAT	A16	+3.3V
	23	RSVBUS	AM4	GND	A15	RSVBUS
	24	GND	A07	*IRQ7	A14	+3.3V
	25	RSVBUS	A06	*IRQ6	A13	RSVBUS
	26	GND	A05	*IRQ5	A12	+3.3V
	27	RSVBUS	A04	*IRQ4	A11	LI/I*
	28	GND	A03	*IRQ3	A10	+3.3V
	29	RSVBUS	A02	*IRQ2	A09	LI/O*
	30	GND	A01	*IRQ1	A08	+3.3V
	31	RSVBUS	-12V	+5 STDBY	+12V	GND
	32	GND	+5V	+5V	+5V	VPC

	1	UD		+5V		UD
	2	GND		GND		UD
	3	UD		RESERVED		UD
	4	GND		A24		UD
	5	UD		A25		UD
	6	GND		A26		UD
	7	UD		A27		UD
	8	GND		A28		UD
	9	UD		A29		UD
P2/J2	10	GND		A30		UD
	11	UD		A31		UD
	12	GND		GND		UD
	13	UD		+5V		UD
	14	GND		D16		UD
	15	UD		D17		UD
	16	GND		D18		UD
	17	UD		D19		UD
	18	GND		D20		UD
	19	UD		D21		UD
	20	GND		D22		UD
	21	UD		D23		UD
	22	GND		GND		UD
	23	UD		D24		UD
	24	GND		D25		UD
	25	UD		D26		UD
	26	GND		D27		UD
	27	UD		D28		UD
	28	GND		D29		UD
	29	UD		D30		UD
	30	GND		D31		UD
	31	UD		GND		GND
	32	GND		+5V		VPC

		A row	B row	C row	D row	E row	F row
	1	+RFCLK0	-RFCLK0	TSC_ADDR0	-RFCLK15	+RFCLK15	GND
	2	+RFCLK1	-RFCLK1	TSC_ADDR1	-RFCLK14	+RFCLK14	GND
	3	+RFCLK2	-RFCLK2	TSC_ADDR2	-RFCLK13	+RFCLK13	GND
	4	+RFCLK3	-RFCLK3	TSC_ADDR3	-RFCLK12	+RFCLK12	GND
	5	+RFCLK4	-RFCLK4	TSC_ADDR4	-RFCLK11	+RFCLK11	GND
	6	+RFCLK5	-RFCLK5	TSC_ADDR5	-RFCLK10	+RFCLK10	GND
	7	+RFCLK6	-RFCLK6	TSC_ADDR6	-RFCLK9	+RFCLK9	GND
	8	+RFCLK7	-RFCLK7	TSC_ADDR7	-RFCLK8	+RFCLK8	GND
	9	GND	GND	TSC_ADDR8	GND	GND	GND
P3/J3	10	+BSYNC0	-BSYNC0	TSC_ADDR9	-BSYNC15	+BSYNC15	GND
	11	+BSYNC1	-BSYNC1	TSC_ADDR10	-BSYNC14	+BSYNC14	GND
	12	+BSYNC2	-BSYNC2	TSC_ADDR11	-BSYNC13	+BSYNC13	GND
	13	+BSYNC3	-BSYNC3	TSC_DS	-BSYNC12	+BSYNC12	GND
	14	+BSYNC4	-BSYNC4	TSC_RW	-BSYNC11	+BSYNC11	GND
	15	+BSYNC5	-BSYNC5	TSC_BS	-BSYNC10	+BSYNC10	GND
	16	+BSYNC6	-BSYNC6	TSC_RST	-BSYNC9	+BSYNC9	GND
	17	+BSYNC7	-BSYNC7	/STATSEL	-BSYNC8	+BSYNC8	GND
	18	GND	GND	TSC_DAT0	GND	GND	GND
	19	+RAWBSYNC0	-RAWBSYNC0	TSC_DAT1	-RAWBSYNC15	+RAWBSYNC15	GND
	20	+RAWBSYNC1	-RAWBSYNC1	TSC_DAT2	-RAWBSYNC14	+RAWBSYNC14	GND
	21	+RAWBSYNC2	-RAWBSYNC2	TSC_DAT3	-RAWBSYNC13	+RAWBSYNC13	GND
	22	+RAWBSYNC3	-RAWBSYNC3	TSC_DAT4	-RAWBSYNC12	+RAWBSYNC12	GND
	23	+RAWBSYNC4	-RAWBSYNC4	GND	-RAWBSYNC11	+RAWBSYNC11	GND
	24	+RAWBSYNC5	-RAWBSYNC5	GND	-RAWBSYNC10	+RAWBSYNC10	GND
	25	+RAWBSYNC6	-RAWBSYNC6	GND	-RAWBSYNC9	+RAWBSYNC9	GND
	26	+RAWBSYNC7	-RAWBSYNC7	GND	-RAWBSYNC8	+RAWBSYNC8	GND
	27	GND	VTT	GND	VTT	GND	GND
	28	LSLFDAT0	GND	GND	GND	RSLFDAT0	GND
	29	LSLFDAT1	VTT	GND	VTT	RSLFDAT1	GND
	30	LSLFDAT2	GND	TSC_INIT_ACK	GND	RSLFDAT2	GND
	31	LSLFDAT3	VTT	TSC_GB_ERR	VTT	RSLFDAT3	GND
	32	LSLFDAT4	GND	TSC_IRQ	GND	RSLFDAT4	GND
	33	LSLFDAT5	VTT	STATACK	VTT	RSLFDAT5	GND
	34	LSLFDAT6	GND	TSC_DAT5	GND	RSLFDAT6	GND
	35	LSLFDAT7	VTT	TSC_DAT6	VTT	RSLFDAT7	GND
	36	LSLFDAT8	GND	TSC_DAT7	GND	RSLFDAT8	GND
	37	LSLFDAT9	VTT	TSC_DAT8	VTT	RSLFDAT9	GND
	38	LSLFDAT10	GND	TSC_DAT9	GND	RSLFDAT10	GND
	39	LSLFDAT11	VTT	TSC_DAT10	VTT	RSLFDAT11	GND
	40	LSLFDAT12	GND	TSC_DAT11	GND	RSLFDAT12	GND
	41	LSLFDAT13	VTT	TSC_DAT12	VTT	RSLFDAT13	GND
	42	LSLFDAT14	GND	TSC_DAT13	GND	RSLFDAT14	GND
	43	LSLFDAT15	VTT	TSC_DAT14	VTT	RSLFDAT15	GND
	44	LEMU	GND	TSC_DAT15	GND	REMU	GND

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1/15/99