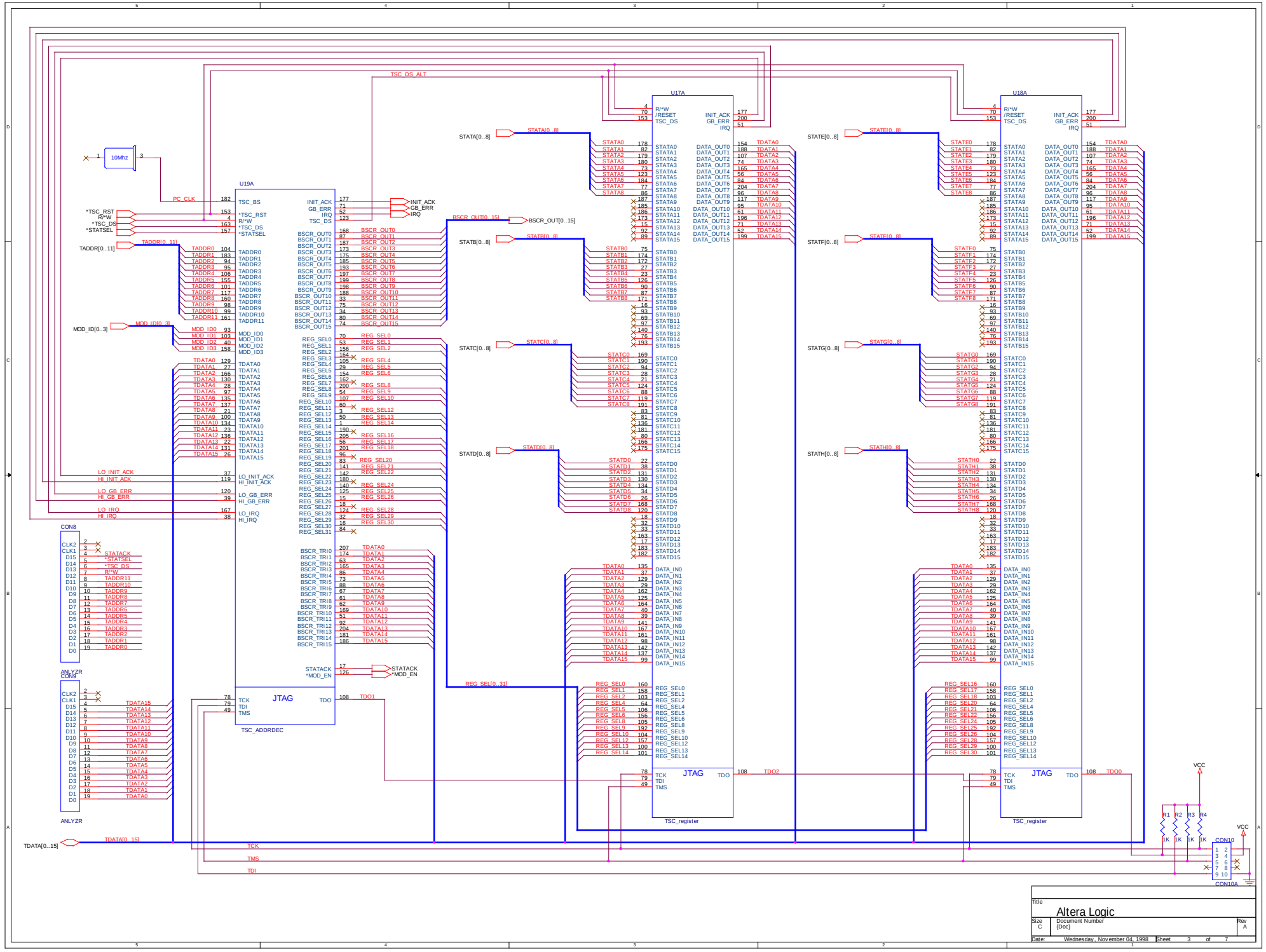
U17A
U18A
U19A
TSC_register
TSC_ADDRDEC
JTAG
10Mhz
CON8
CON9
ANLYZR
CON10
TSC_DS_ALT
PC_CLK
TADDR[0..11]
MOD_ID[0..3]
TDATA[0..15]
STATA[0..8]
STATB[0..8]
STATC[0..8]
STATD[0..8]
STATE[0..8]
STATF[0..8]
STATG[0..8]
STATH[0..8]
BSCR_OUT[0..15]
REG_SEL[0..31]
TCK
TMS
TDI
VCC
R1 1K
R2 1K
R3 1K
R4 1K
Title
Altera Logic
Size C
Document Number {Doc}
Rev A
Date: Wednesday, November 04, 1998
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