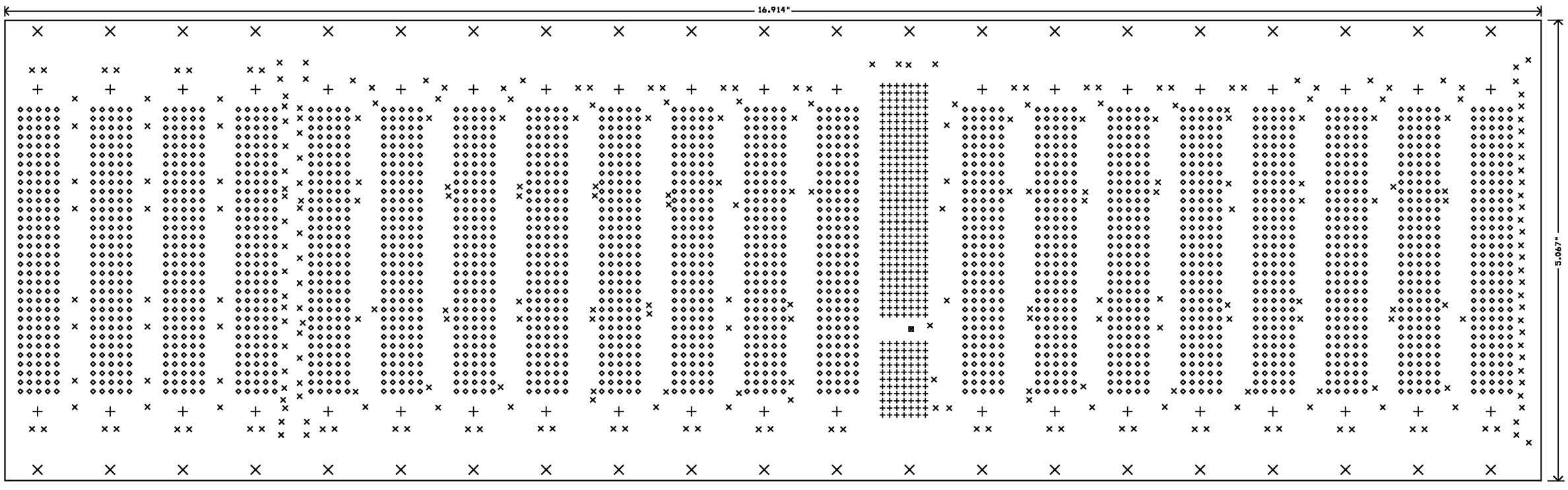
Fermilab D0 J3 Backplane Drill / Fab Drawing



Controlled Impedance Requirements:

50 Ohms between layers 1 & 2
100 Ohms between layers 2 & 3
50 Ohms between layers 3 & 4
50 Ohms between layers 6 & 7
50 Ohms between layers 7 & 8

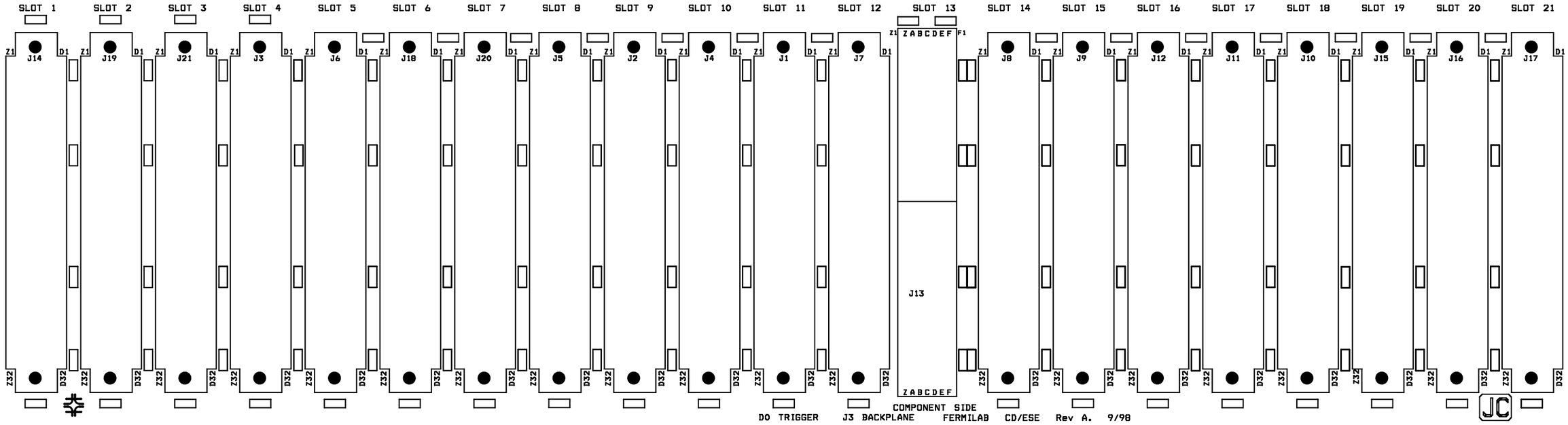
LAYER STACKUP: (0.195) Total Board Thickness

1) Top Trace: (Copper Pour Ground)
2) Inner Trace 1: Differential ECL (+)
3) Inner Trace 2: Differential ECL (-)
4) Ground Plane
5) VTT Power Layer (Copper Pour)
6) Ground Plane
7) Inner Trace 3: ECL Traces
8) Ground Plane
9) Inner Trace 4: TTL Traces
10) Bottom Trace: (Copper Pour Ground)

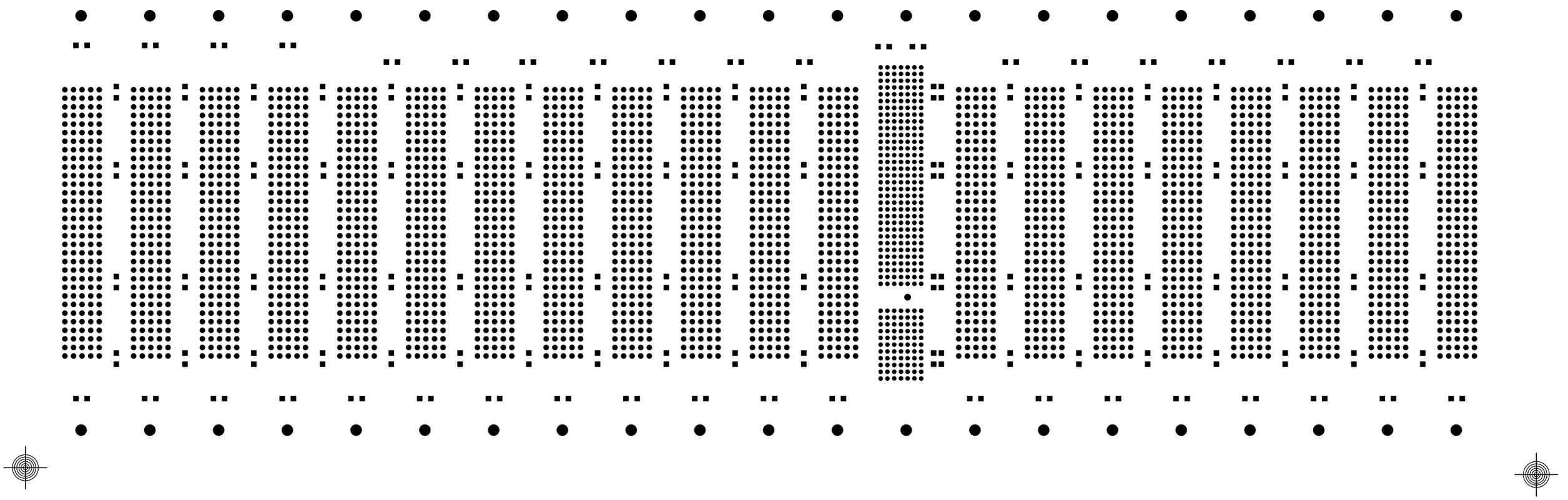
HOLE LEGEND

SYM	DIAM	TOL	QTY	NOTE
×	0.020		299	
+	0.024		308	
◇	0.040		3200	
◙	0.080		1	NON-PLATED
┼	0.106		40	
X	0.110		42	
TOTAL			3890	

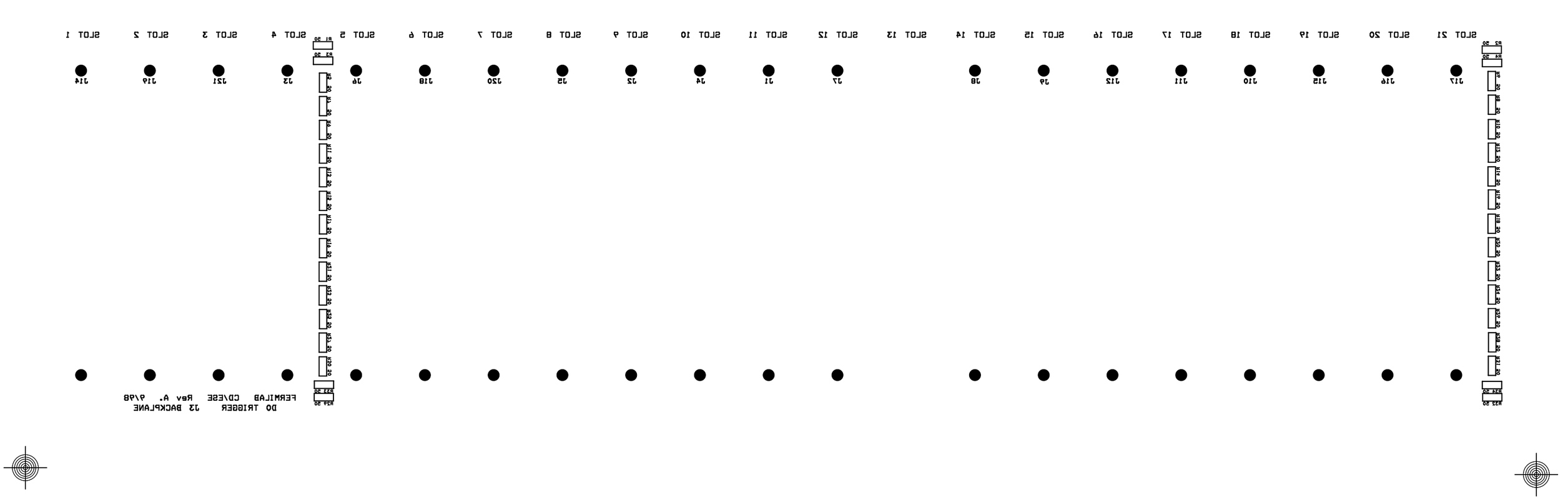
Fermilab D0 J3 Backplane Top Silkscreen



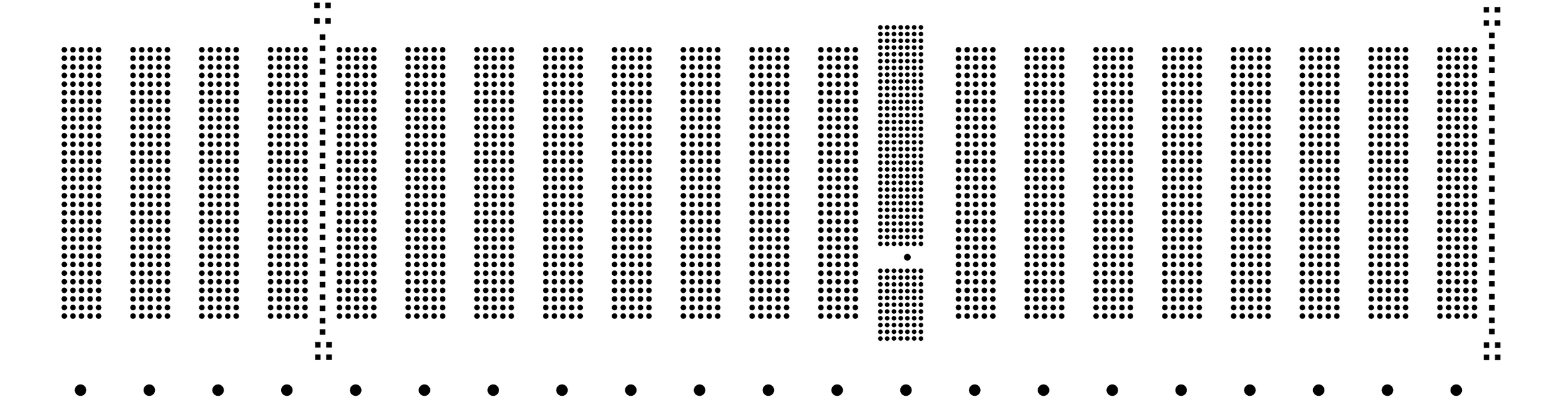
Fermilab D0 J3 Backplane Top Soldermask



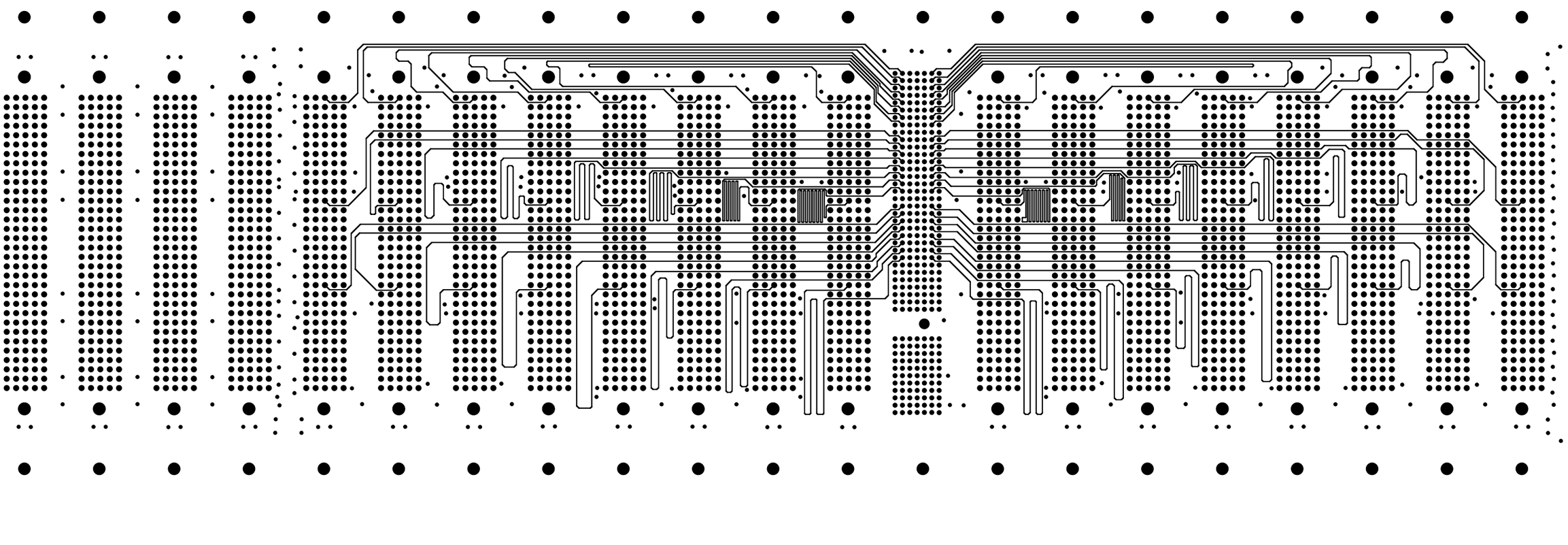
Fermilab D0 J3 Backplane Bottom Silkscreen



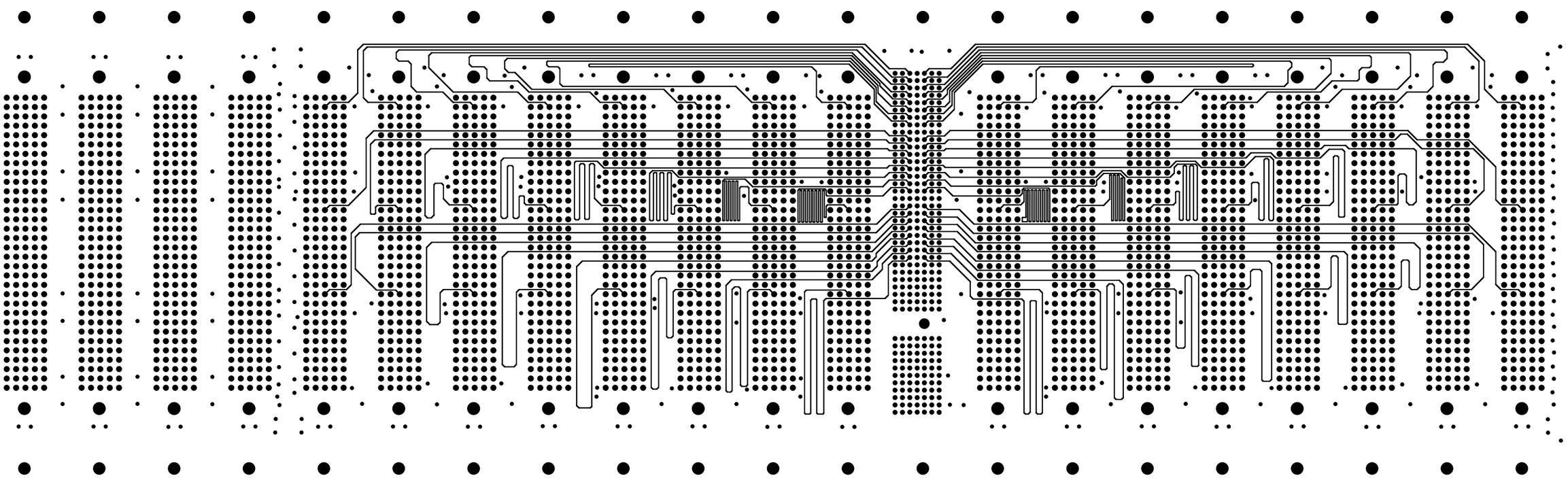
Fermilab D0 J3 Backplane **Bottom Soldermask**



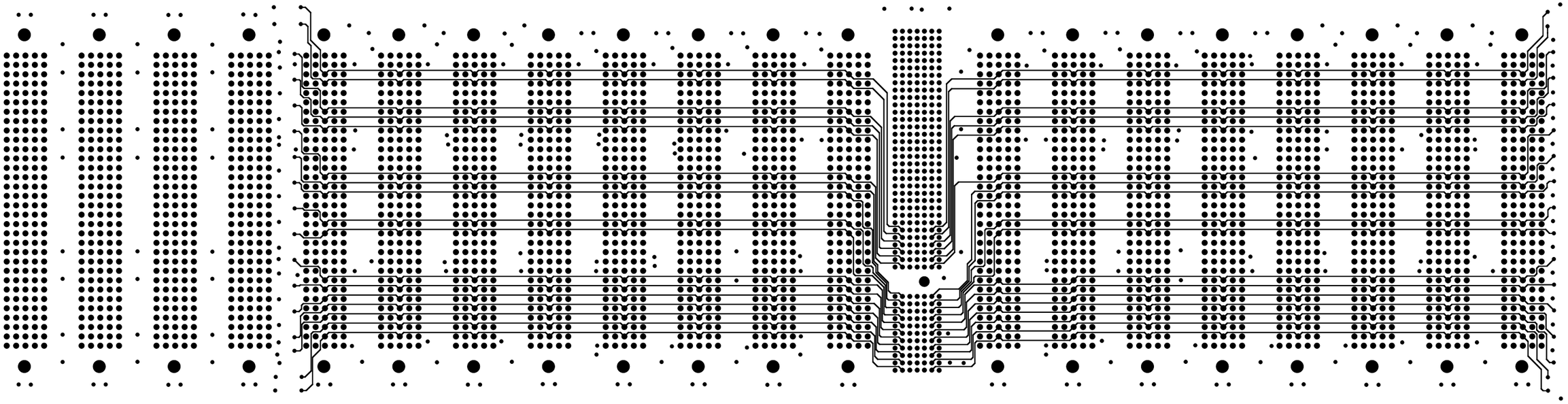
Fermilab D0 J3 Backplane Inner Trace 1 (Differential ECL Traces / (+))



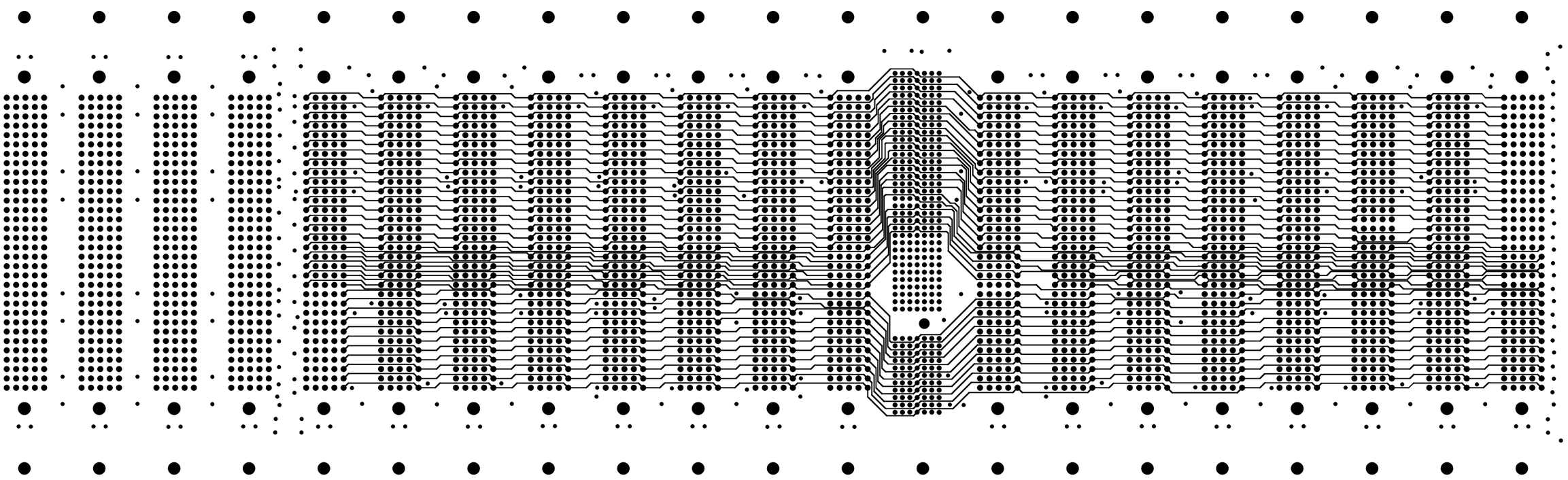
Fermilab D0 J3 Backplane Inner Trace 2 (Differential ECL Traces / (-))



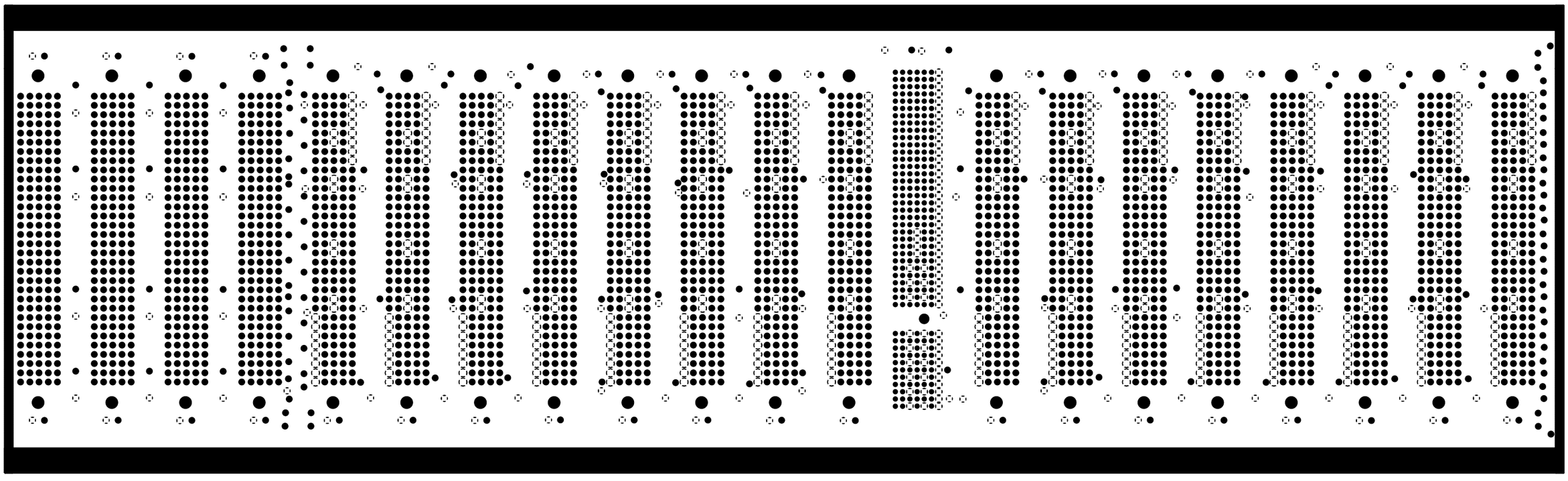
Fermilab D0 J3 Backplane Inner Trace 3 (ECL Signals)



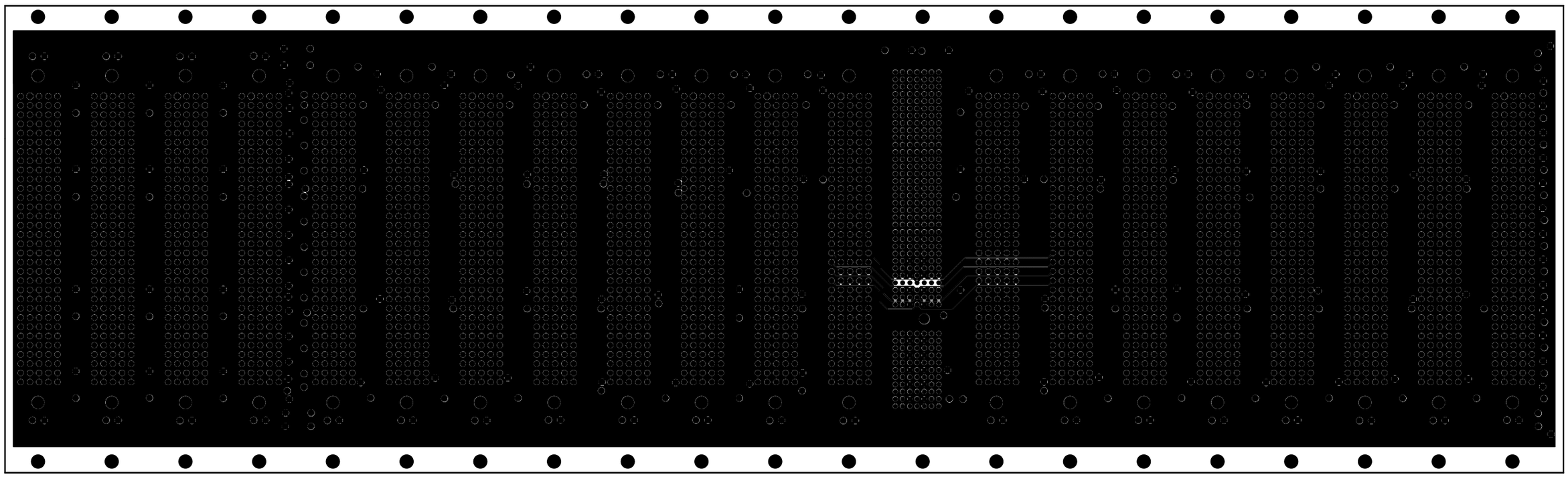
Fermilab D0 J3 Backplane Inner Trace 4 (TTL Traces)



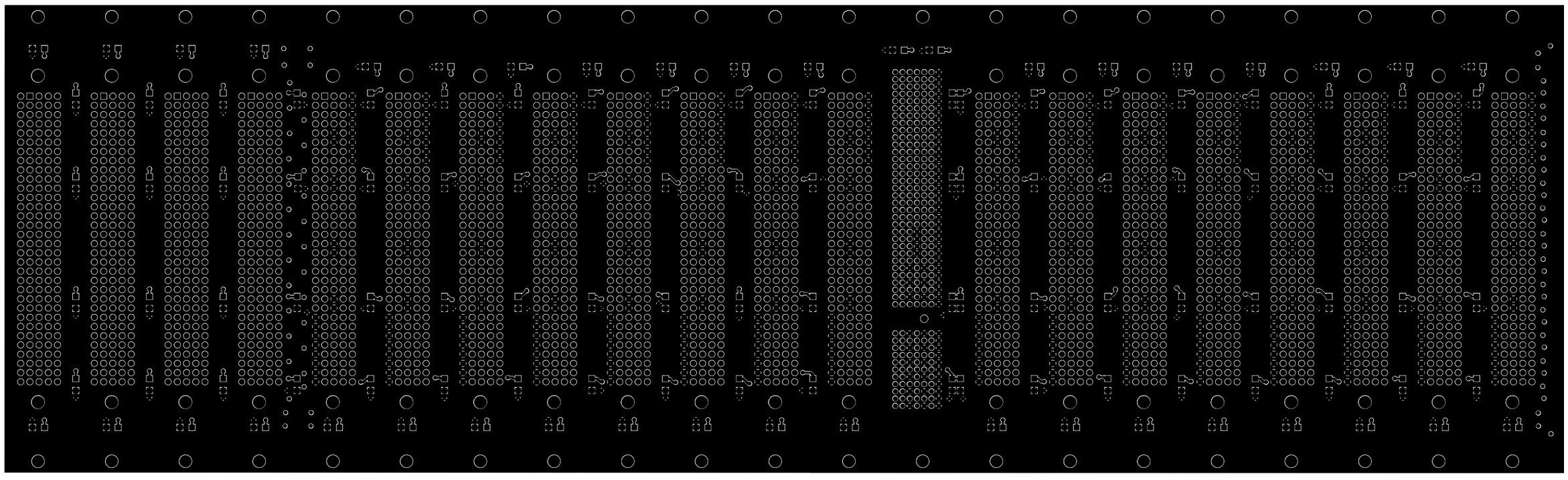
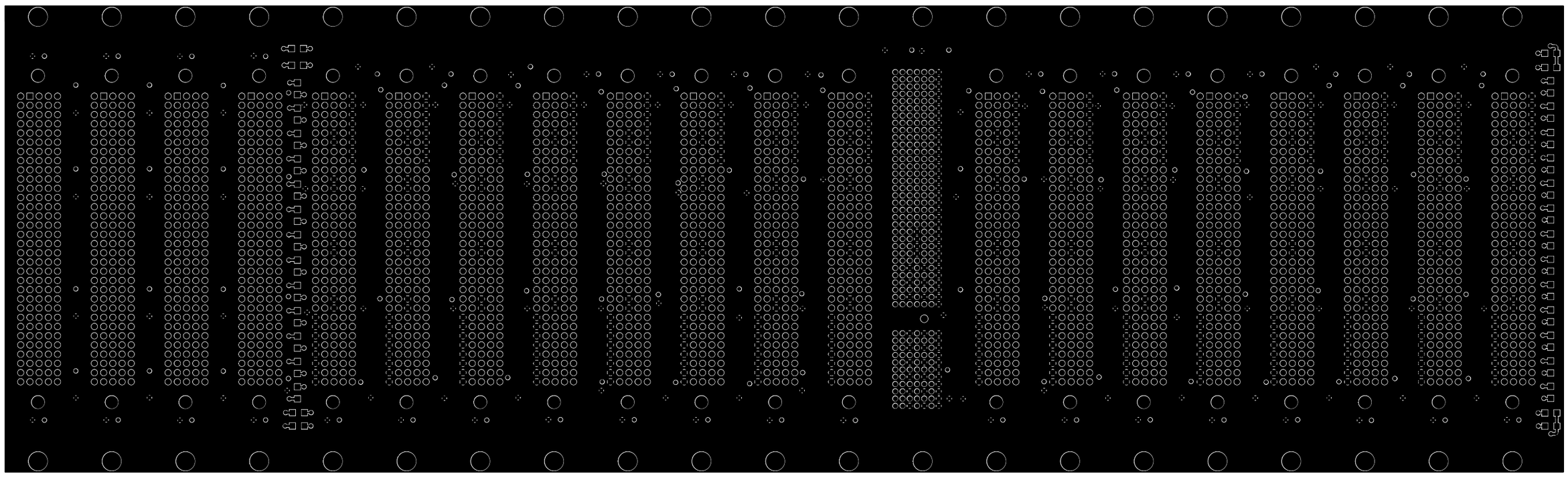
Fermilab D0 J3 Backplane Ground Plane('s)



Fermilab D0 J3 Backplane VTT Power Layer



Fermilab D0 J3 Backplane Top Trace Layer (Copper Pour Ground)



Fermilab D0 J3 Backplane Bottom Trace Layer (Copper Pour Ground)