

# The ASDQ ASIC

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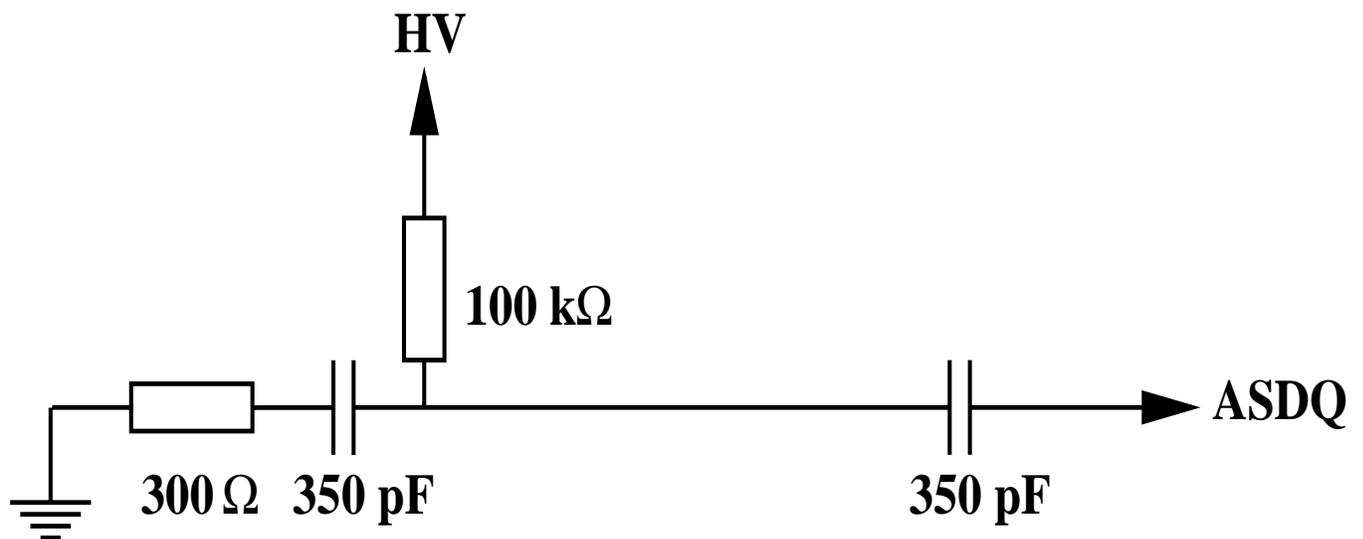
- ◇ *Introduction*
- ◇ *Signal*
- ◇ *Circuit and Design*
- ◇ *Fabrication*
- ◇ *Measurements*
- ◇ *Conclusions*

## Highlights

- ★ Performed measurements on prototype ASDQ's
- ★ Good Agreement with SPICE expectations
- ★ All functionalities work
- ★ High Yield

## COT Cell

- ◇ Tevatron Run II: 132 ns bunch crossing
- ◇ Luminosity(Run II)  $\approx 8 \times$  Luminosity(Run I)
- ◇ COT inner layers will operate at  $\lesssim 5$  MHz
- ◇ Drift distance: COT (0.9 cm) CTC (3.6 cm)
- ◇ Max drift time: COT (100 ns) CTC (706 ns)
- ◇ 50:35:15 Ar-Ethane-CF<sub>4</sub> ( $90 \mu\text{m}/\text{ns} = 200\text{K mph}$ )



- ◇ Cell dimen:  $1 \text{ cm}^2 \times 3.1 \text{ m}$
- ◇ 30,240 wires (16,128 axial; 14,112 stereo)

The ASDQ ASIC provides eight channels of complete analog signal processing between the COT chamber and the TDC's.

# ASDQ Requirements

High Run II Luminosities require:

**Good Position Resolution (200  $\mu\text{m}$ )**  
**Good Double Pulse Resolution (20 ns)**  
**Good charge measurement (resolution and range)**

- ◇ Short peaking time (8 ns)
- ◇ Low intrinsic noise
- ◇ Sub ns timing accuracy
- ◇ Low operating threshold circuit (2-3 fC)
  
- ◇ Reduce RF pickup and improve S/N by mounting on COT
- ◇ Low power to minimize heat dissipation within the COT superconducting volume

# Signal Generation

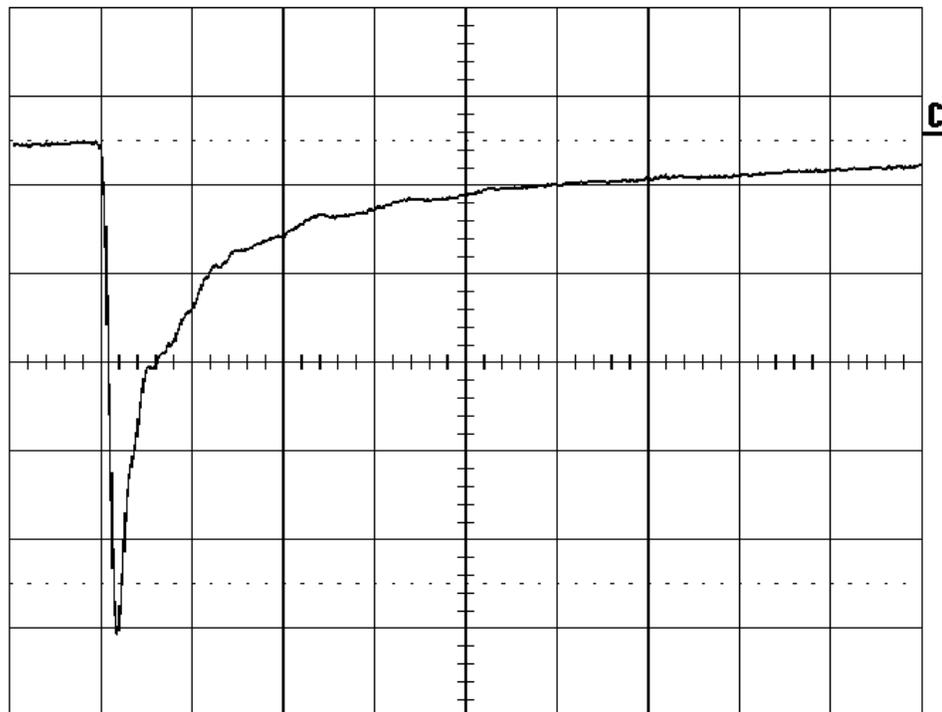
- ◇ Charged particle leaves ionization trail
- ◇  $\approx 3$  clusters/mm (9 electrons/mm)
- ◇ Electrons cause controlled avalanche ( $G \sim 2 \times 10^4$ )
- ◇ Electrons have a small contribution to the signal
- ◇ *Ion Tail* extends over few  $\mu s$

$$I(t) = \bar{Q}\delta(0) + \frac{k}{t+t_0}$$

$$\bar{Q} = 0.1 * \int_0^8 I(t)dt$$

26-Mar-98  
22:05:32

Ⓒ: Average(2)  
10 ns  
0.70 mV  
455 swps



10 ns RIS

← 92 ns

1 disabled  
2 2.00 mV 50Ω  
3 50 mV 50Ω  
4 disabled



Ext AC -70 mV 50Ω

10 GS/s

□ NORMAL

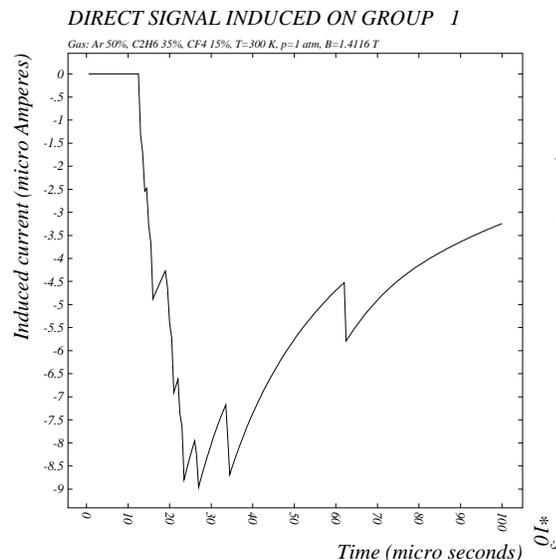
## ASDQ Blocks

- ★ **Preamp**: Amplify the signal without adding noise. No appreciable signal shaping.
- ★ **Ion Tail Cancellation**: Tail extends for few  $\mu\text{s}$  inhibiting high rate operation. Pole-zero shortening filter removes the ion tail.
- ★ **Baseline Restoration**: Capacitively de-couples the Preamp and the Shaper from the Comparator with a short time constant (Diode-shunt clipper).
- ★ **dE/dx**: Charge measurement useful for particle identification (low  $p_T$  electrons,  $p/\pi/K$  separation for limited momentum range). Encode  $Q$  into Discriminator output width by switching to a long charge integration time once an above threshold signal is detected.

Analog **S**haping **D**iscriminator **Q**-measurement

## Signal Properties

◇ Track produces many point ionizations staggered in time. Sum to get chamber signal. (GARFIELD simulation)



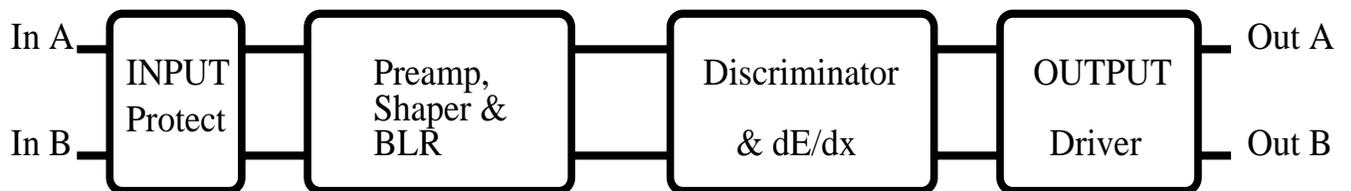
- ◇ 18% of the total charge is available in first 8 ns
- ◇ 37.5% of charge deposited (in 8 ns) into the Preamp
- ◇ Losses due to charge division in sense wire (50%) and stray capacitance (12.5%) are dominant

MIP: 20 fC into the Preamp

In this talk, refer to charge in the Preamp used in signal processing (7% of charge on wire)

# ASDQ Channel

Eight identical channels

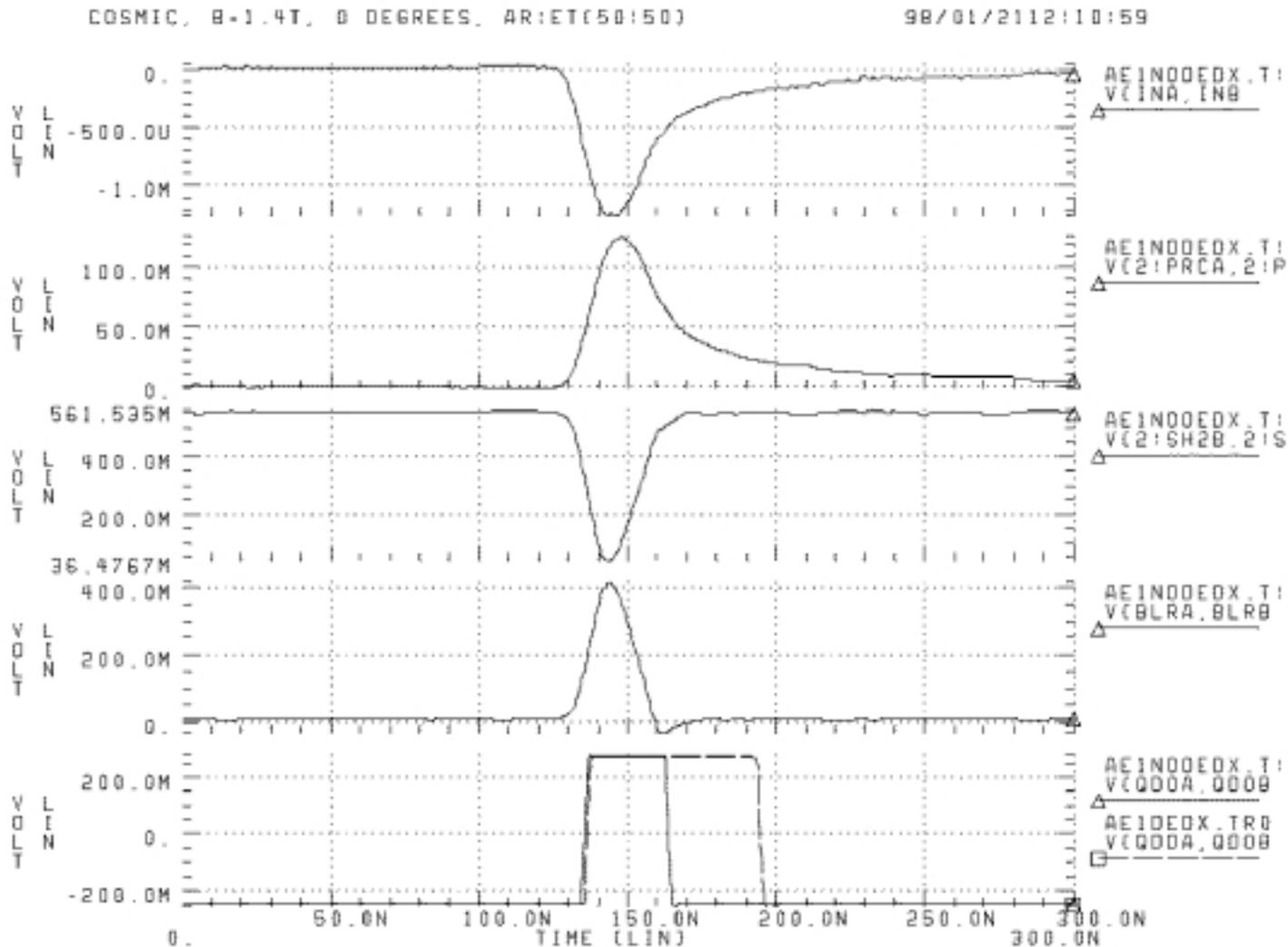


- ★ Input Protection (Pos and Neg HV spikes)
- ★ Preamplifier
- ★ Tail Cancellation (Shaper)
- ★ Selectable Attenuator
- ★ Baseline Restorer
- ★ Output Monitor
- ★  $dE/dx$  integration and Width encoding Disc
- ★ Output Driver

# Signal Evolution

Radial Cosmic Track in Prototype Chamber (B=1.4T)  
Corrected for Preamp Integration and Gain, and fed into SPICE  
model of ASDQ

$Q \sim 80fC$



## Input Protection

Sense wire capacitor has 1.5mJ stored energy  
Protection against breakdown necessary

Both On-Chip and Off-Chip Protection

**Off-Chip:** Provision for series  $R$  and diode on ASDQ daughterboard.

**On-Chip:** Series  $R$  into large area diodes.

On-Chip	
Negative Spike	$350 \mu m \times 400 \mu m$ epi-resistance and epi-P+ resistor diode
Fast Neg. Spike	$32 \times$ transistor, diode-wired
Positive Spike	$100 \mu m \times 250 \mu m$ P+ epi-wired

## Preamplifier

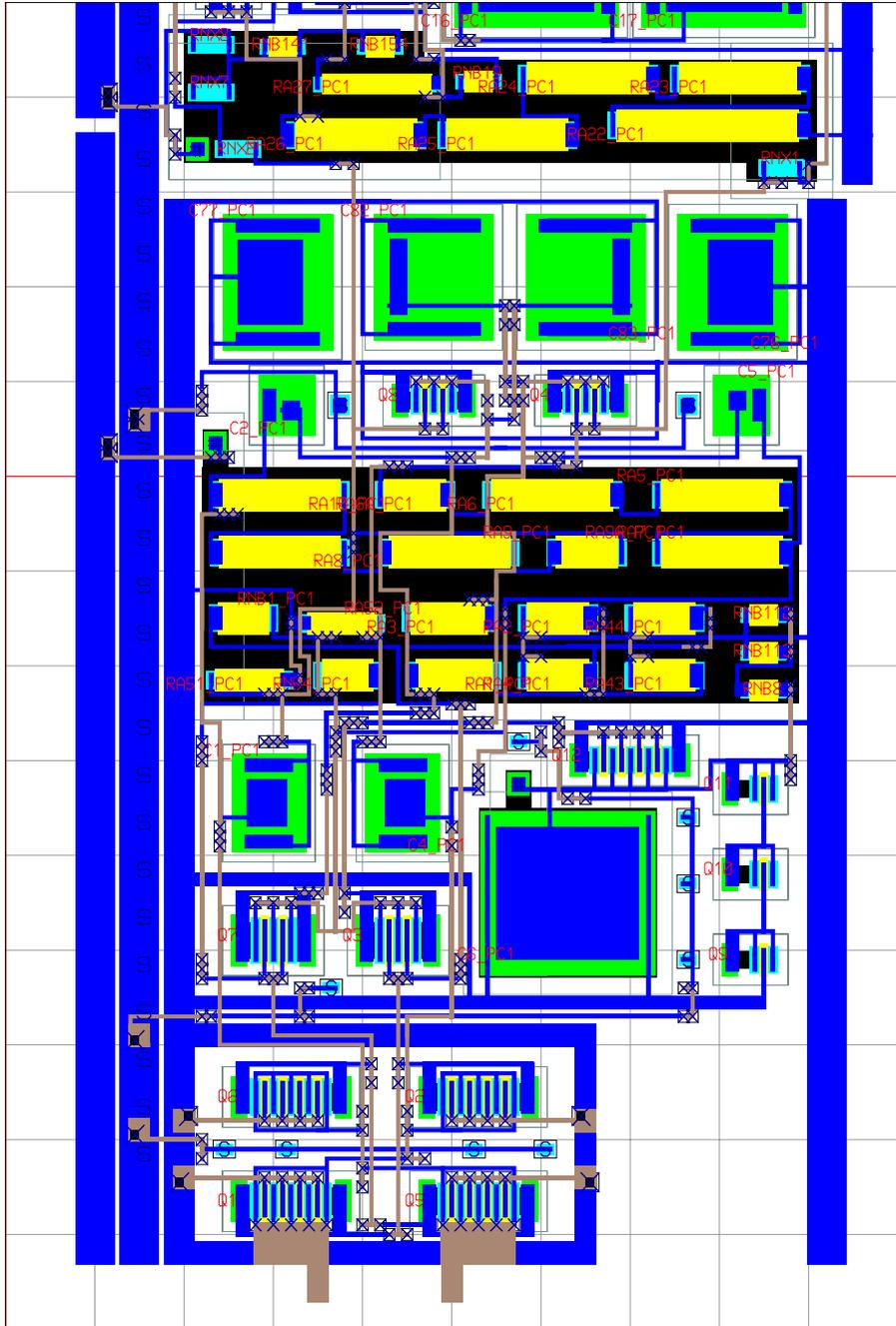
Two identical fully functional preamplifiers in each channel (pseudo-differential)

Three transistor, cascoded common-emitter circuit

- ◇ Provide DC balanced input to the Shaper
- ◇ Good common-mode noise rejection
  
- ◇ Preamps are interweaved in the layout to reduce imbalanced pickup
  
- ◇ The transistor pairs at the input are laid out in *cross quad* formation for good geometric and thermal matching

Preamp Specs	
Gain	1.5 mV/fC
Range	linear to 1.5 pC
Shaping	1.5 ns rise

# Preamp Layout



Cell: prshreca Modified: Tue Nov 11 13:53:57 1997 Plotted: Thu Mar 12 15:46:55 1998 Scale: 460

## Shaper

- ◇ Fully differential two stage Multipole shaping
- ◇ Ion Tail Cancellation
- ◇ Signal limiting into the BLR

Selectable  $\times 2$  Attenuator: Reduces the amplitude of the pulse into second stage of the Shaper

Shaper Specs	
Gain	25 mV/fC
Range (Ion Tail)	$\leq 600$ fC
Range (Preamp Tail)	$\leq 120$ fC
Shaping	5 ns 0-Peak at BLR input
Undershoot	$\leq 2\%$

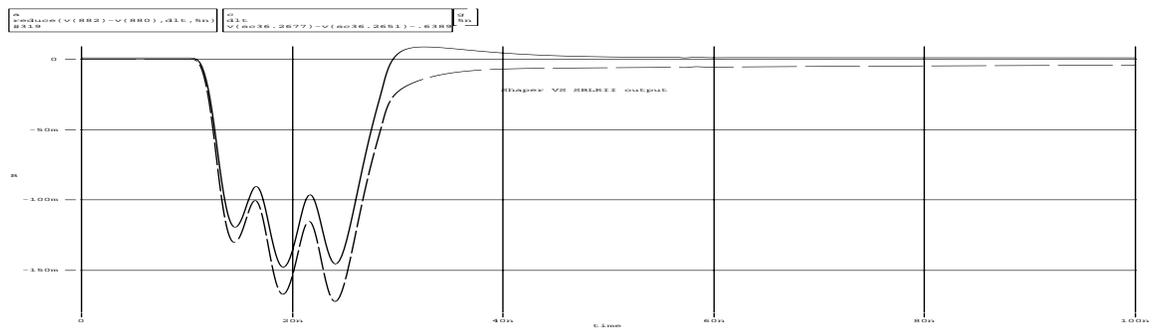
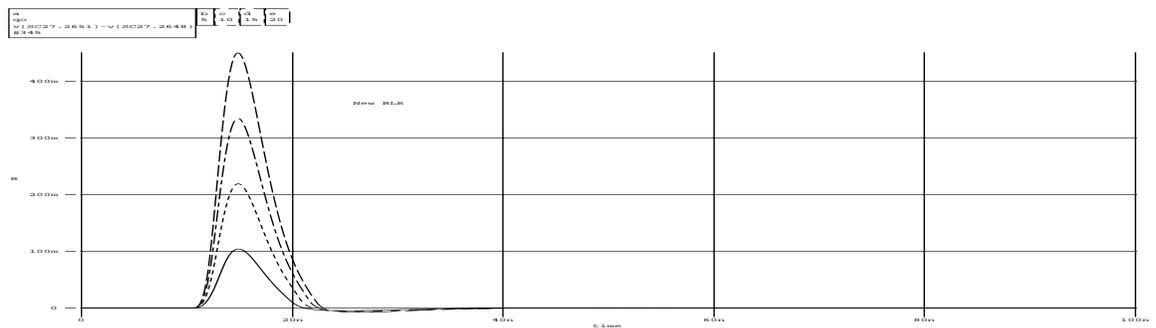
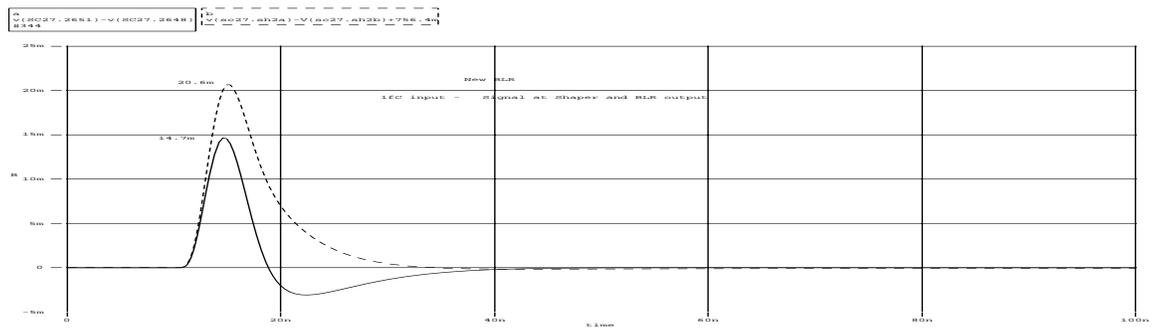
## BaseLine Restoration

- ◇ Fully differential
- ◇ AC coupling removes DC process variations before the discriminator
- ◇ Allows high rate performance
- ◇ Provides insensitivity to Tail cancellation imperfections
- ◇ For large  $Q$  depositions ( $> 30$  MIPs):  
Allows earlier re-triggering and eliminates multiple triggers when tail cancellation is saturated
- ◇ Designed to minimize effect on  $dE/dx$
- ◇ Analog monitor point (Ch 8) provides a copy of the BLR output

<b>BLR</b>	
Gain	$\geq 66\%$ (3fC), 90% ( $> 30$ fC)
Range	120 fC
Shaping	No significant additional shaping for large pulses
Undershoot	$\leq 3$ fC (Signals $\leq 100$ fC)

# Shaper and BLR

SPICE simulation of Shaper and BLR behavior



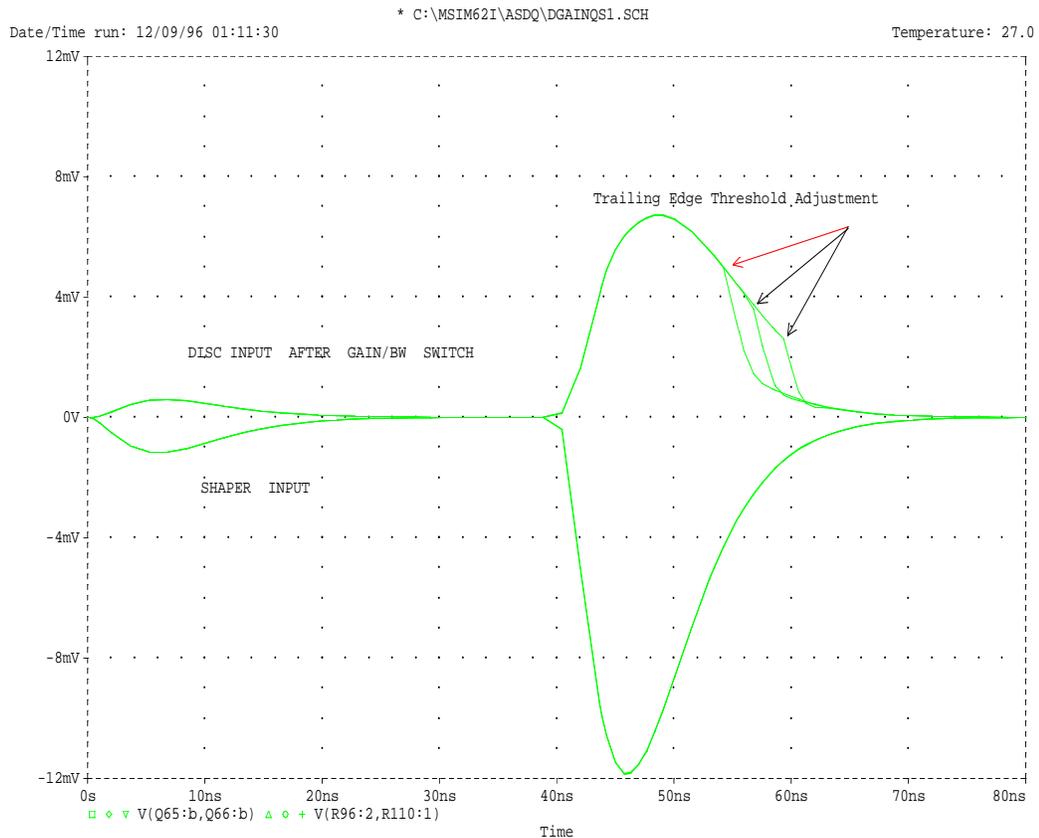
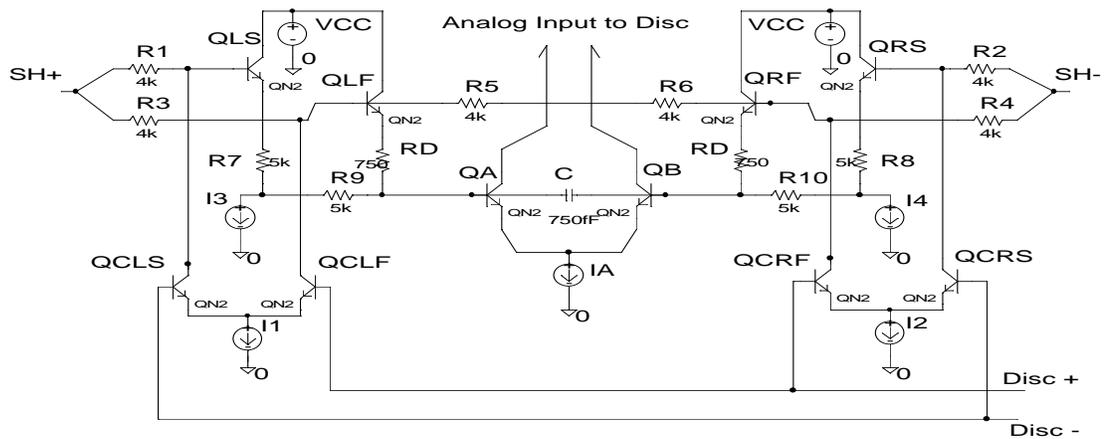
## $dE/dx$ and Discriminator

- ◇ Programmable leading edge discriminator threshold allows triggering on  $Q \geq 2$  fC
- ◇ Selectable  $dE/dx$  switch based on CTC switched gain discrete circuit. When enabled switches to longer integration times for above threshold signals.
- ◇ Fast shaping for leading edge detection: 8 ns
- ◇ Switch to 28 ns for charge integration.
- ◇ Once signal falls below trailing edge threshold, switch back to short integration time.

Programmable trailing edge threshold and  $dE/dx$  capacitor drain current allow tuning of the discriminator output pulse width for given  $Q$ .

# $dE/dx$ and Discriminator

$dE/dx$  schematic and trailing edge threshold



## $dE/dx$ and Discriminator

<b>Discriminator Specs</b>	
Power dissipation	7mW
Time slewing	<1 ns/decade of overdrive
Minimum width	5 ns
Internal offset	$\leq 1\text{mV}$ (0.05fC)
Threshold range	10fC
Threshold uniformity	$\Delta(\text{thresh})/\text{thresh} < 10\%$ (chip-to-chip)
Output	Bi-level

<b>dE/dx Specs</b>	
Shaping	Peaking time 8 ns
Pedestal	5 ns
Encoding	$\Delta t \propto \log(Q)$
Saturation	120 fC
Mean pulse width	10-15ns beyond width of shaped pulse (40-50ns)

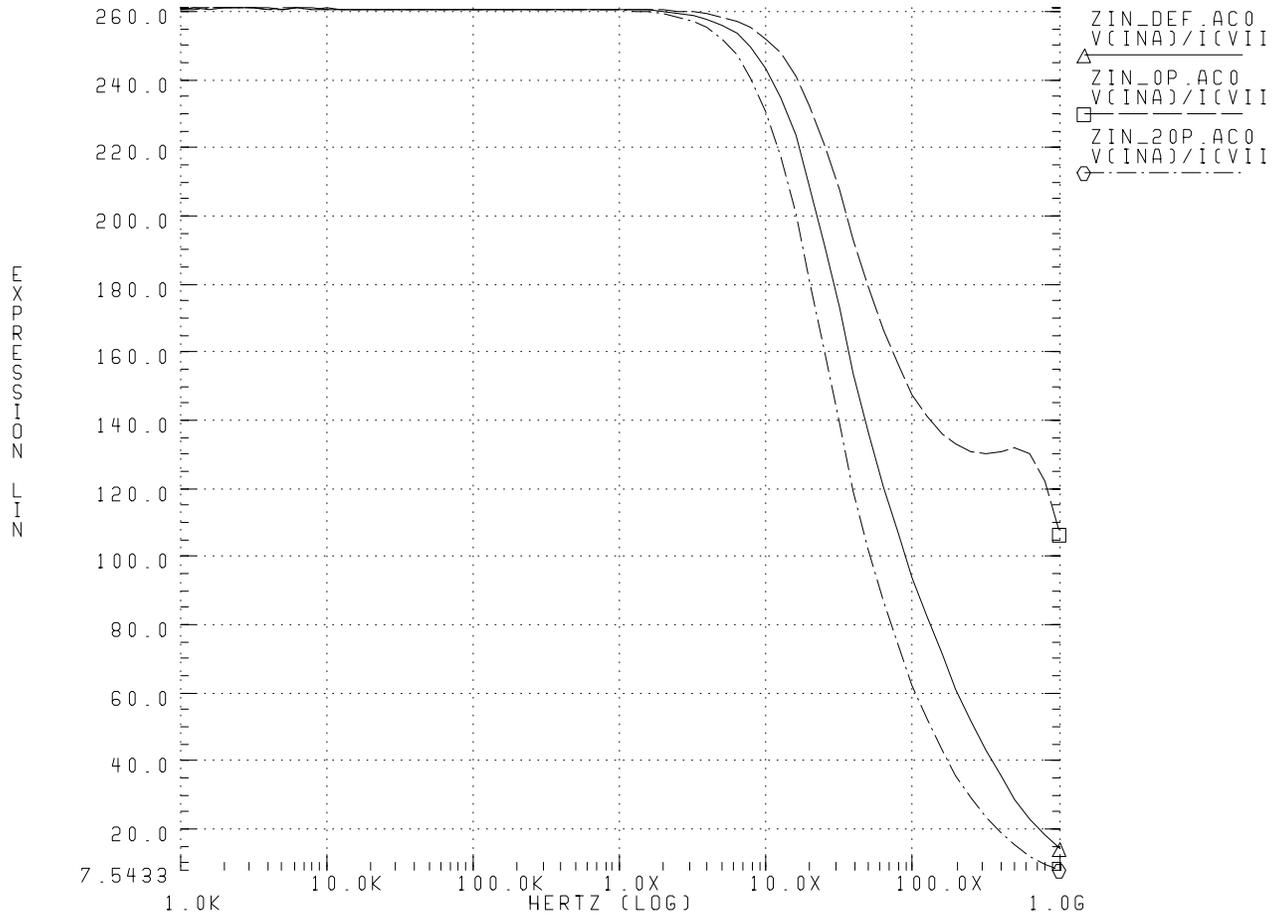
## Calibration Circuit

- ◇ Allows determination of relative  $t_0$  and  $Q$  vs. width relation for different channels.
- ◇ Provides a programmable pulse up to  $\sim 30$  fC.
- ◇ Separate control of even and odd channels

Calibration	
Test Pulse	Transition board Input
Minimum input width	5ns
Input amplitude	Differential ECL
Test Pulse	ASDQ input
Minimum input width	5 ns
Minimum input amplitude	250 mV differential
Test Pulse Reference	0V (max out), -3V (zero out)
Output Range	$\lesssim 30$ fC

# ASDQ Input Impedance

ASDQ INPUT IMPEDANCE, C\_STRAY=20PF, 10PF, 0PF 98/02/26



## Fabrication and Layout

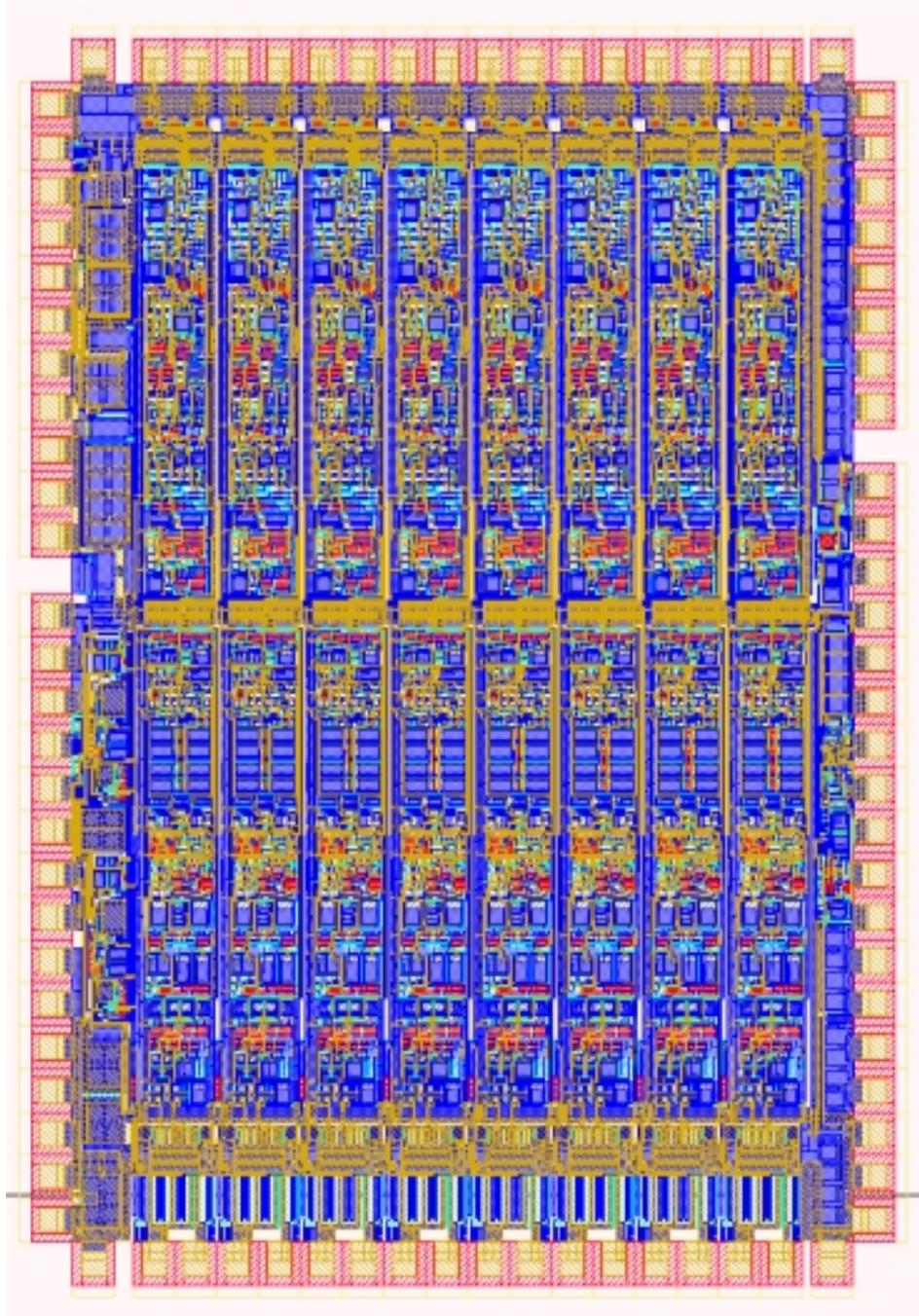
- ◇ MAXIM SHPi Analog Bipolar Process
- ◇ Well Characterized, Radiation Tolerant
- ◇ Active devices: Vertical npn transistors
- ◇ Passive devices: Active Base ( $1.2 \text{ k}\Omega/\text{sq}$ ) & P+ resistors, CMOS capacitors ( $0.5 \text{ fF}/\mu \text{ m}^2$ )
- ◇ Die Size:  $5.4 \text{ mm} \times 3.9 \text{ mm}$
  
- ◇ MAXIM Quickic8 Layout Tool
- ◇ >800 hand-placed components per channel
- ◇ >6000 components per chip

**Good isolation in layout to minimize cross-talk**

**Conservative “in-house” design rules for high yield**

**Layout details allow circuit modifications through metal mask changes (cheaper and faster). Accomplished through strategic placement of components.**

# Layout



## ASDQ Specs

<b>Overall Specifications</b>	
Size	$5.4\text{ mm} \times 3.9\text{ mm}$
Technology	Rad-Hard Analog Bipolar
Channels	8
Pins	64
Package	Quad flat pack
Required power (stability)	$\pm 3\text{V DC}$ ( $\pm 5\%$ )
Power Dissipation (channel)	$40\text{ mW}$
Channel Crosstalk	$\leq 1\%$
Threshold Temperature Sensitivity	$0.1\text{ fC}/10^\circ\text{C}$
Saturation (Tail Cancellation)	Linear to 600 fC
Saturation ( $dE/dx$ , no attenuation)	120 fC
Saturation ( $dE/dx$ , attenuation)	240 fC (reduced resolution)

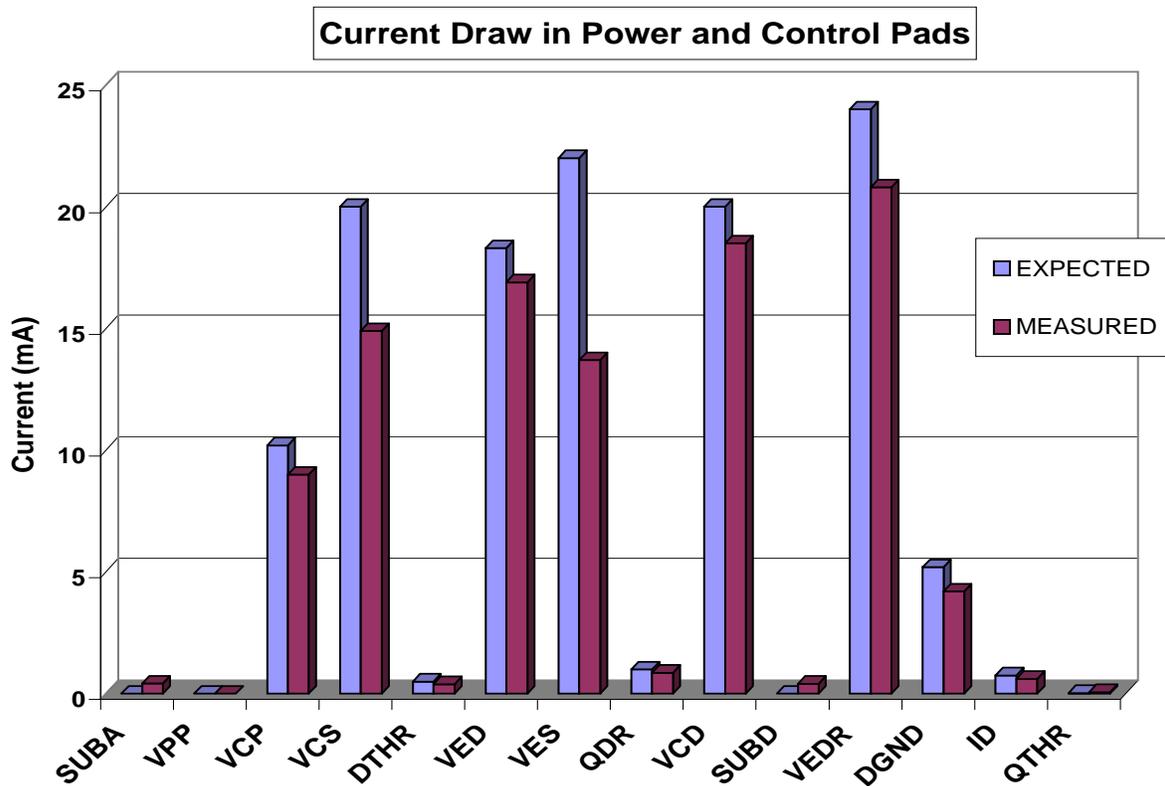
<b>Signal Input</b>	
Input Impedance (Low Freq.)	$260\Omega$ (Total: $300\Omega$ )
Input Impedance (High Freq.)	Roll-off by $\sim 30\%$ at $\sim 30\text{ MHz}$
Noise ( $10\text{pF}$ inp. cap)	$\sim 2300\text{e}$
Noise ( $10\text{pF} + \text{COT} + \text{Term. Res}$ )	$\sim 3800\text{e}$

For 3fC Thresh: S:N  $\sim 5:1$

## Tests on the Prototype Wafer

- ◇ Each wafer has  $\sim 250$  ASDQ sites
- ◇ Ordered: 120
- ◇ Power Up
- ◇ Threshold stability
- ◇ Different size pulses (2 fC to 200 fC)
- ◇ Discriminator Output Width  $dE/dx$  (ON/OFF)
- ◇ Checks of chip controls
- ◇ Double pulse resolution
- ◇ Time-Slewing
- ◇ Calibration circuit
- ◇ Yield

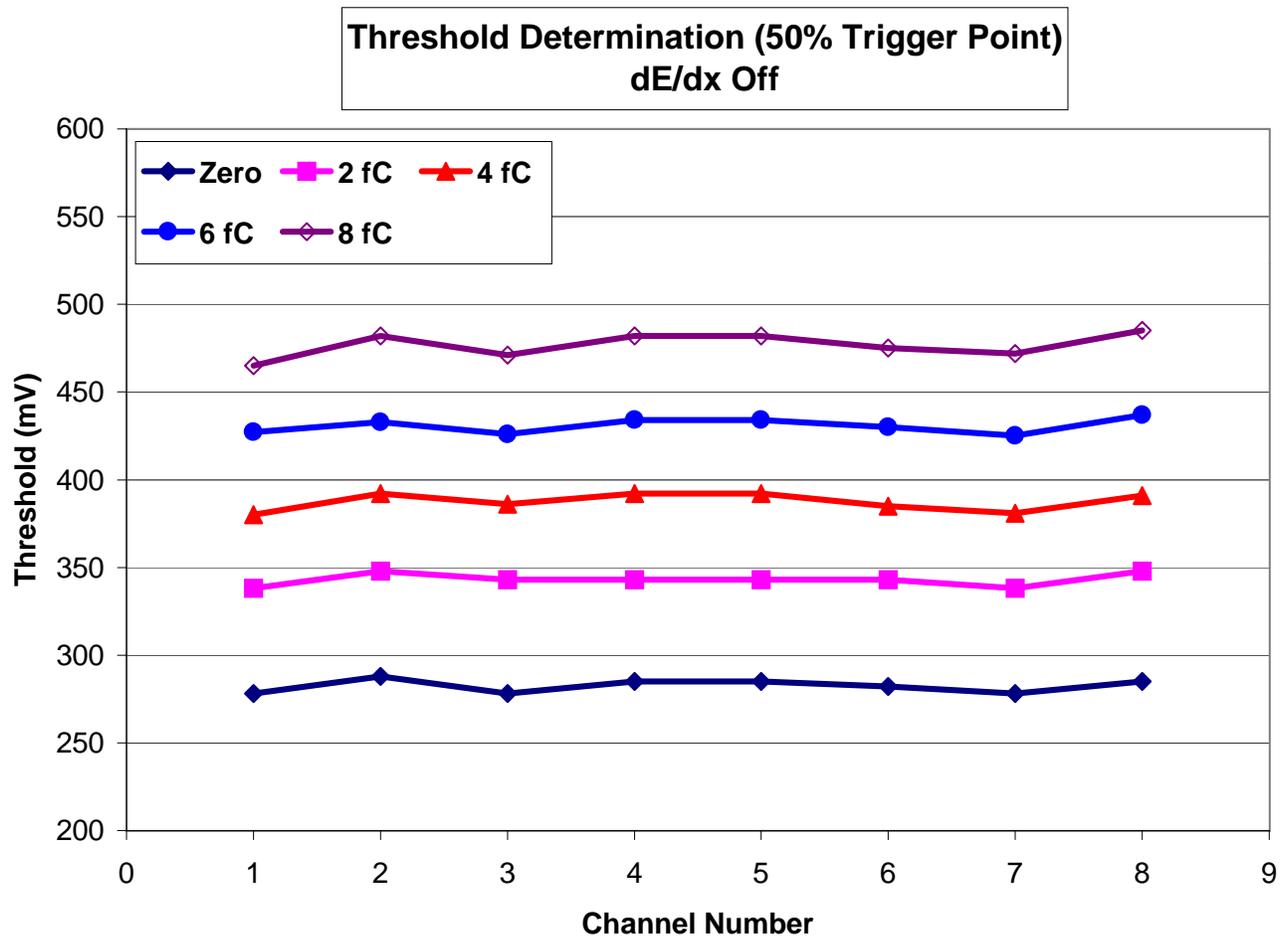
# Current draw in Power and Control pads



Consistent with SPICE

# Threshold Uniformity

Check thresholds for different charges and channels

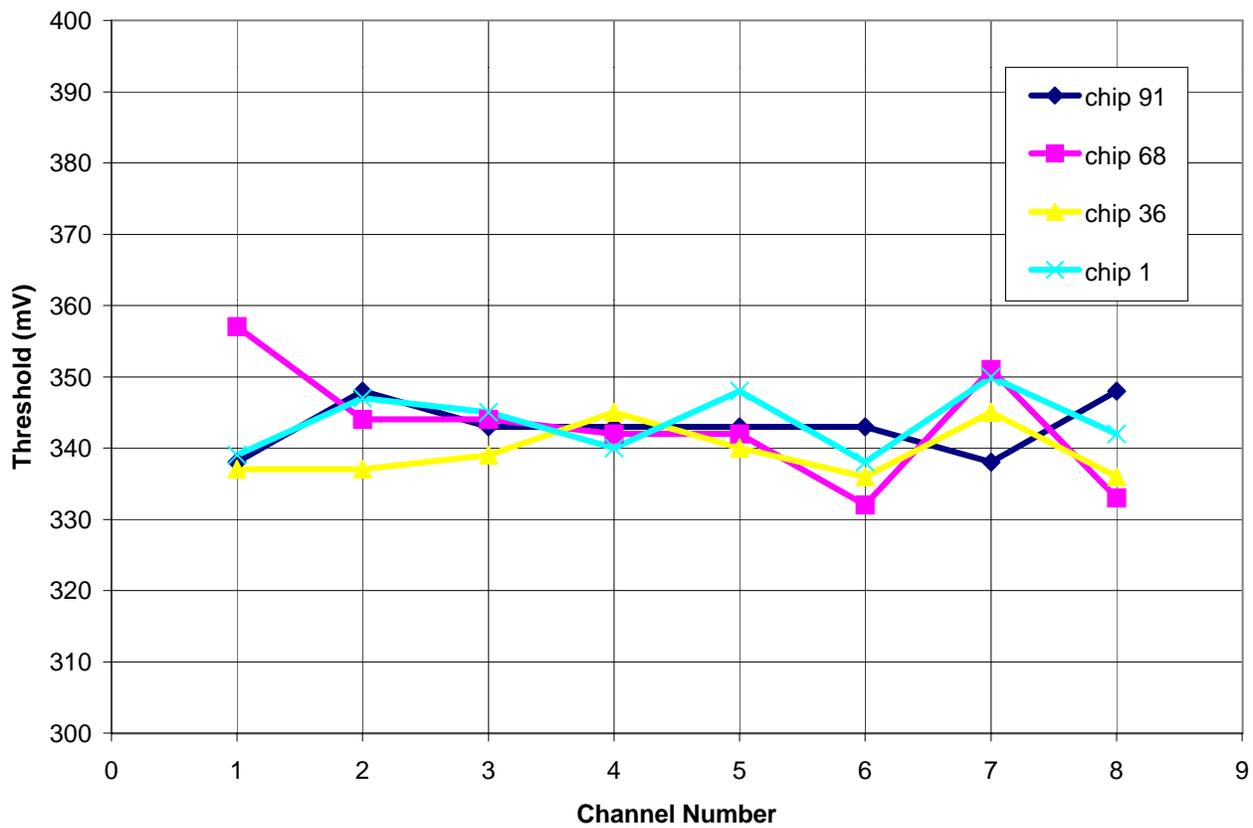


Good threshold uniformity and linearity

# Threshold Uniformity

Check 2 fC thresholds for different chips

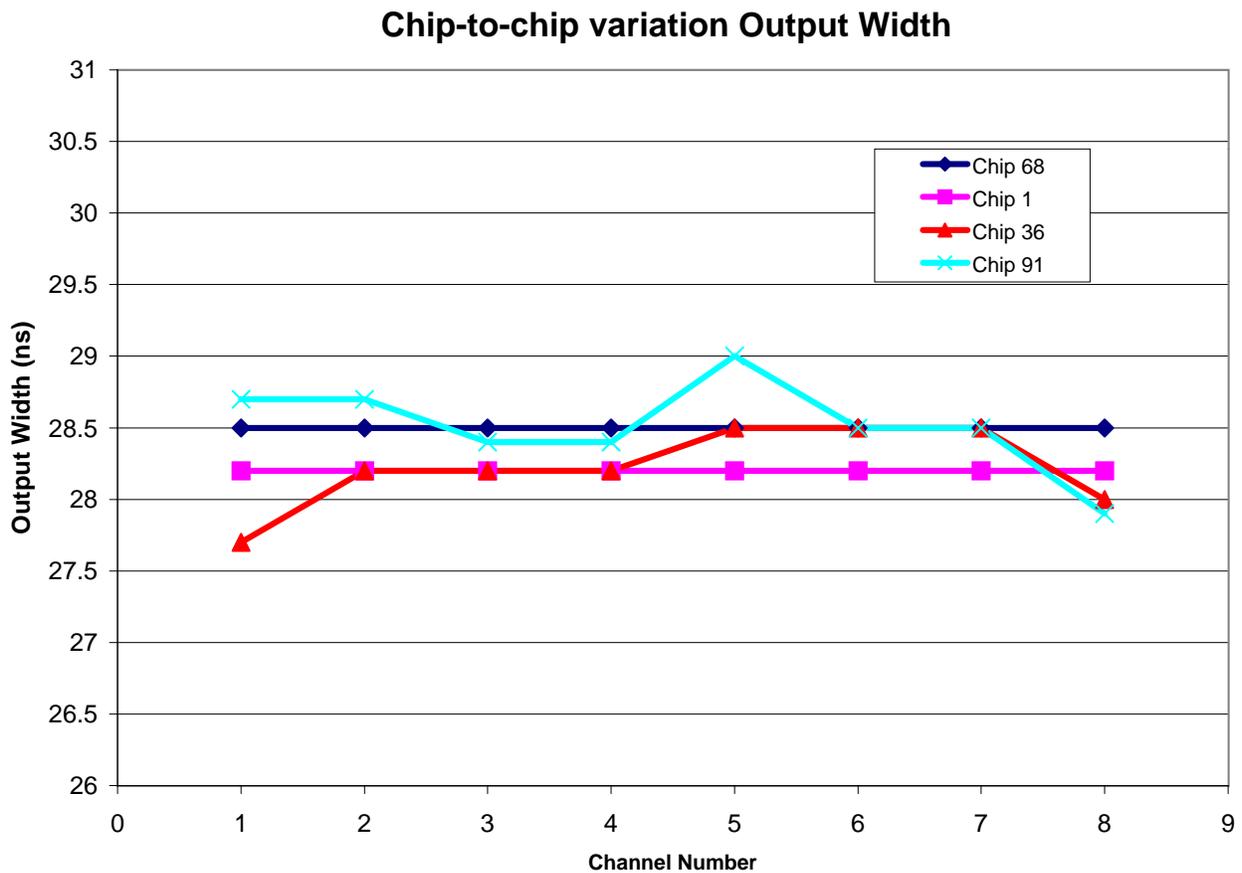
Chip-to-chip Threshold Variation



Good chip to chip uniformity

# Disc Output Width

Check chip-chip Disc output width uniformity



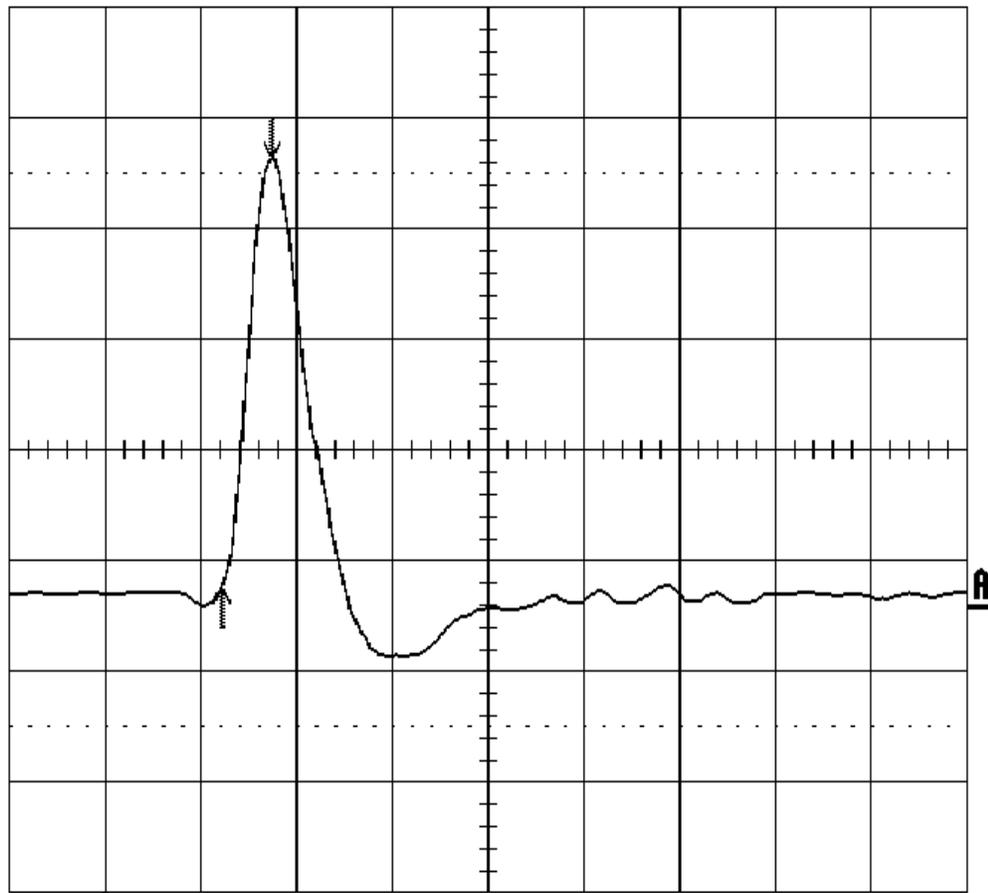
Good chip to chip uniformity

# BLR Monitor

Inject  $Q=20$  fC into the channel. Check output at the BLR monitor point.

17-Mar-98  
18:32:38

Average (2)  
20 ns  
2.15 mV  
-8.345 mV  
1518 swps



20 ns

- 1 disabled
- 2 5 mV 50Ω
- 3 50 mV 50Ω
- 4 disabled

$\Delta t$  -10.5 ns  $\frac{1}{\Delta t}$  -95.2 MHz



Ext AC -80 mV 50Ω

1 GS/s

STOPPED

Consistent with SPICE

# BLR Monitor

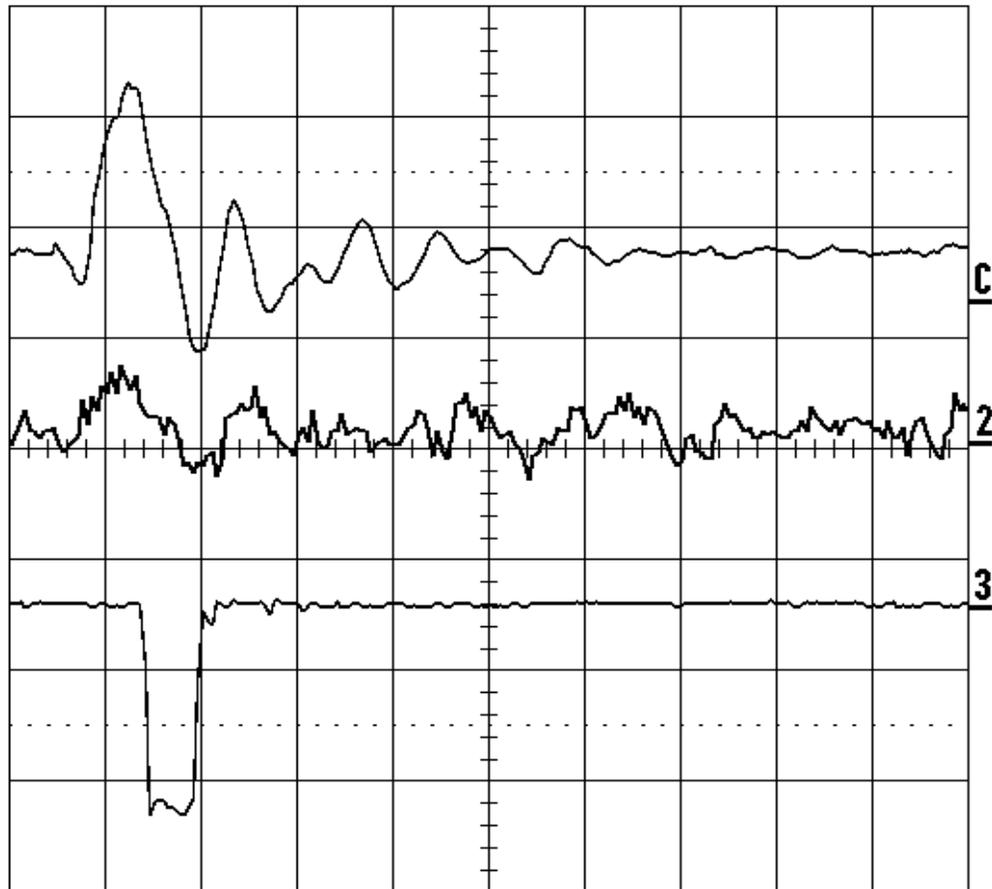
Inject  $Q=3$  fC into the channel. Check output at the BLR monitor point. (2 fC thresh)

26-Mar-98  
22:16:21

**0**: Average (**2**)  
20 ns  
0.70 mV  
—254 swps

**2**  
20 ns  
2.00 mV

**3**  
20 ns  
50 mV



20 ns

← 96 ns

- 1** disabled
- 2** 2.00 mV 50Ω
- 3** 50 mV 50Ω
- 4** disabled



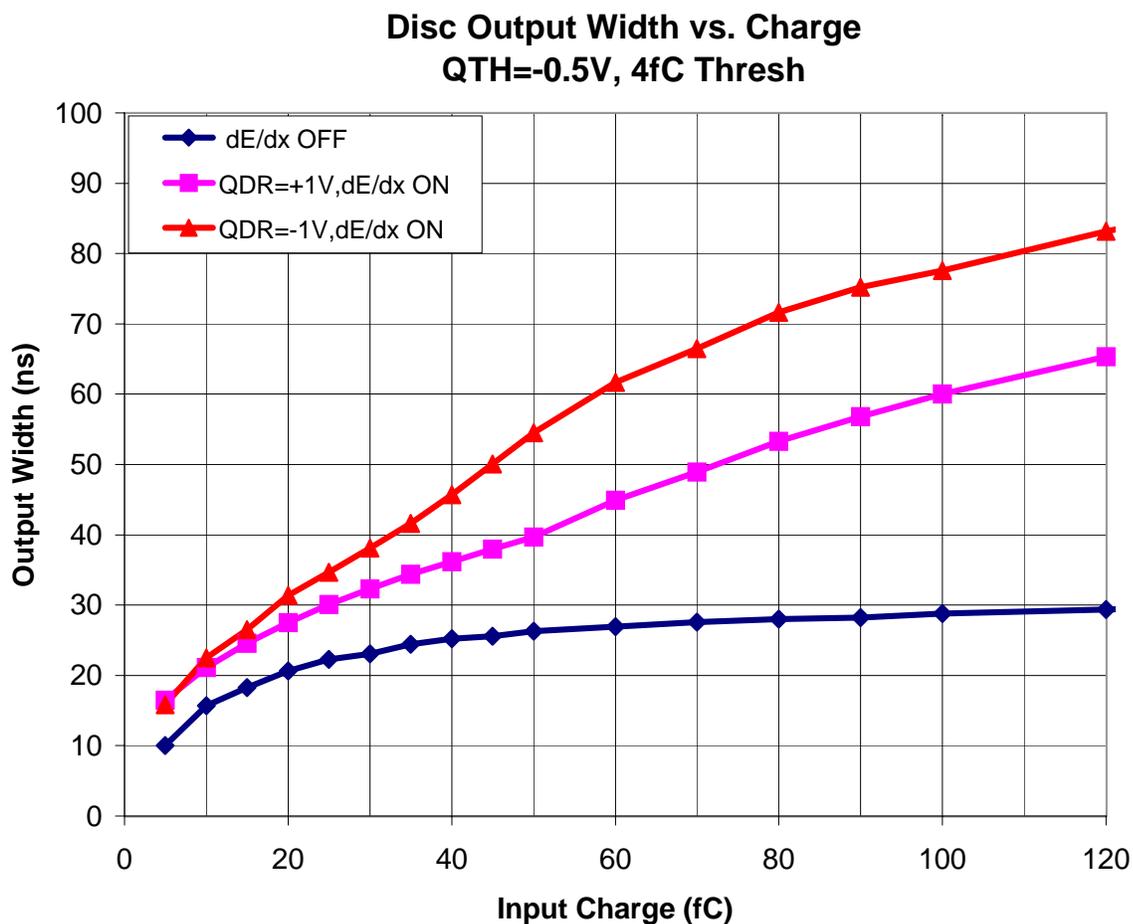
Ext AC -70 mV 50Ω

1 GS/s

STOPPED

# $dE/dx$

Check Disc Output width ( $dE/dx$  On and Off)

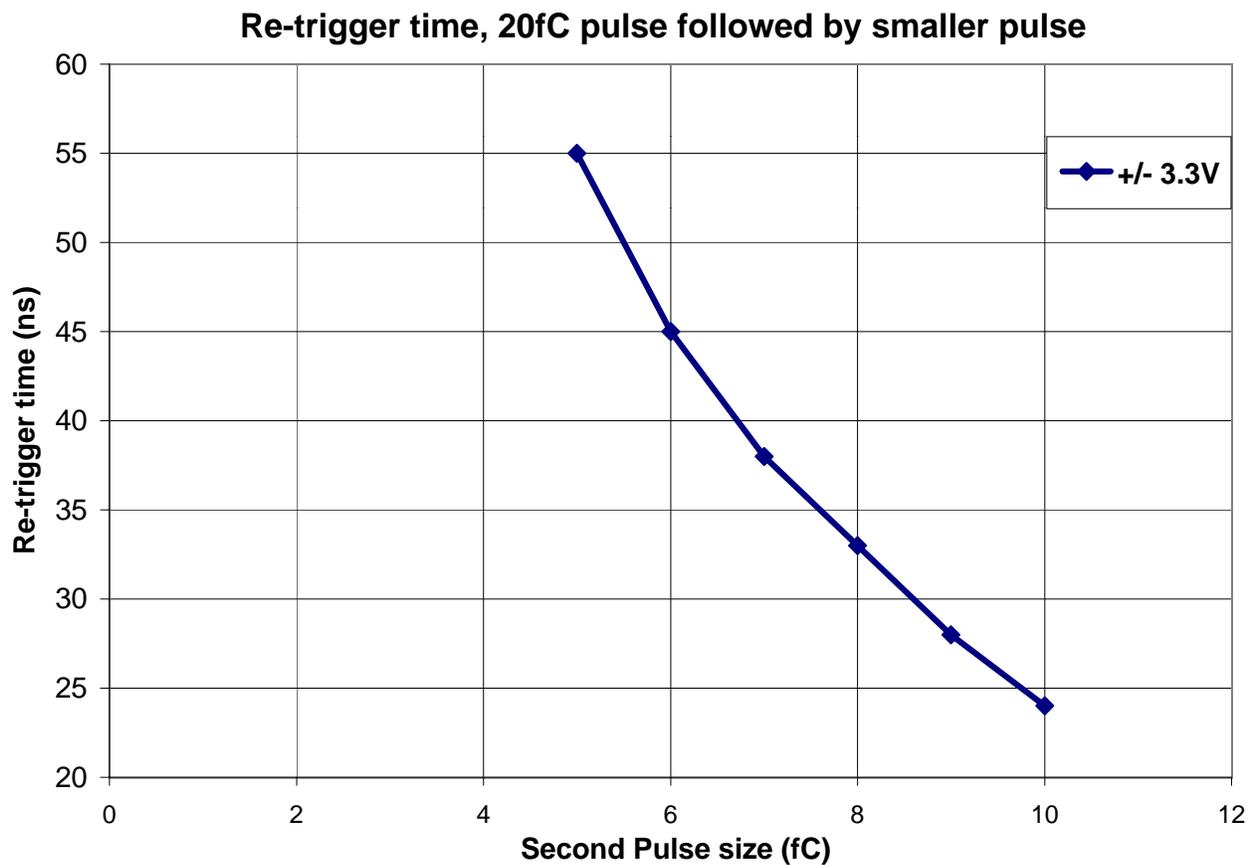


Can adjust the width by varying the drain current

$dE/dx$  works

## Double-Pulse Resolution

20 fC pulse followed by a smaller pulse. (dE/dx en-



For signals  $\geq 0.5\text{MIP}$ ,  $\leq 25\text{ ns}$  (2.3 mm)

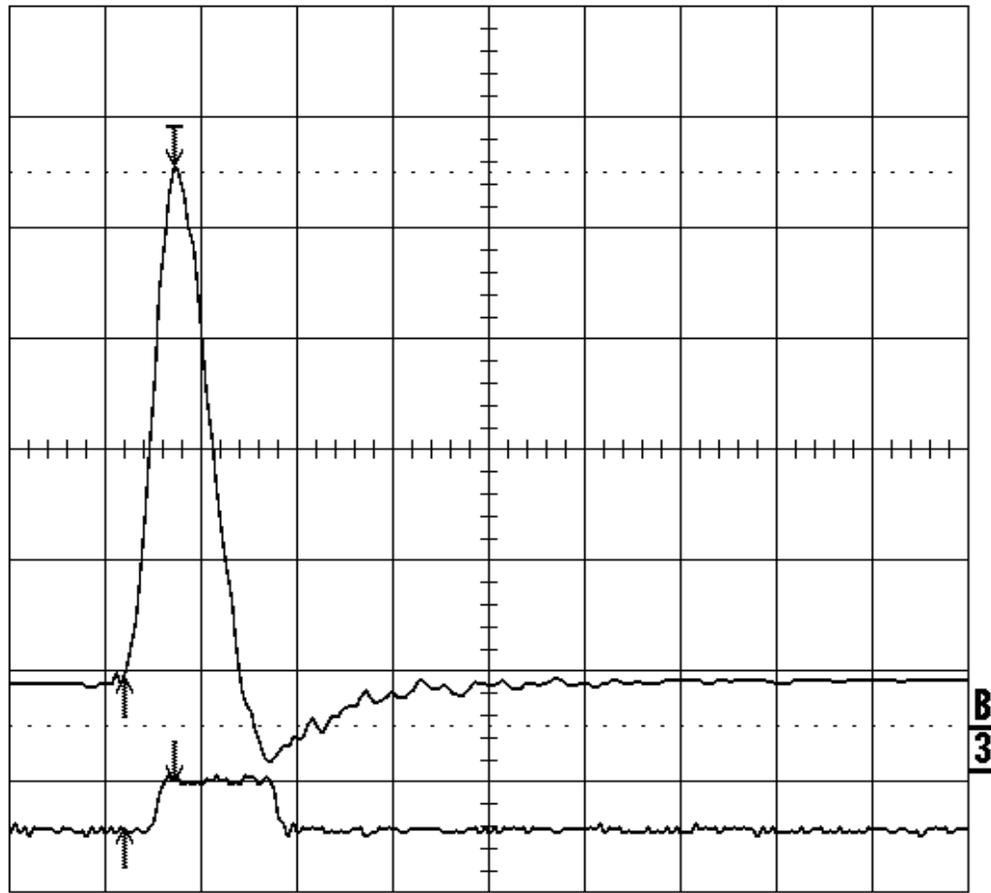
# Calibration Circuit

A 30 fC calibration pulse at the BLR monitor point and the discriminator output.

18-Mar-98  
18:54:03

3  
20 ns  
200 mV  
-84 mV

3: Average (2)  
20 ns  
4.05 mV  
-18.79 mV  
380 swps



20 ns

← 118 ns

$\Delta t$  -10.6 ns  $\frac{1}{\Delta t}$  -94.3 MHz

1 GS/s

- 1 disabled
- 2 10 mV 50 $\Omega$
- 3 .2 V 50 $\Omega$
- 4 disabled



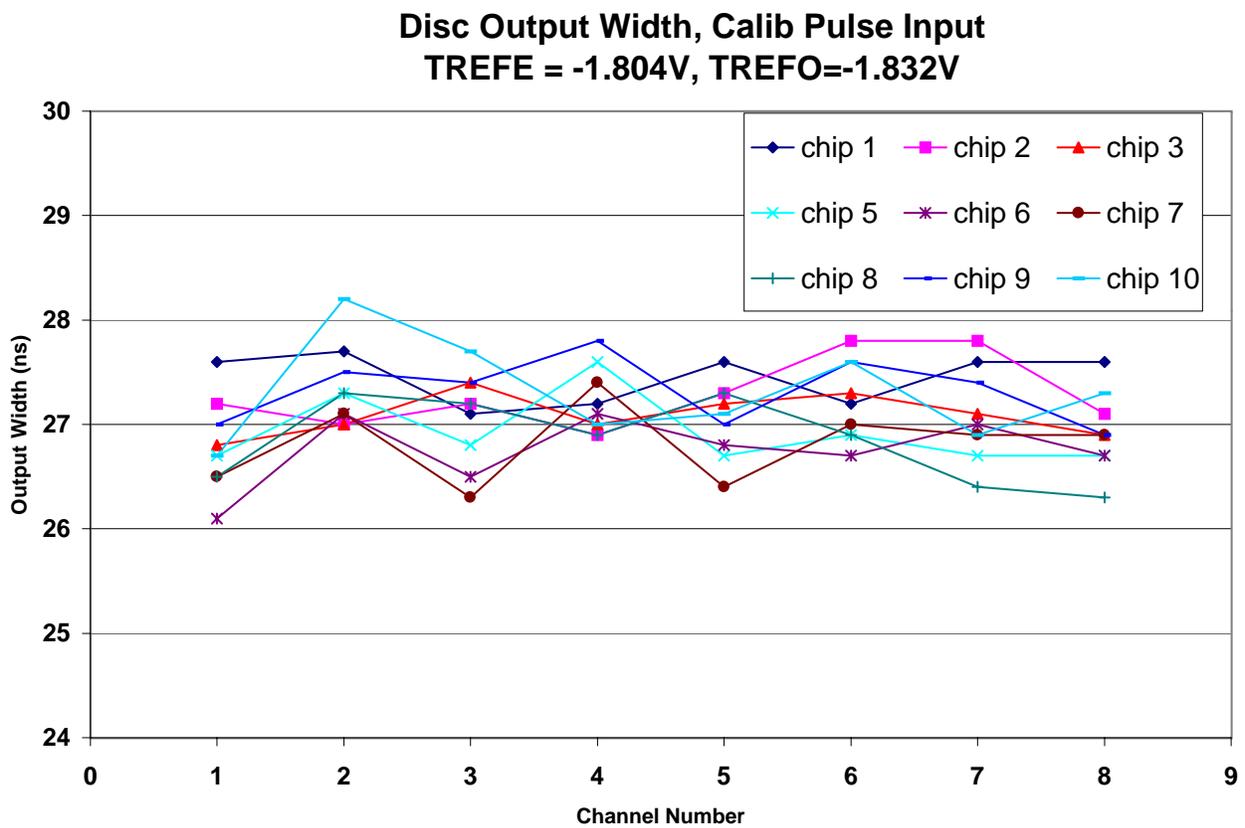
Ext AC -75 mV 50 $\Omega$

□ STOPPED

Good range of calibration (0-30 fC)

# Calibration Circuit

Good discriminator output width uniformity for Calibration pulses



## Prototype Wafer Yield

★ Tested:  $\approx 200$  channels

★ Failed: 1

★ Yield  $> 90\%$

## Test Summary

- ★All controls and features perform as expected
- ★Amplitudes and thresholds nearly identical (chip/channel)
- ★Good output timing uniformity (chan-chan)
- ★BLR, Attenuator, Monitor,  $dE/dx$ , Calibration work
- ★Can run at low threshold (2 fC)
- ★Good yield
- ★Agreement with SPICE

## **Future Plans**

- ★ ASDQ board is in fabrication (Due back May 4)
- ★ Based on test-bench measurements, ready to submit the current design for production
- ★ Need chamber measurements (PCB) to verify performance