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The ASDQ ASIC for the Front End electronics of the COT

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Abstract

The ASDQ ASIC provides eight channels of Preamplifier, shaper, dE/dx and discriminator circuitry for the Run II COT front end electronics. It fulfills the competing requirements of short measurement times (≈ 7 ns), good double pulse resolution (≈ 30 ns), low power (≈ 40 mW/ch) and low operational threshold (≈ 2 fC) by implementing a fully differential circuit. Baseline Restoration is implemented to allow fast performance in a typical Run II conditions. In addition, Ion tail compensation is provided using the pole-zero cancellation technique. The measurement of the charge (dE/dx) is encoded into the width of the discriminator output. The ASDQ ASIC has been implemented on a $5.4\text{ mm} \times 3.9\text{ mm}$ silicon substrate using a radiation tolerant analog bipolar process.

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1 Overview

The ASDQ ASIC provides eight channels of Preamplifier, shaper, dE/dx and discriminator circuitry for the Run II COT front end electronics. The purpose of this note is to present the necessary documentation about the ASDQ's design, performance and usage. The note is roughly divided into two major parts. The first part comprises of sections 2, 3 and 4, and provides an overview of the COT relevant for this document. Reader's familiar with this material are advised to skip ahead. The second part, consisting of section 5 provides the details of the ASDQ. In the end, simulations of the ASDQ performance are presented in section 6.

2 The Central Outer Tracker

The Colliding Detector Facility (CDF) at Fermi National Accelerator Laboratory (Fermilab) is being upgraded to accommodate a higher 7.6 MHz beam crossing rate (132 ns bunch spacing time) that is planned for Run II [1]. The new Central Outer Tracker (COT) is designed to operate with a maximum drift time of 100 ns compared to 706 ns for the Run I Central Tracking Chamber (CTC). This reduction in drift time is achieved by reducing the maximum drift distance of electrons to $l_{drift} = 0.9\text{cm}$ ($\sim 25\%$ of the CTC drift distance) and by using a 50:35:15 Ar-Ethane- CF_4 gas mixture with a faster drift velocity of $90 \mu\text{m/ns}$. In 36 bunch mode of operation, Run II luminosities will be approximately eight times higher than typical Run I luminosities. The performance of the COT is expected to be similar to that of CTC under these conditions. Similarly, in 108 bunch operation with luminosities of $\sim 4 \times 10^{32} \text{ cm}^{-2}\text{s}^{-1}$ (~ 20 times the luminosities of Run I), the COT is expected to maintain its performance. Apart from the factor of four in the number of cells, these performance requirements are met with faster electronics and a modified geometry of the COT cells to allow a more uniform charge collection.

Each COT cell is approximately 1 cm^2 in cross section and 3.1 meters in length. A cell consists of alternating potential and sense wires (13 potential and 12 sense wires respectively) enclosed by cathode field panels consisting of gold plated Mylar sheets. Each sense wire along the length of the cell attaches to the high voltage supply through a 550 pF decoupling capacitance

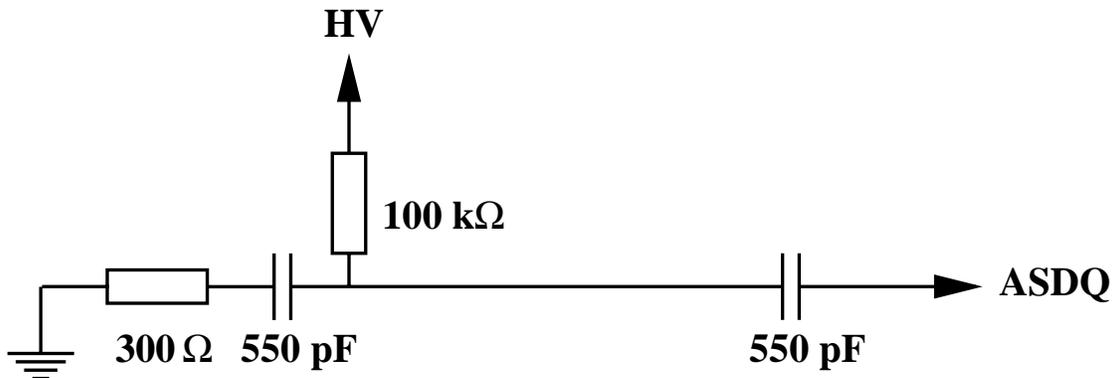


Figure 1: *The COT wire connection diagram.*

with a resistance of 300Ω to ground on one end. The high voltage connection to the wire is through a $100\text{ k}\Omega$ resistor. The COT wire connection scheme is shown in figure 1. The resistance of the sense wire is 180Ω , the total impedance of the COT cell is 300Ω , and the stray capacitance is estimated to be 10 pF . The field panels are the equivalent of the field wires of the CTC, and allow for a higher and a more uniform drift field in a COT cell compared to the CTC. With a higher drift field, the Lorentz angle for the COT is 35deg compared to 45deg for the CTC. The ends of the cells are mechanically and electrostatically sealed by additional Mylar strips called Shaper Panels. The potential wires are held at a potential of $\sim 1.9\text{ kV}$, the sense wires at $\sim 2.9\text{ kV}$ and the cathode field panel is grounded. The drift field in the cell is set to $\sim 2.5\text{ kV/cm}$.

The general scheme of the COT front end electronics is shown in figure 2. One side of the COT sense wire connects to the ASDQ daughterboard. Each daughterboard houses three ASDQ ASIC's. The signals from the daughterboard (24 channels) are carried off in micro-coaxial cables to the TDC. Each TDC receives the output of three ASDQ daughterboards (96 channels). The repeater boards that sit between the daughterboards and the TDC in the electronics chain compensate for the shaping of the signal through the micro-coaxial cables. The ASDQ ASIC's provide full analog signal processing between the COT chamber and the TDC.

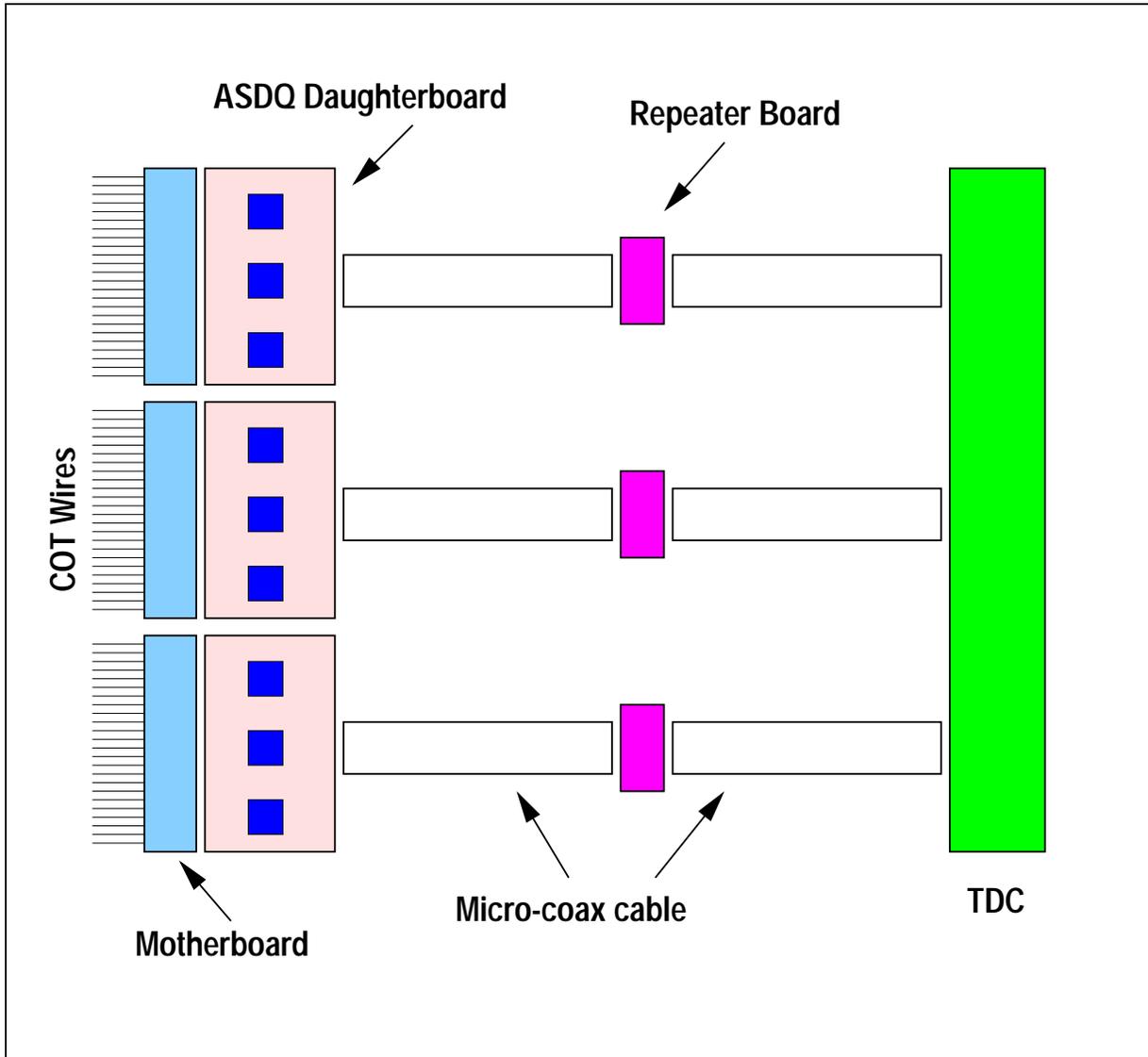


Figure 2: *The COT front end electronics scheme.*

3 ASDQ Requirements

Acceptable high luminosity operation requires good double-pulse resolution for the electronics. Since the gas gain for the COT has a limited range for stable operation and the signal collection time is limited by the double-pulse resolution requirement, the noise in the electronics needs to be kept at a low level. In addition, to ensure that the double-pulse resolution is not degraded by the electronics, the discriminator is required to have a sub-nanosecond timing accuracy. All these requirements result in a high bandwidth and low threshold circuit that is susceptible to noise pickup from RF sources and to signal-to-noise losses. To minimize the RF pickup and the signal-to-noise losses, the electronics are mounted on the COT itself. This presents an additional constraint of low power requirement of the circuit in order to minimize heat dissipation in the tracking volume of the CDF-II detector.

4 COT Signal

When a charged particle traverses a cell in 50:35:15 Ar-Ethane-CF₄, it leaves an ionization trail in its wake. From experimental data[2], there are ~ 28 clusters per cm for a minimum ionizing particle in Ar. The cluster size distribution in terms of the number of electrons (N_e) is also determined from experimental data, and is shown in figure 3. About 85% of the clusters have three or fewer electrons in them. The distribution has a long tail, which has been truncated at $N_e = 100$, and the mean of the distribution¹ is about 3.

The electrons in the ionization trail move towards a sense wire of the cell with the gas drift velocity of $v_{drift} \sim 90 \mu\text{m/ns}$. Within a few diameters of the sense wire, the large gradient of the logarithmically increasing electric field accelerates the electrons and they initiate a limited avalanche through secondary ionizations. The average number of secondary ionizations produced per primary electron, or the *Gas Gain*, is determined by the potential of the sense wire and is approximately $G \sim 2 \times 10^4$ for the COT chamber. A high gas gain results in rapid aging of the wires, and may also deteriorate the signal. Therefore, the gas gain of the chamber has a limited range for stable operation.

¹If the distribution is not truncated then the mean can be arbitrarily large.

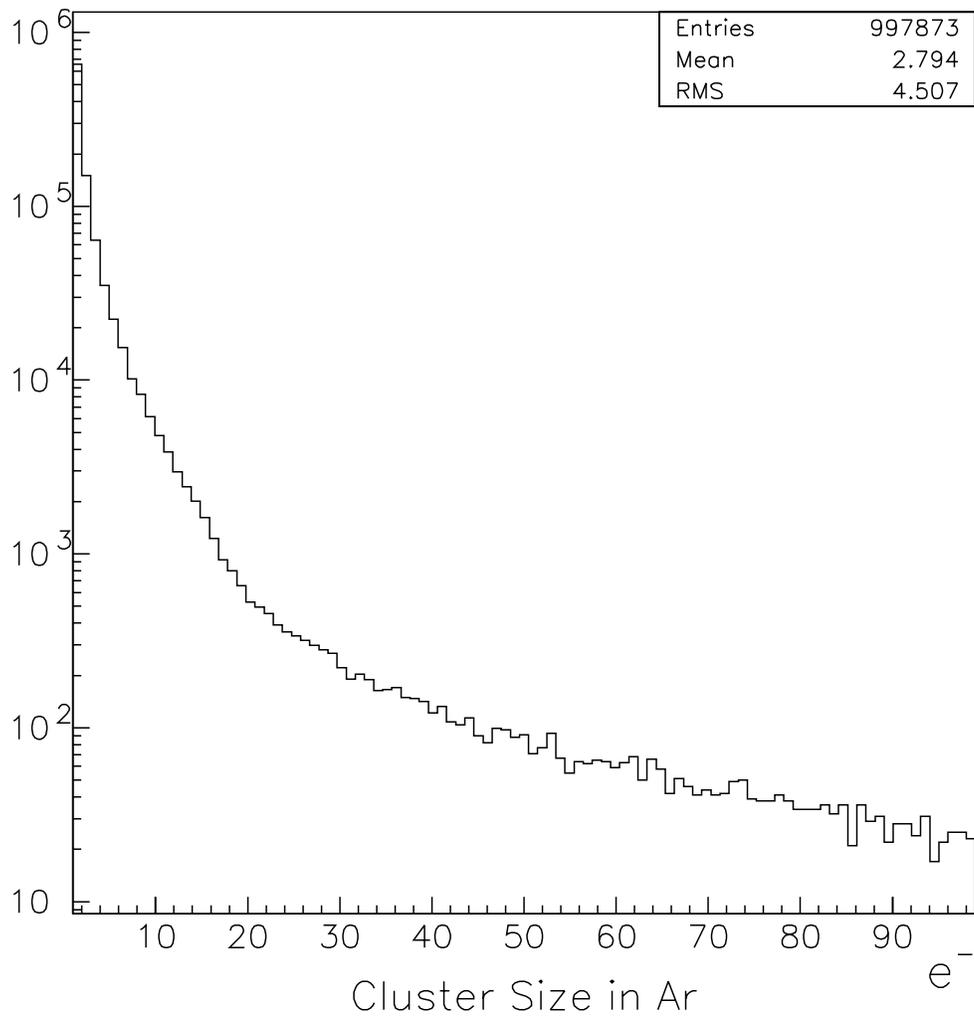


Figure 3: *Cluster size distribution for minimum ionizing tracks in Argon.*

The typical distance traveled by a minimum ionizing particle in the gas is 3 mm. In order to determine the total number of electrons (N_i) that drift to the sense wire (in the absence of Gas Gain), the mean number of clusters produced per cm (28/cm) is Poisson fluctuated and then combined with the individual cluster sizes. The resulting distribution is shown in figure 4. On average about 20 electrons drift to the sense wire. For an operational threshold of 5 (10) electrons, approx. 95% (80%) of the ionization signal is accepted. The figure also shows the distribution for a 5 mm path of a minimum ionizing particle. In that case the average number is about 30.

The total amount of charge deposited by a typical minimum ionizing track is given by $Q \sim N_i \cdot G$. This corresponds to a charge of 4×10^5 electrons or 64 fC². However, not all of this charge is available for signal processing to the front end electronics.

Electrons produced by secondary ionization drift immediately to the sense wire. Since they are already close to the potential of the sense wire, they do not contribute significantly to the total signal. The positive ions produced in the avalanche move away from the sense wire and induce the signal on the wire that is detected by the readout electronics. Since the drift velocity of the relatively massive ions is much smaller than that for the electrons, they produce a measurable signal, referred to as the *ion tail*, on the wire that lasts for several microseconds. For good double-pulse resolution it is essential that both the charge collection time, and the inherent noise in the measurement (which is favored by a long charge collection time) be minimized. The optimal strategy chosen is to collect enough charge to efficiently detect the initial charge while rejecting the remaining long tail in the signal.

The time evolution of the signal can be determined by analysing the drift of charge in the electric field surrounding the sense wire. For the case of a proportional tube, this is done in detail elsewhere[2]. Here we only present the qualitative arguments.

In the case when the signal rise times are shorter than the typical timescales ($\tau = CR$) of the capacitances and resistances connecting to the sense wire, the potential of the sense wire is re-established quickly. The readout electronics then act as a current source, and the signal manifests itself as a current that flows in the readout circuit. In terms of the wire radius (a), the tube radius (b), the radial electric field of the wire ($E(r)$), the ion mobility (μ_0)

²1fC= 6250 electrons

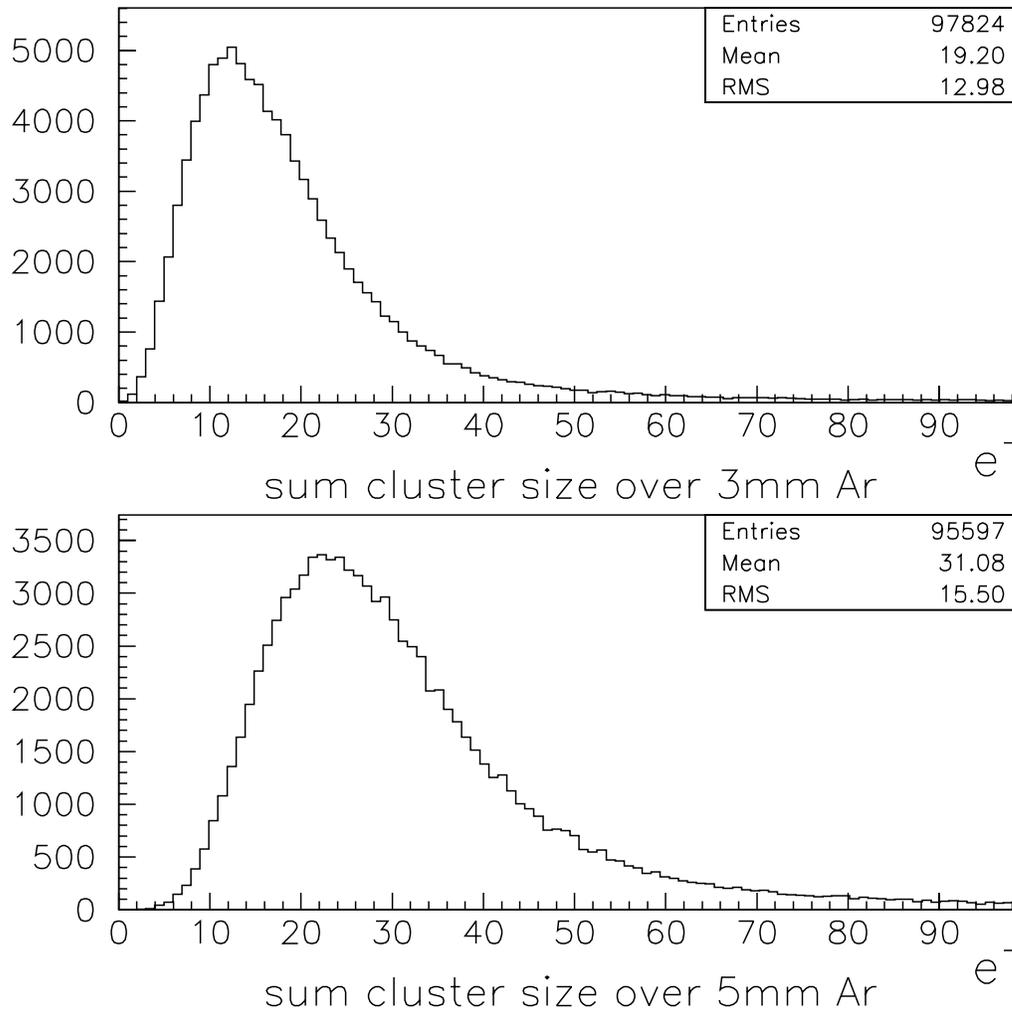


Figure 4: *Total number of electrons produced by a minimum ionizing particle that drift to the sense wire.*

and the deposited charge (q), the time evolution of the current is described by:

$$I(t) = \frac{q}{\ln(b/a)} \frac{1}{t + t_0}$$

Here $t_0 = a/2\mu_0 E(a)$ is the characteristic time for the sense wire in a given gas mixture. The current distribution in time is very narrowly peaked at zero, with a width t_0 . The remainder of the signal is a factor b^2/a^2 wider than t_0 . This $1/(t + t_0)$ behavior is characteristic of the signal induced by the ions. Strictly, this holds only in the case of perfect radial symmetry of the system, and neglects the effect of the electron contribution to the signal.

For the COT cells, such a simple treatment would not be sufficient. The electrons arrive almost instantaneously on the wire, and their contribution, is not negligible during time periods equal to the measurement time of the circuit. The electron component of the signal is incorporated by adding to the $1/(t + t_0)$ term a delta function at time $t = 0$ whose contribution to the charge is one-tenth of the charge collected in the measurement time of the circuit (8 ns). The COT signal is then parameterized as:

$$I(t) = \frac{k}{t + t_0} + \delta(0) \cdot \frac{1}{10} \int_0^8 I(t) dt \quad (1)$$

Here $k = -0.8$ fC and $t_0 = 3$ ns have been determined using previous studies of drift chambers with similar properties[3].

Figure 5 shows the characteristic shape of this signal as produced by a circuit that mimics the electron spike and the ion tail. It should be noted that this is the signal of one electron-ion pair on the wire. The actual signal on the sense wire is the sum of all the individual point ionizations and is shown in figure 6. This figure has been produced using GARFIELD[5]. More details about GARFIELD simulations are presented in Section 6.

The measurement time of 8 ns for the circuit has been chosen by studying digitized signals from a prototype COT chamber that have been fed into a SPICE simulations[6]. In addition, a longer integration time also decreases the bandwidth, and therefore improves the signal to noise ratio by lowering the noise.

In order to determine the fraction of of total deposited charge that is available in the first 8 ns, one should integrate equation 1. Since the ion-tail

extends for several microseconds, the fraction is normalized relative to the charge collected in $t_{1/2} = 1.5\mu s$. It is seen that only $\approx 18\%$ of the total deposited charge is available in the first 8 ns.

In addition, only 37.5% of the charge available during the first 8 ns makes its way into the circuit. This is because of two reasons. First, since the signal propagates in both directions, only 50% of the charge available comes into the circuit. In addition, the stray capacitance of the system results in further loss of charge equal to $C_{stray}V_{sense}$. This figure of 37.5% does not include the effects of a further loss of charge due to the attenuation of the signal as it travels down the sense wire which acts as a transmission line. Therefore, the total amount of “usable” charge for signal processing is about $18\% \times 37.5\% = 7\%$ of the charge deposited on the wire.

As a benchmark, a minimum ionizing particle deposits about 7 fC of usable charge into the circuit.

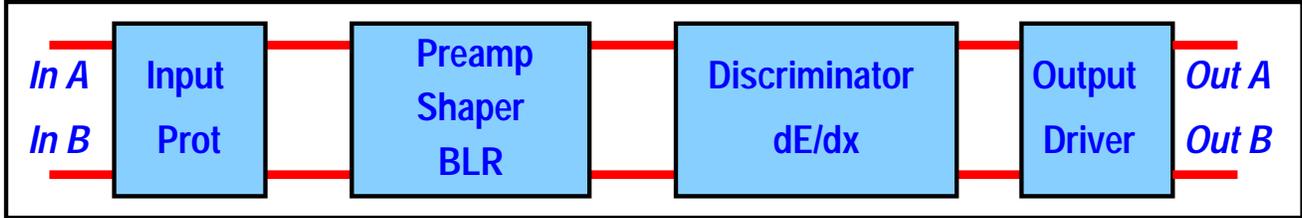


Figure 7: *ASDQ single channel block diagram.*

5 The ASDQ ASIC

5.1 Overview

The ASDQ ASIC has been implemented on a monolithic $5.4 \text{ mm} \times 3.9 \text{ mm}$ silicon substrate using an analog bipolar process. The block diagram of an individual ASDQ channel is shown in Figure 7. An incoming signal from the chamber goes through the following components of an individual channel:

1. Input Protection
2. Preamplifier
3. Tail Cancellation
4. Baseline Restorer
5. Discriminator
6. Width Encoder (dE/dx)
7. Output Driver

The signal from the wire goes into an *input protection* circuit designed to buffer the *preamplifier* from large external positive and negative spikes. The preamplifier amplifies the signal and converts the charge input into a voltage output while minimizing the noise added to the signal.

The presence of the ion tail inhibits efficient high rate operation. Fortunately, the time development of this signal is well understood and can be cancelled by introducing a circuit element whose impulse response produces

a mirror image of the ion tail. This is referred to as *Ion Tail Cancellation* and is implemented in the ASDQ. After the preamplifier, a pole-zero cancellation technique is used to eliminate the ion-tail in the signal. An additional pole-zero element removes the tail introduced by the preamplifier.

A large signal in the chamber can introduce a significant shift in the baseline of the pulse. This can artificially cause the signal to stay above threshold for a long time, inhibiting fast performance in a busy environment. For this reason a circuit element is introduced to bring the signal quickly back to its nominal baseline. This is referred to as *Baseline Restoration*.

After the tail cancellation, the signal is fed into the *baseline restorer* which brings the signal back to nominal zero. The shaped signal is then DC coupled to a three stage *discriminator*. If an above-threshold signal is detected, a charge measurement is performed using the dE/dx element.

Due to the energy of the colliding beams, crude particle identification is possible using a pulse height information from several cells. Specifically, the number of primary ions produced in the gas by electron tracks is significantly (up to 40%) larger than those produced by heavier particles due to the highly relativistic nature of the electron in comparison to other heavier particles. This charge information can be crudely encoded into the comparator width but would be far too ambiguous if simply treated as the time spent by the signal over threshold. In the ASDQ, once an above-threshold signal is detected, a long time-constant signal integration is used to keep the comparator from returning to baseline before the signal from several primary ions can be integrated. This feature is often referred to as dE/dx . This feature can be turned off which is of utility for inner COT cells that are expected to operate at high rates, .

Finally, the output is fed into a differential open collector *output driver* for final shaping. The evolution of the signal after the various stages of an individual ASDQ channel is shown in figure 8.

Various controls are also provided in the circuit. A selectable *attenuator*, when enabled, reduces the amplitude of the signal into the baseline restorer by a factor of 2. The leading and trailing edge thresholds of the discriminator can be adjusted externally. This impacts the triggering threshold for the discriminator and the width of its output pulse. The width of the discriminator output can also be adjusted by varying the drain current in the integrating capacitors in the width encoder. A larger drain current corresponds to a faster return to the trailing edge threshold of the discriminator and therefore

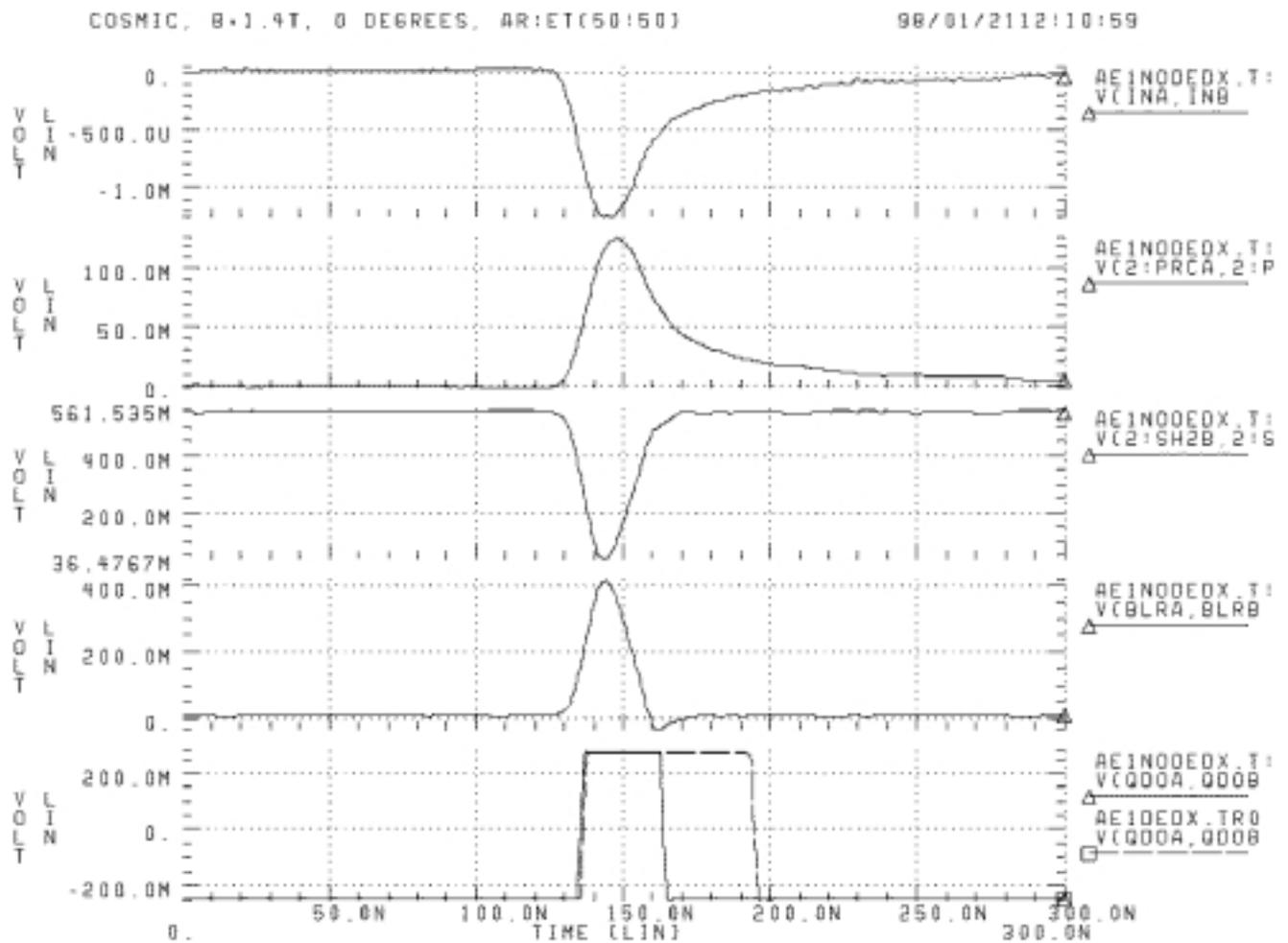


Figure 8: Signal evolution for a Cosmic ray track which deposits 80 fC into the Preamplifier. From top to bottom the input into the Preamplifier, the output of the Preamplifier, the output of the Shaper, the Output of the Baseline Restorer and the output of the Discriminator (dE/dx on and off) are shown.

a smaller discriminator output pulse width. In addition, the output width may also be changed by changing the a trailing edge threshold.

Two calibration circuits housed on the ASDQ provide COT-like pulses to the even and odd numbered channels respectively. The pulses are programmable in the range of zero to ≈ 30 fC. The calibration circuits provide an *in situ* capability to determine the absolute delay in the response (t_0) and the output width to charge relation for every channel.

A monitor circuit allows the user to examine the “analog” portion of the signal in the circuit. Specifically, the output of the BLR can be studied for the eighth channel of every ASDQ for debugging purposes.

The CTC readout electronics were fabricated using a mixture of discrete components and commercial Integrated Circuits. The ASDQ borrows from past experience with wire chamber ASIC’s (ASD8[3] and ASDBLR[4]) and the original CTC charge encoding scheme. In this design we have modified the Baseline Restorer used in the ASDBLR, replacing it with a controlled current bridge diode array described later. The Preamp, Tail Cancellation and Shaper circuit is based on previous designs used in the ASD8 and later in the ASDBLR.

In summary, the design of the ASDQ has been driven primarily by the following considerations:

- Good position resolution ($\sim 200\mu\text{m}$)
- Good double-pulse resolution of the circuit with and without dE/dx enabled (~ 20 ns).
- Good charge measurement by the Width Encoder (dE/dx) over a large range (5 fC to 150 fC).
- Low operating thresholds (2 – 3 fC)
- Uniformity of response (channel/chip)
- Good stability of the circuit to temperature and process variations.

The specifications of the present circuit have been studied using SPICE[7], ADS[8], GARFIELD[5] simulations and a prototype COT chamber using Cosmic Ray and Fe^{55} data[6]. In the following sub-sections, the different components of the circuit are described in sufficient detail. Interested readers are strongly encouraged to get the technical details from [3].

5.2 Technology

The ASDQ chip is fabricated using the inherently radiation-hard bipolar technology. This technology offers low intrinsic noise, low intrinsic capacitance, high speeds and the highest transistor gains, g_m , per unit of quiescent current of all commercially available technologies. This particular combination of properties makes it ideal for fast designs with low power requirements and low intrinsic noise. The typical noise level is 2000 ENC. This process offers excellent device matching and well characterized SPICE models. One micron layout rules for the two metal layers allow close packing of devices. The active devices used in this circuit include vertical and lateral npn transistors. The passive components include Active Base (AB) and P+ resistors. The passive components also include CMOS capacitors. Most of the filtering capacitors used in the circuit are provided by the **Cpi** libraries supplied by Tektronix. Other custom devices are constructed during the layout using the basic models contained in the process libraries. For detailed characteristics of the different devices, the reader is referred to the MAXIM technical manual [9].

The layout of the ASDQ was performed using **Quickic8**[10]. Figure 9 shows the layout of the ASDQ chip. The eight individual channels in the chip are visible. The signal enters from the input pads at the bottom of the chip. After passing through the input protection circuitry, it is fed into the preamplifier. The layout of each channel is sub-divided into two areas. The lower half of the chip comprises of the “analog” portion, which includes the preamplifier, shaping and baseline restoration stages. The output of baseline restoration is then sent into the upper half of the chip which contains the “digital” parts of the chip -the discriminator and the width encoder. The smallest rules in the layout are $1.8\mu m$ in width. Along the sides of the chip, the protective decoupling capacitors and the calibration circuitry are visible.

In order to ensure low channel-to-channel cross-talk, good isolation has been implemented in the layout. In addition, in order to maximize the yield, certain “in-house” layout rules have been followed. These rules involve the spacing between the active and passive components, proximity of components to major power and ground buses and shielding of the sensitive areas of the circuit from sources of potential noise pickup. Finally, in order to allow circuit changes through metal mask changes only, extra components have been strategically placed throughout the critical sections of the layout.

HV Protection (Negative Spike)	350 $\mu m \times 400 \mu m$ epi-resistance and epi-P+ resistor diode
HV Protection (Fast Neg. Spike)	32 \times transistor, diode-wired
HV Protection (Positive Spike)	100 $\mu m \times 250 \mu m$ P+ epi-wired

Table 1: Input Protection Specifications.

Metal mask changes are cheaper and faster than more involved changes in the layout.

The ASDQ has been fabricated at MAXIM. Each wafer has been contains about 250 ASDQ sites. The chip is housed in a 64 pin package by IPAC. A thorough characterization of each wafer has been provided by the manufacturer.

5.3 Input Protection

The sense wire of the COT attaches through a 550pF capacitor to the ASDQ. The sense wire is held at a potential of 3 kV, which implies that the capacitor has a stored energy of about 1.5mJ. In the case of a breakdown of a wire, all that energy would be dumped into the ASDQ. Therefore an input protection is necessary. In addition to the input protection provided on the chip, a diode will be present on the ASDQ daughterboard. Figure ?? shows the schematic of the input protection circuit.

Following previous designs, the buried layer is used to form a low value resistor, and P+ resistor bodies are used to provide anodes for a large area multi-contact diode. The incoming signal is fed in parallel to several rake like fingers with multiple epitub contacts to provide a conduction path through the buried layer. The resistance of each leg is approximately 6 Ω . Near the second row of epitub contacts that connect to the preamplifier input, a row of P+ resistors, shorted to ground, provide the contacts for diode protection. The common emitter preamplifier keeps the input voltage at V_{be} above ground. Under normal operating conditions, the P+ resistor bodies do not conduct a signal current. Since the turn-on time for this kind of diode has not been characterized in sufficient detail, a standard large area transistor is included. The base and the emitter of the transistor are connected to ground,

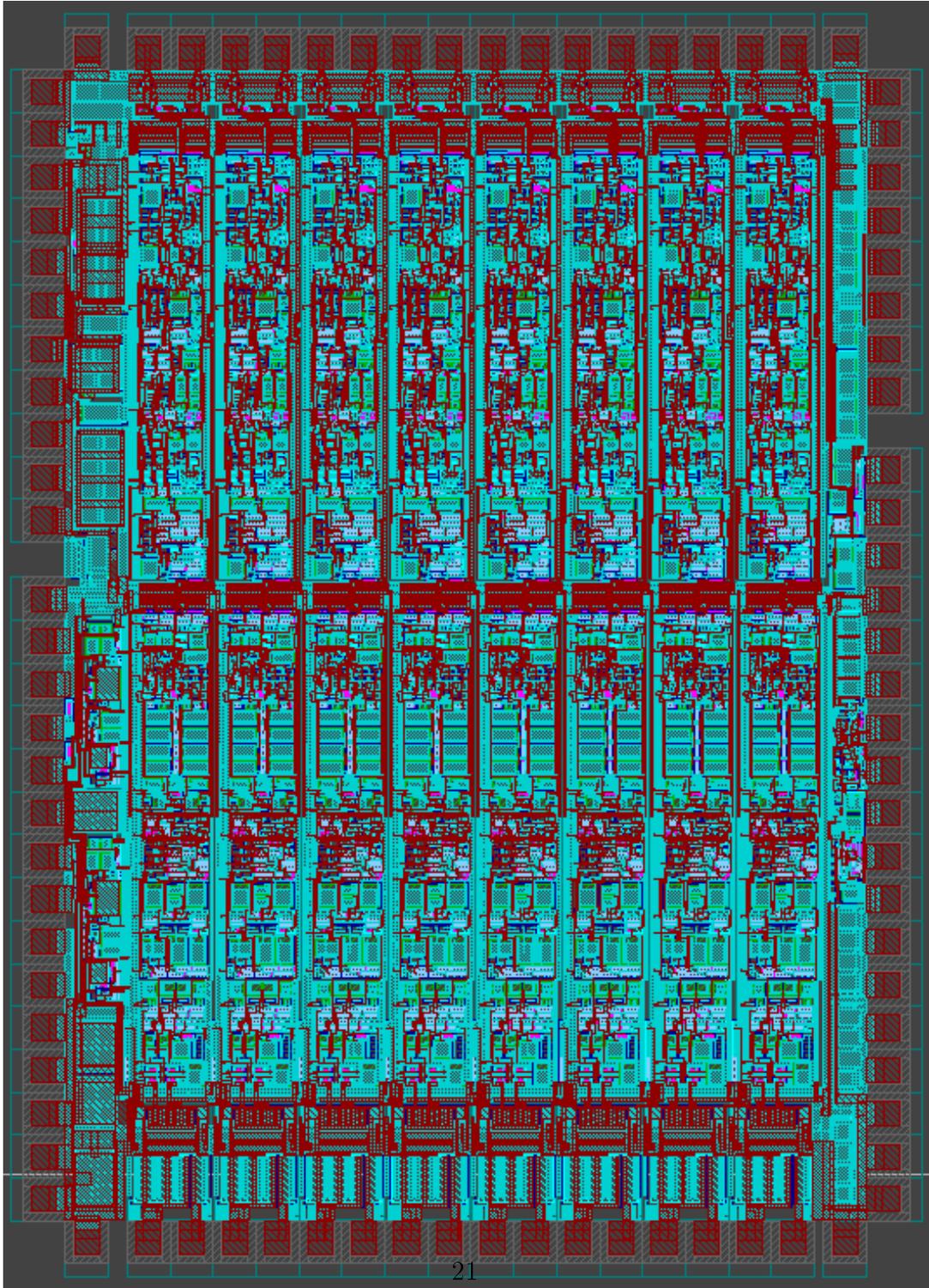


Figure 9: *The layout of the ASDQ chip.*

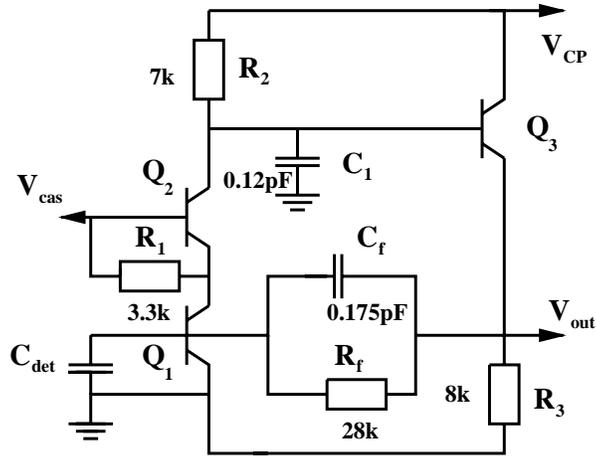


Figure 10: *The Preamplifier Schematic.*

and the collector is connected to the signal to help catch the initial parts of a breakdown pulse.

In order to dissipate the energy from an inductive spike in the positive direction, the signal is attached to several resistors in a smaller epitub. The epitub contacts attach to a separate supply held at 1.2V.

The performance of this configuration has been tested in fabricated ASDQ's. A 560pF coupling capacitor, charged to 3 kV is discharged into the input of the ASDQ. No performance change is observed in the ASDQ.

The specifics of the input protection circuit are summarized in table 1.

5.4 Preamplifier

The preamplifier consists of a three transistor cascoded common emitter configuration that has a rise time of 1.5ns and an approximate gain of 3 mV/fC. Although the input from the chamber is single ended, two identical preamplifiers are implemented for each channel. This pseudo-differential configuration provides a DC balanced input to the differential shaper and allows good common mode noise rejection. Inputs to each Preamplifier at the package level allow the exploitation of differential noise pickup rejection methods. A simplified schematic for each of the Preamplifiers is shown in figure 10.

Figure 8 shows the response of the preamplifier to an input signal from

a Cosmic ray track. Figure 11 shows the evolution of the signal through the preamplifier. The signal enters from the left and is sent to the shaper on the right. The gain of the preamp is 1.5 mV/fC and it is linear for charges upto 4 pC. The preamp has a fast shaping time, 1.5 ns, and does not appreciably shape the input signal.

The preamp input impedance is controlled by balancing the capacitive and resistive feedback in the circuit. At low frequencies it is matched to the 260 Ω characteristic impedance of the COT. In order to maximize charge collection with the expected input stray capacitance of 10 pF, the input impedance has been designed to roll off at high frequency. The roll off is about 30% at 30 MHz. Figure 12 shows a SPICE simulation of the input impedance of the ASDQ as a function of frequency for three different values of the stray capacitance, 0 pF, 10 pF and 20 pF, where the realistic value is estimated to be 10 pF.

The intrinsic noise of the preamplifier in 8 ns is determined from SPICE to be 2100 electrons. The termination resistance of the wire introduces an additional noise of about 1500 electrons making the intrinsic noise of the system of the order of 4000 electrons. For efficient triggering, we require a signal to noise ratio in the preamplifier to be about 5 to 1. For a Gas Gain of 2×10^4 , this corresponds to $\frac{5 \times 4000}{0.375 \times 20000 \times 0.15} \sim 18$ electrons or 6 clusters as the minimum amount of primary ionization in the chamber.

The details of input impedance, noise and the preamplifier are summarized in tables 2 and 3 respectively.

Signal Input	
ASDQ Impedence (Low Freq.)	260 Ω
ASDQ Impedence (High Freq.)	Roll-off by 30% at 30 MHz
Noise (10pF inp. cap)	$\sim 2300e$
Noise (10pF+COT+Term. Res)	$\sim 3800e$

Table 2: ASDQ input impedance and noise

The Preamplifiers are inter-weaved in the layout in order to reduce imbalanced noise pickup. In addition, the input transistors of the Preamps are laid out in a *cross-quad* formation which ensure good geometric and thermal matching, and protect against systematic process variations.

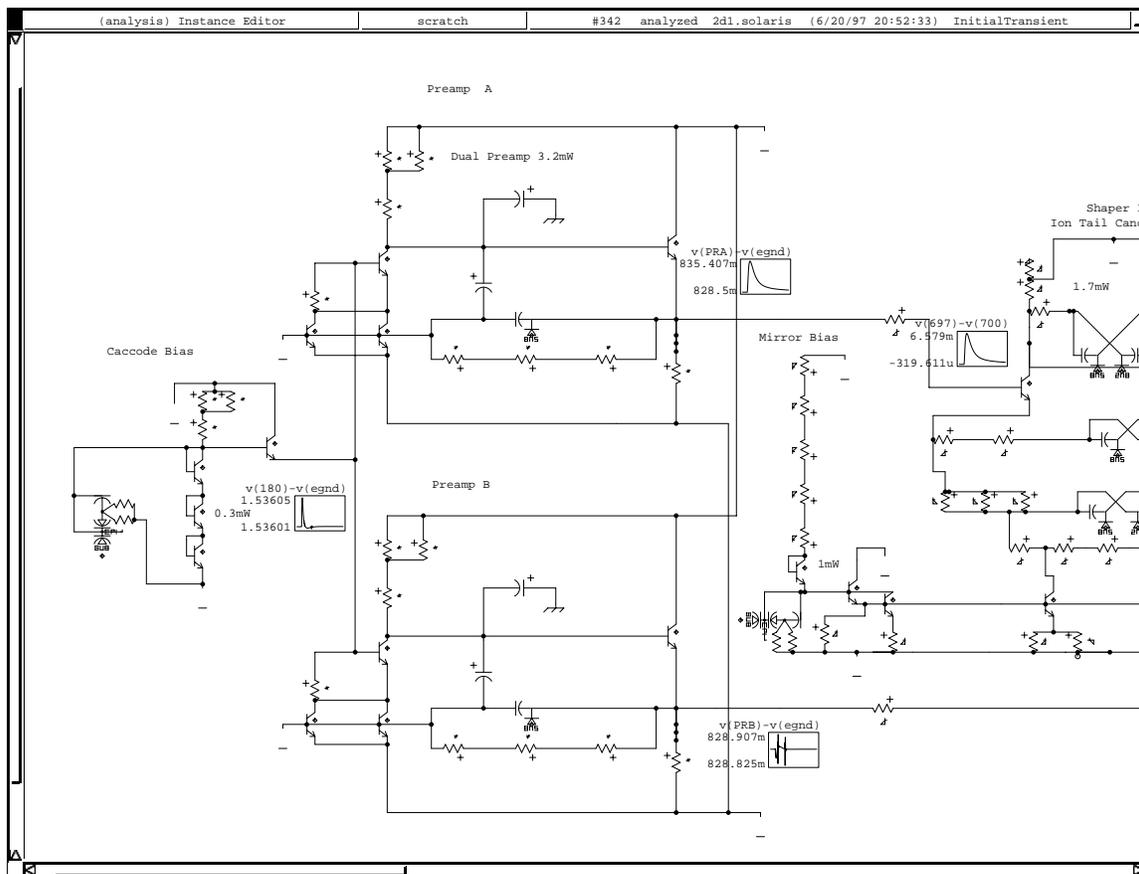


Figure 11: *Signal evolution through the Preamplifier.*

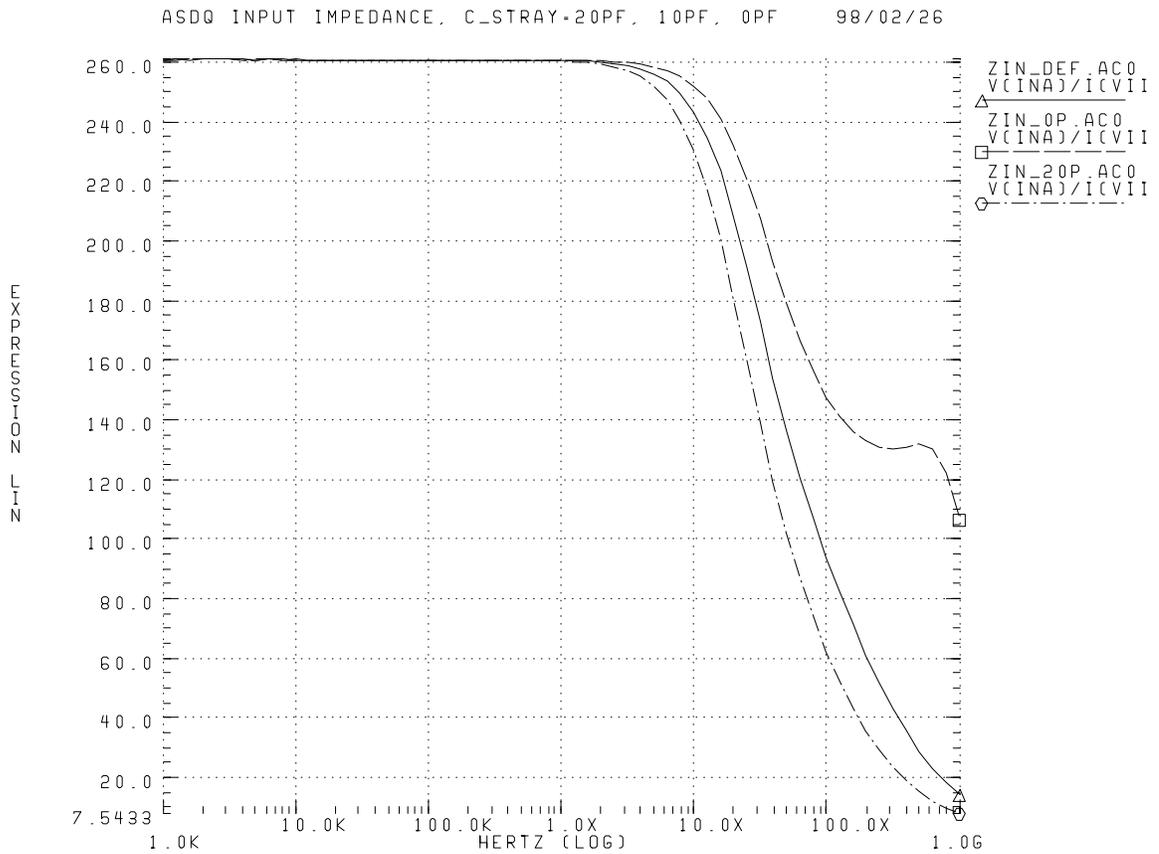


Figure 12: *ASDQ input impedance as a function of frequency. The three curves are for stray capacitance of 0, 10 and 20 pF. The realistic estimate for the stray capacitance is 10 pF (middle curve).*

Preamplifier	
Gain	1.5mV/fC
Range	linear to 4pC
Shaping	1.5ns rise

Table 3: Preamp Specifications

5.5 Shaping and Tail Cancellation

The ASDQ has a two stage fully differential multipole shaper. The goal of the shaping stage is to eliminate the ion tail using the technique of pole-zero cancellation. In addition, the tail induced by the preamp is also eliminated. The shaper consists of two stages, the first stage eliminates the ion tail and the second the preamp tail. In addition, the shaper provides a limited and fully differential signal to the BLR.

Figure 13 shows the schematic of the shaping stage. The signal processed by the preamp enters from the left and after the shaping stage is sent to the BLR on the right.

Equivalent pole shaping results in an almost symmetric impulse response. This is good for double pulse resolution and does not impact the noise levels in the circuit. RC integrations in the collectors of each of the shaper stages in combination with the poles in the ion and preamp tail cancellation yield the almost symmetric impulse response. To minimize slew and optimize signal to noise, we have targeted a peaking time of 6 ns for the ion-tail compensated signal at the input to the Baseline Restorer. Additional shaping following the BLR increases the final peaking time to 8ns preceding the discriminator.

Ion tail cancellation depends on linear amplification of the input signal and is performed early (in stage one) of the shaper where the largest dynamical range exists. The first shaper stage consists of a cascoded differential pair with a pole zero network in the emitters. Although the signal is single sided at the bases of the first stage shaper, it becomes differential in the collectors where the first integration occurs. Figure 13 shows the output of the first stage of the shaper. It is seen that the ion tail contained in the input signal (on the left) has been eliminated at this stage.

The zero in the second stage of the shaper is intended to cancel the lowest

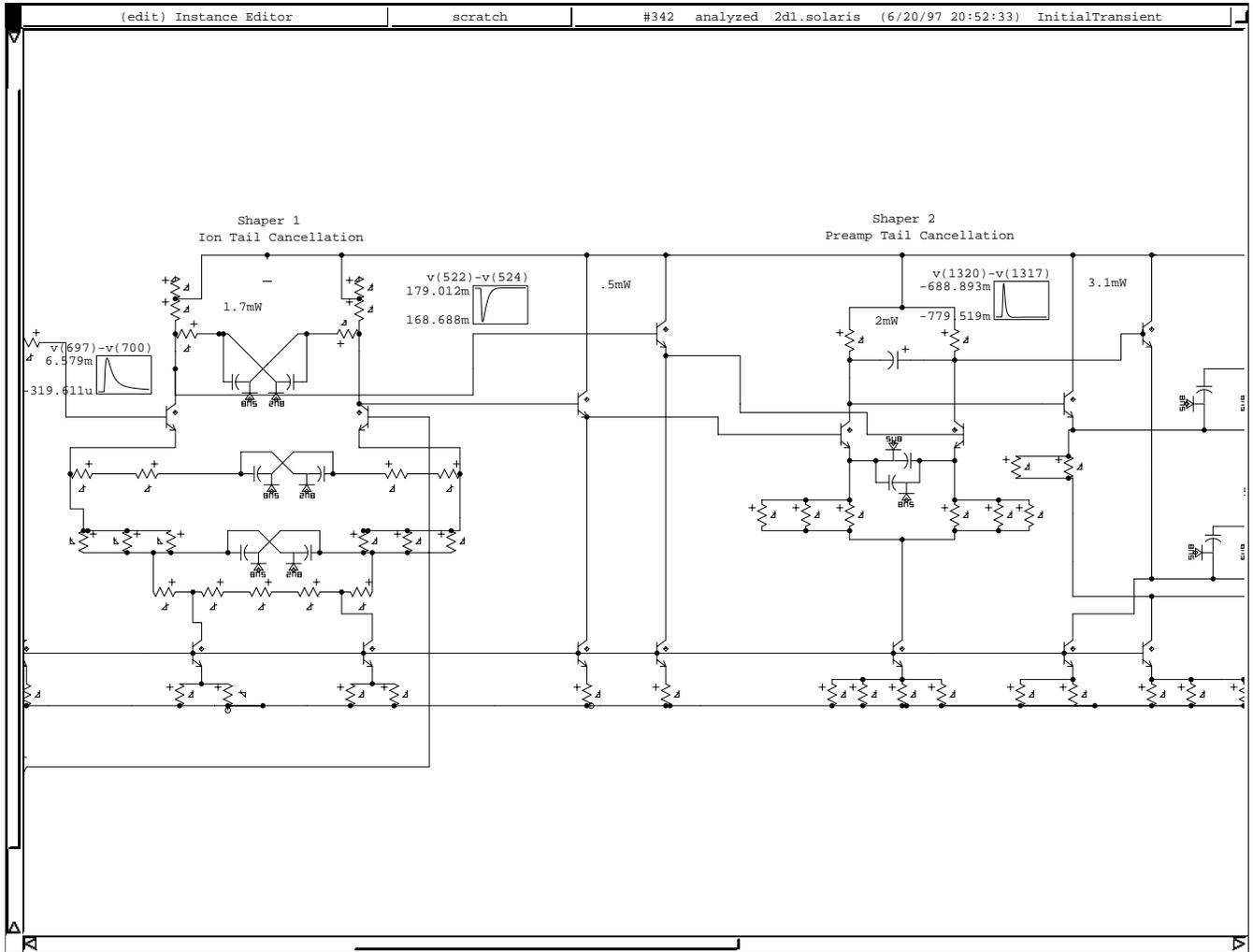


Figure 13: Schematic of the shaper.

frequency pole in the preamplifier. Figure 13 also shows the output of the second shaper stage where now the tail has been completely eliminated. It is also seen that the output from the shaper is quite narrow.

The specifications of the shaper are summarized in table 4. A signal of 2 fC into the preamp results in a 45 mV signal with a 6 mV overshoot at the BLR output. The first stage of the shaper is linear to about 600 fC and the second stage begins to limit for an impulse (single ion) signal of 120 fC on the wire. Looking at the same charge split into 4 equal ion depositions over a period of 10 ns, the FS range increases to greater than 250 fC. A plot of width vs charge, which is sensitive to area and not the peak of the voltage profile shows a very linear relationship to about 60 fC. The relationship is nearly linear to about 120 fC and begins an obvious rollover out beyond 300 fC.

Shaper Specs	
Gain	25 mV/fC
Range (Ion Tail)	≤ 600 fC
Range (Preamp Tail)	≤ 120 fC
Shaping	6 ns 0-Peak at BLR input
Undershoot	$\leq 2\%$

Table 4: Shaper Specifications

5.5.1 Attenuator

A level selectable times-two resistor-based attenuator (as shown in Figure 13) has been added after the emitter followers attached to the first differential pair in the Shaper. A 4K resistor is added in series with the output of each emitter follower and the input to the next differential pair. Attenuation is accomplished by supplying current to two diode-connected transistors which are attached to each other by an 8k resistance. When enabled, this provides a shunt resistance across the outputs, cutting the voltage input to the next differential pair stage by a factor of nearly 2.

5.6 Baseline Restoration (BLR)

The ASDQ has a fully differential BLR. The BLR offers several attractive advantages in signal processing. Its AC coupling removes DC process variations before the discriminator. It provides insensitivity to small offsets in the preamp arising mainly from differences in the base currents in the input transistors if the matched dual preamps. By breaking the DC path from input to output, it reduces the number of components that affect the DC offset, thus making it more feasible to consider a chip-wide threshold. In addition, its short time constant provides insensitivity to imperfections in the tail cancellation circuits. This is especially helpful in recovery from very large signals that saturate the shaper. In DC coupled circuits for comparison, several microseconds of unstable behavior can accompany an input pulse that is large enough to fully saturate the tail compensation network. Thus the BLR significantly improves high rate performance and allows earlier re-triggering and eliminates multiple triggers when tail cancellation is saturated.

The BLR circuit schematic is shown in Figure 14. Note that a 40K resistance, not shown in this schematic, has been added between the 8pF capacitors on the BLR side to set a known high impedance time constant.

The BLR implemented in the ASDQ has been designed to have minimal impact on the dE/dx capabilities. The initially proposed a baseline restorer consisted of a 10 pF integrating capacitor on each of the differential shaper outputs, followed by a single diode shunt that set the quiescent operating point of the other terminal of the capacitors. This arrangement provided satisfactory performance, maintaining a stable baseline, and introducing non-linear overshoot with minimal excursions. Examining the performance as an integrator, significant losses in integrated charge were found for signals spread out in time over periods of up to 20 ns. Feeling that this would result in an unpredictable dE/dx width encoding, alternative designs were explored.

The alternative design significantly improves the integration function and improves the baseline recovery. Refer to Figure 14. In this design, the shaper output is coupled to the BLR with two 8 pF capacitors. A four diode bridge offers a shunt path between the capacitors and holds each to the same potential. The current in the bridge is maintained by a differential pair biased to provide one third of the available current through the bridge in quiescent operation. The current available to this stage will be externally adjustable using a chip wide control by about $\pm 50\%$ to allow optimization after fab-

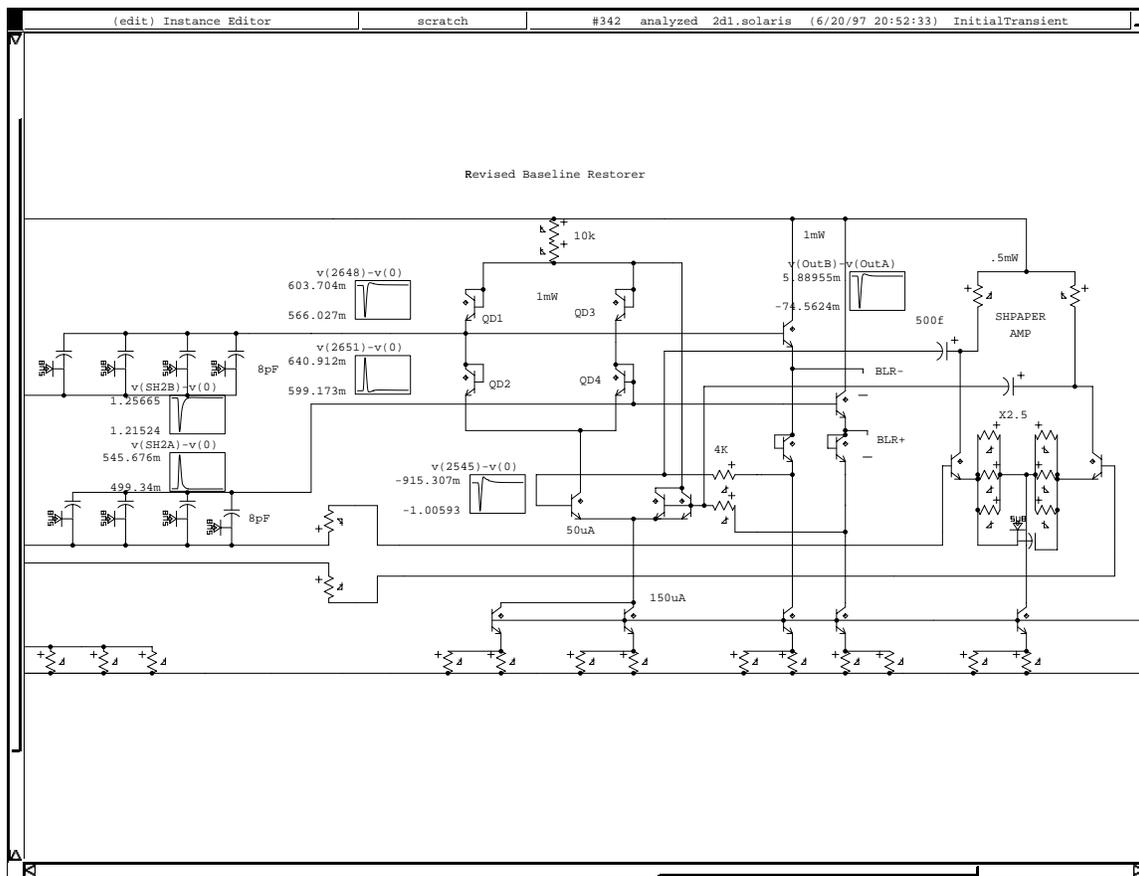


Figure 14: *The BLR Schematic.*

rication. The current in the bridge sets the shunt impedance between the outputs which is controlled directly by the BLR output level. The impedance goes to high values when the signal is of the desired polarity and goes to very low values when the output polarity is below baseline. Figure 15 shows the response at the BLR output for signals ranging between 5 and 45 fC. The response of the BLR is seen to be linear over this charge range.

The 800 mV lobe of the 45 fC pulse is followed by a 33 mV excursion below baseline that is largely gone in 15 ns. The recovery time is shown in figure 16 where the discriminator response is plotted for a series of simulations with two 15 fC input pulses followed by a 2 fC pulse varied from 25 to 55 ns following the first 15 fC pulse. Both the single diode BLR and the new BLR retrigger within 35 ns of first pulse with the discriminator set to 1.5 fC. To improve the sensitivity to low level signals, the shaper output is used to drive a $2.5\times$ gain stage which is capacitively coupled to the diode bridge current regulator.

Also, it should be noted that the negative undershoot, as a fraction of the positive lobe of the signal, is progressively smaller for larger signals.

The specifications of the BLR are summarized in table 5.

BLR	
Gain	$\geq 66\%$ (3fC), 90% ($> 30\text{fC}$)
Range	120 fC
Shaping	No significant additional shaping for large pulses
Undershoot	≤ 3 fC (Signals $\leq 100\text{fC}$)

Table 5: BLR Specifications

The response to a 1 fC chamber-like input signal at the shaper and BLR outputs for BLR circuits is plotted in Figure 17. While the signal attenuation is not large for this minimum size signal, the most striking feature is that the overshoot is significantly smaller than a simple diode clamp. This behavior continues to much larger pulseheight as can be seen in Figure 18.

Figure 19 shows the response at the shaper and BLR outputs for a 20 fC chamber like pulse split into three equal 6.7 fC depositions that are 5 ns apart. As is seen in the plot, the effect in the BLR output signal is minimal.

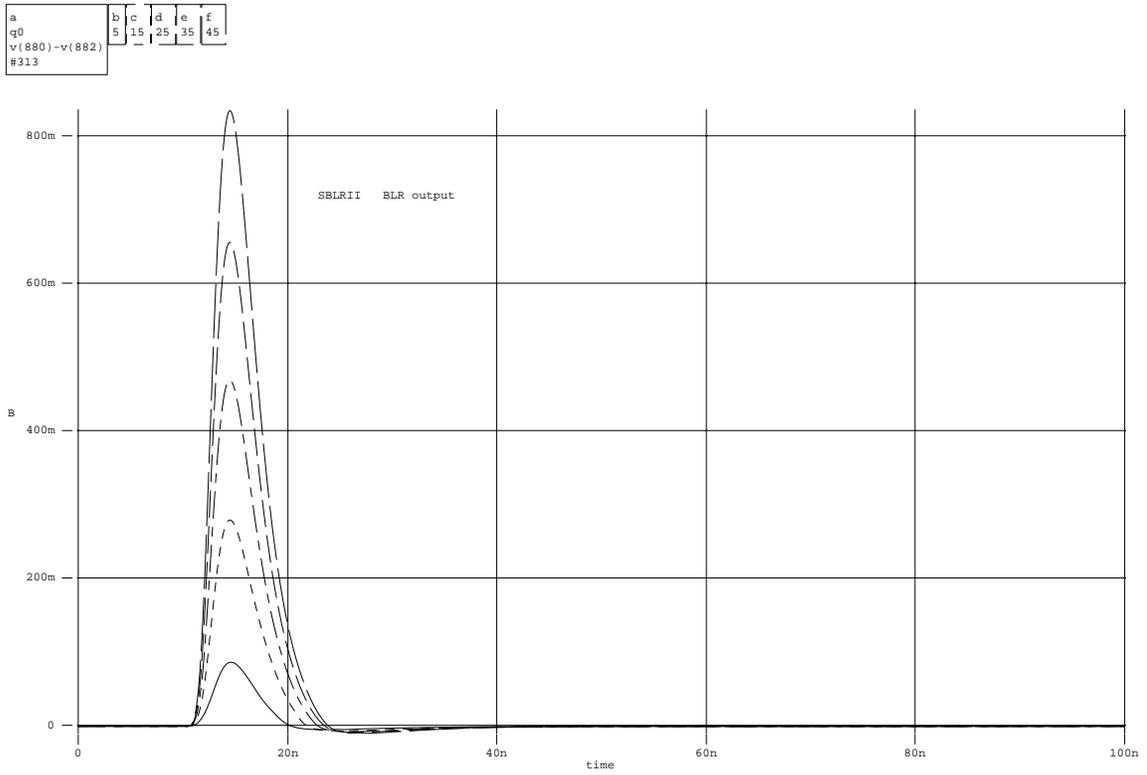


Figure 15: *Response at the BLR output for signals ranging between 5 and 45 fC.*

a	b	c	d	e
dly2	35n	45n	55n	65n
v(797)-v(798)				
#312				

