



Fermi National Accelerator Laboratory

SVX II Silicon Strip Detector Upgrade Project

Production Test Plan Summary

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1. GENERAL INFORMATION

This document is a summary of component, subsystem and system test plan for the readout electronics (DAQ) for the CDF Silicon System (SVX) for Run II. The series of tests for each system component and subsystem, as well as system tests using the CDF SVX DAQ software are given with brief explanations. Thus, this document summarizes required testing before system components can be installed at B0. This document also describes the uses of different kinds of test stands and an explanation for the need for given quantities of various test stands.

2. Component, Subsystem & System Test Plan Summary

2.1 SRC Modules

Modules received from the assembly house will go through the following sequence of tests at FCC:

1. Visually inspect the quality of the pc board and its assembly.
2. Check w/ DVM for electrical shorts between power & ground.
3. Power up the module and measure at several critical points for excessive voltage drops.
4. Insert any components not supplied to assembly house (i.e. programmable devices).
5. Check basic operation of the module.
 - VME reads & writes if possible.
 - Low speed data tests w/ GSTM.
 - Error insertion tests w/ GSTM.
6. Full speed tests w/ system modules.
7. Temperature cycle tests w/ multiple modules.
8. Long term system reliability tests w/ multiple modules and DAQ Software.

2.2 VRB, VRB Fanout & VTM Modules

Modules received from the assembly house will go through the following sequence of tests at FCC:

1. Visually inspect the quality of the pc board and its assembly.
2. Check w/ DVM for electrical shorts between power & ground.
3. Power up the module and measure at several critical points for excessive voltage drops.
4. Insert any components not supplied to assembly house (i.e. programmable devices).
5. Check basic operation of the module.
 - VME reads & writes if possible.
 - Low speed data tests w/ GSTM.
 - Error insertion tests w/ GSTM.
6. Full speed tests w/ system modules.
7. Temperature cycle tests w/ multiple modules.
8. Long term system reliability tests w/ multiple modules and DAQ Software.

2.3 FIB, FIB Fanout (FFO) & FIB Transition Module (FTM) Modules

Modules received from the assembly house will go through the following sequence of tests at FCC:

1. Visually inspect the quality of the pc board and its assembly.
2. Check w/ DVM for electrical shorts between power & ground.
3. Power up the module and measure at several critical points for excessive voltage drops.
4. Insert any components not supplied to assembly house (i.e. programmable devices).
5. Check basic operation of the module.
 - VME reads & writes if possible.
 - Low speed data tests w/ GSTM.
 - Error insertion tests w/ GSTM.
6. Full speed tests w/ system modules.
7. Temperature cycle tests w/ multiple modules.
8. Long term system reliability tests w/ multiple modules and DAQ Software.

2.4 Port Cards

Modules received from the assembly house will go through the following sequence of tests at FCC:

1. Visually inspect the quality of the hybrid substrate and its assembly.
2. Check w/ DVM for electrical shorts between power & ground.
3. Power up the substrate and measure at several critical points for excessive voltage drops.
4. Insert any components not supplied to assembly house (i.e. programmable devices).
5. Connect to SVX3 emulator & check basic operation of the module.

- Low speed data tests w/ GSTM.
 - Error insertion tests w/ GSTM.
6. Full speed tests w/ system modules.
 7. Temperature cycle tests w/ multiple modules.
 8. Long term system reliability tests w/ multiple modules and DAQ Software.

2.5 Control/Timing & Data G-Links and Optical Splitters

Modules received from the assembly house will go through the following sequence of tests at FCC:

1. Visually inspect the quality of the assemblies.
2. Interconnect portions of the optical assemblies to be tested.
3. Check basic operation of the optical assemblies.
 - Low speed data tests w/ GSTM.
 - Error insertion tests w/ GSTM.
4. Full speed tests w/ system modules.
5. Temperature cycle tests w/ multiple modules.
6. Long term system reliability tests w/ multiple modules and DAQ Software.

2.6 Pleaded Foil & Flex Cable Control/Timing Links

Modules received from the assembly house will go through the following sequence of tests at FCC:

1. Visually inspect the quality of the assembly.
2. Check w/ DVM for electrical shorts.
7. Interconnect portions of the optical assemblies to be tested.
3. Check basic operation of the module.
 - Low speed data tests w/ GSTM.
 - Error insertion tests w/ GSTM.
4. Full speed tests w/ system modules.
5. Temperature cycle tests w/ multiple modules.
6. Long term system reliability tests w/ multiple modules and DAQ Software.

2.7 Optical (DOIM) Data Links

Modules received from the assembly house will go through the following sequence of tests at FCC:

1. Visually inspect the quality of the DOIM.
2. Insert the DOIM in its test fixture.
3. Check basic operation of the module.
 - Perform read/write transfers.
 - Determine BER of device.
4. Full speed tests w/ DOIM in final system modules.
5. Temperature cycle tests w/ multiple modules.
6. Long term system reliability tests w/ multiple modules and DAQ Software.

3. Test Stand Quantities & Usage

3.1 GSTM-Based Test Stands

The GSTM-Based Test Stand (GTS) is specialized to meet the initial low speed testing of incoming modules from assembly houses. Basically the incoming module will be interconnected to the various GSTM adapters and all low level tests are to be performed by the GSTM. The GSTM Based Test Stand consist of a single subrack with a split J3 backplane to permit the VRB or FIB subsystem to be tested.

The number of GSTM-Based Test Stands expected to be assembled are as listed below:

- 1 -2 VRB testing at FCC
- 1 - FIB testing at FCC
- 1 - SRC testing at Harvard
- 1 - Miscellaneous testing
- 4 - Total Production Test Stands

3.2 Production Test Stand

The Production Test Stand (PTS) is a general test system controlled by an SRC module rather than a GSTM with data fed from a DEM-II test module. The PTS supports the testing of both VRB and FIB subsystems within a single VIPA subrack with use of a split J3 backplane. This reduces the costs of the test stands (1-CPU, 1-PS, 1-Subrack) and minimally impacts the reliability of the tests being performed. All the system modules that pass in the GSTM-Based test stands will move to one of the Production Test Stands (PTS) consisting a full complement of system modules for high speed, temperature and long term reliability tests.

The number of Production Test Stands expected to be assembled are as listed below:

- 1 - 3 VRB testing at FCC
- 1 - 2 FIB testing at FCC
- 1 - 2 Ladder testing at lab D
- 1 - 3 Miscellaneous testing
- 7 - Total Production Test Stands

3.3 Integration Test Stands

The Integration Test Stand (ITS) is also a general test system controlled by an SRC module with data fed from a Port Card rather than a DEM-II. The ITS supports the testing of up to 12 VRBs and 12 FIBs simultaneously for long term reliability testing and DAQ software integration & testing. The ITS is as close to the final system as possible without fully duplicating its CDF system at FCC; consisting of two VIPA standard subracks and a full complement of all modules, cables and accessories. All the system modules that pass in the Production Test Stands will move to the Integration Test Stand (ITS) in batches of 12 modules.

The number of Integration Test Stands (ITS) expected to be assembled at FCC is one to two.

3.4 DOIM Production Test Stands